Mitigating Voltage Lead Errors of an AC Josephson Voltage Standard by Impedance Matching

Dongsheng Zhao, Helko E. van den Brom and Ernest Houtzager

VSL B.V., P.O. Box 654, 2600 AR Delft, the Netherlands

E-mail: hvdbrom@vsl.nl

Abstract. A pulse-driven AC Josephson voltage standard (ACJVS) generates calculable AC voltage signals at low temperatures, whereas measurements are performed with a device under test (DUT) at room temperature. The voltage leads cause the output voltage to show deviations that scale with the frequency squared. Error correction mechanisms investigated so far allow the ACJVS to be operational for frequencies up to 100 kHz. In this paper, calculations are presented to deal with these errors in terms of reflected waves. Impedance matching at the source side of the system, which is loaded with a high-impedance DUT, is proposed as an accurate method to mitigate these errors for frequencies up to 1 MHz. Simulations show that the influence of non-ideal component characteristics, such as the tolerance of the matching resistor, the capacitance of the load input impedance, losses in the voltage leads, non-homogeneity in the voltage leads, a non-ideal on-chip connection and inductors between Josephson junction array and the voltage leads, can be corrected for using the proposed procedures. The results show that an expanded uncertainty of 12 parts in 10^6 at 1 MHz and 0.5 part in 10^6 at 100 kHz is within reach.

PACS. 06.20.-f Metrology, 06.20.fb Standards and calibration, 06.30.Ka Basic electromagnetic quantities, 84.37.+q Measurements in electric variables

Submitted to Measurement Science and Technology

1. Introduction

Using a pulse-driven AC Josephson voltage standard (ACJVS) one can generate calculable AC voltage signals [1]. Most of the researches in the last two decades had focused on increasing the output voltage towards levels which were useful for practical applications [2],[3]. However, these signals are generated in a cryoprobe at low temperatures, but measured with a device under test (DUT) at room temperature. The voltage leads cause the output voltage to show deviations that scale with the frequency squared [4]. These frequency dependent deviations turn out to be the dominant source of uncertainty for frequencies above approximately 10 kHz. For practical applications, this frequency dependence limits the ACJVS output frequency to approximately 100 kHz [4]-[7].

When measuring the output voltage of an ACJVS with an AC reference voltmeter, the values turned out to be larger than the corresponding calibration results. Therefore, until recently these deviations were thought of as the result of a resonance in the system, dependent on parameters such as cable inductance and capacitance, that could be damped, filtered or corrected for. However, several possible approaches to deal with this resonance, such as the use of very low inductive cable, have shown unexpected measurement results.

Recently it is discussed that these deviations can also be understood in terms of electromagnetic waves reflected by the DUT and the ACJVS due to impedance mismatch, even for signal path lengths much shorter than the signal wavelength [8]. The deviations being possible to describe in terms of reflected waves suggests that solutions can be found in methods commonly used at radio and microwave frequencies to minimize or compensate these reflected waves.

The most straightforward solution is using a smaller cryostat to reduce the cable length [9], since the deviation increases proportional to the cable length L squared. Reducing the cable length, however, will only lower the deviations by an order of magnitude, but will not fully diminish them.

Another method is detection of the reflected wave using a directional coupler and re-injection of a compensation signal. For wavelengths as long as dealt with in the experiments described here this could be achieved using a so-called tandem match coupler, which is used in radio technology [10]. However, this method is expected not to have the desired accuracy.

The approach proposed in this paper is to use impedance matching, such that reflections are avoided or reduced as much as possible. The voltages measured at any point along the transmission line are the same if no reflections occur at the source side and the load side. The impedance matching requirement is a common design criterion in the fields of radio frequency (RF) or signal integrity (SI). In this paper the impedance matching approach is applied to mitigate the errors in an AC Josephson voltage standard, where the signal path is much smaller than the wavelength (i.e., typically 200 m for a 1 MHz signal as compared to voltage leads of less than 2 m).

2. Theory

2.1. Reflected waves at low frequencies

An ACJVS can be modeled as a voltage source V_S with output impedance Z_S at $x = 0$ and a transmission line of length L with characteristic impedance Z_C representing the voltage leads, terminated by a load Z_L being the (high-ohmic) input impedance of the DUT (see figure 1). The general equation for the voltage $V(x)$ along such transmission line is given by [11]

$$V(x) = \frac{1 + \Gamma_L e^{-j2\beta L} e^{j2\beta x}}{1 - \Gamma_S \Gamma_L e^{-j2\beta L}} \frac{Z_C}{Z_C + Z_S} V_S \, e^{-j\beta x} \tag{1}$$

Here, the phase constant β is equal to $\omega/v = 2\pi/\lambda$, where $\lambda = v/f$ is the wavelength of the electromagnetic waves having frequency f and propagation velocity v. The reflection coefficients Γ_S and Γ_L at the source and load, respectively, are equal to

$$\Gamma_S = \frac{Z_S - Z_C}{Z_S + Z_C} \text{ and } \Gamma_L = \frac{Z_L - Z_C}{Z_L + Z_C}.$$

For a Josephson junction array we assume $Z_S \approx 0$ such that $\Gamma_S \approx -1$, and for a DUT with high input impedance $Z_L \gg Z_C$ which means $\Gamma_L \approx 1$. Filling in these numbers in equation (1) one can find that for wavelengths $\lambda \gg L$ the voltage measured at the DUT is approximately equal to

$$V(L) \approx \frac{1}{\cos(\beta L)} V_S \approx (1 + 2\pi^2 (fL/v)^2) V_S \tag{2}$$

This equation confirms the frequency behavior observed before, i.e., the deviation increases with the frequency squared [4]. Note that the deviation only depends on cable length, frequency, and the propagation velocity, *independent* of other parameters. Filling in the numbers and using $v = 1/\sqrt{lc}$, l and c being the inductance and capacitance per meter, for a 4 meter cable (which includes the twisted pair cable inside the probe and the coaxial cables to

DUT and spectrum analyzer) the deviation at 1 MHz is found to be 0.8 %, which is slightly below the experimental result of almost 1 % obtained before [4].

For higher frequencies the input impedance of the DUT becomes capacitive and the approximation $\Gamma_L \approx 1$ should be replaced by:

$$\Gamma_L = \frac{Z_L - Z_C}{Z_L + Z_C} = \frac{\frac{1}{j\omega C_L} - Z_C}{\frac{1}{j\omega C_L} + Z_C} = e^{-j2Z_C\omega C_L} \tag{3}$$

where C_L is the capacitance of the load impedance of the DUT. Starting from equation (1), and still using $\Gamma_S = -1$, the voltage measured at the DUT is found to be equal to

$$V(L) = \frac{\cos(\beta\Delta L)}{\cos(\beta(L+\Delta L))} V_S \approx \frac{1}{\cos(\beta(L+\Delta L))} V_S \tag{4}$$

where $\Delta L = \frac{1}{2\beta} 2Z_C\omega C_L = vZ_C C_L$ can be considered as the equivalent cable length offset caused by the input capacitor of the DUT modifying the length L in equation (2). Note that the last approximation is only valid if $\Delta L \ll L$. Hence, for a cable with 50 Ω characteristic impedance and propagation velocity v equal to 66 % of the speed of light in vacuum, an input capacitance of 40 pF corresponds to an apparent cable length of 40 cm. When adding this equivalent cable length to the actual length (including twisted pair cable inside the probe and the coaxial cables to DUT and spectrum analyzer), using the same propagation velocity, equation (4) indeed gives the almost 1 % deviation at 1 MHz observed before [4].

2.2. Impedance matching for high impedance loads

The approach in this paper is to mitigate the frequency dependent voltage lead errors by impedance matching, i.e., by avoiding or suppressing the reflection of waves. Impedance matching is usually done at the source and the load side of the system, which implies that the source and load impedances Z_S and Z_L should be frequency independent broadband resistors with an impedance matching the characteristic impedance of the cable (typically 50 Ω). Using a matching load resistor means that the Josephson system should provide a considerable amount of current. Furthermore, the output voltage is reduced to half of the ACJVS voltage. To avoid these two unwanted side effects, instead, the impedance matching can be fulfilled at the source side of the system only. A series resistor with impedance $Z_S = Z_C$ can be inserted as close as possible to the Josephson junction array, such that $\Gamma_S = 0$.

As a consequence, the voltage $V(L)$ measured at the end of the transmission line is equal to

$$V(L) = \frac{Z_L}{Z_L + Z_C} V_S \tag{5}$$

Hence, the voltage at the DUT is *independent* of the length of the transmission line, and the

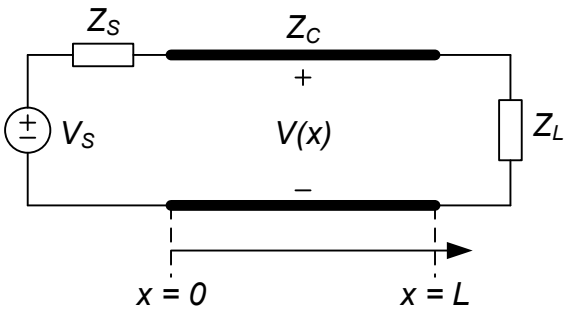

Figure 1. Transmission line model used in our calculations. Here, V_S represents the calculable Josephson voltage, Z_S is the output impedance of the Josephson junction array, Z_C is the characteristic impedance of the cable, $V(x)$ is the voltage along the transmission line, and Z_L is the (high-omhic) load of the DUT.

voltage is simply a voltage division of two impedance values. If the input impedance Z_L is high, the correction to the calculable value of V_S to obtain the output voltage value at the input port of the DUT is small and can be determined with high accuracy.

To reach this result a broadband low temperature resistance should be tuned until it matches the characteristic impedance of the cable. The criterion of satisfying this condition is also straightforward, i.e., until inserting an extra cable no longer changes the output voltage read by the DUT. Apart from a high stability DUT, in this ideal situation no additional instruments are needed.

3. Simulations and discussion

In the theory and tuning procedure presented above, the proposed impedance matching method is based on a very simplified model. In this model we assumed a high impedance resistive load in combination with a perfect transmission line. Several non-ideal properties of the components in the ACJVS and the DUT are ignored, such as the tolerance of the matching resistor, the capacitance of the load input impedance, losses in the voltage leads, non-homogeneity of the voltage leads, a non-ideal on-chip connection and inductors between Josephson junction array and the voltage leads. In the remainder of the paper, starting from the simplified model, the impact of the non-ideal conditions on the accuracy of the measurement result is analyzed one by one by means of simulations. Methods for improvement are proposed and simulated as well.

3.1. Simplified model

To investigate the effect of non-ideal experimental realization, the mitigation method using impedance matching is first implemented in PSpice[1] using an ideal transmission line and a purely resistive load of 10 MΩ. The time delay of the transmission line is set to 7.58 ns to represent a 1.5 m coaxial cable with 50 Ω characteristic impedance and propagation velocity v equal to 66 % of the speed of light in vacuum as specified for an RG-58A cable [10].

In the simulation, we assume that a 1 m extra cable is inserted to check the impedance matching at the source side, and the DUT has enough stability to identify 2 ppm amplitude variation at 1 MHz. The result after tuning is that Z_S is in a range between 49.98 Ω and 50.02 Ω. With this variation range of Z_S, the frequency dependent voltage lead errors of the voltage $V(L)$ measured at the end of the 1.5 m coaxial cable are shown in figure 2. We conclude that in this simplified model the voltage deviation at 1 MHz is reduced to less than 1 ppm if the impedance matching at the source side is fulfilled. The voltage ratio with perfect matching ($Z_S = Z_C$ = 50 Ω) is equal to 0.999995, a 5 ppm deviation from unity which is caused by the voltage division that can be calculated and corrected using equation (5).

[1] The manufacturers and types of instrumentation mentioned in this paper do not indicate any preference by the authors, nor does it indicate that these are the best available for the application discussed.

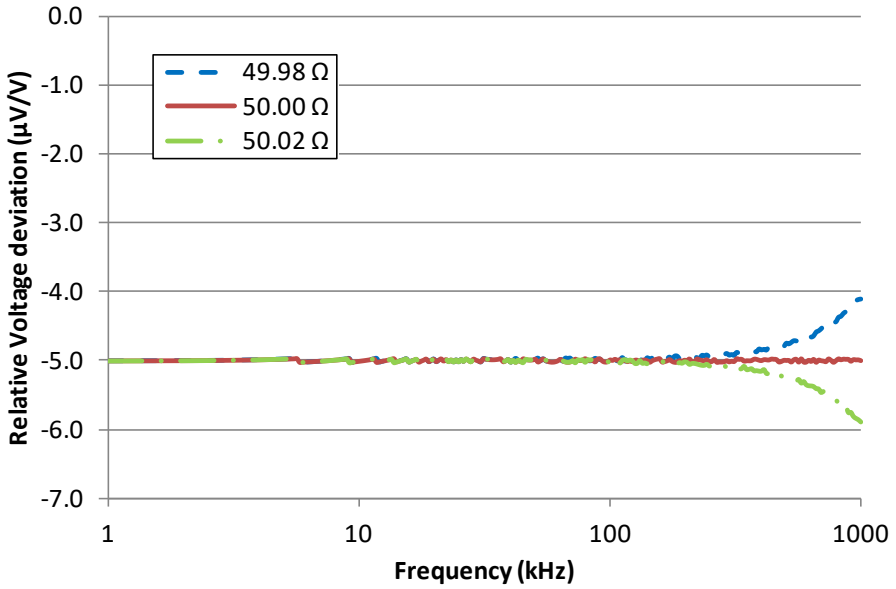

Figure 2. Simulation results of the relative voltage deviation after tuning Z_S within ±0.02 Ω tolerance to obtain impedance matching.

3.2. Input capacitance of the DUT

Above, the input impedance of the DUT is modeled using a 10 MΩ resistor. However, in practice voltmeters have capacitive inputs and present heavier loads at higher frequencies. To investigate the effect of this parallel capacitance the input impedance of a Fluke 792A AC/DC transfer standard has been modeled as a 10 MΩ resistor in parallel with a 40 pF capacitor.

Simulations show that even though a 50 Ω matching resistor has been used, the deviation turns out to be 84 ppm at 1 MHz, independent of the cable length. Obviously, correction for the influence of the input impedance of the DUT is inevitable if uncertainties below the 10^{-4} level at 1 MHz should be reached.

The deviation caused by the capacitive input impedance can be determined experimentally and corrected for using the following steps:

1. Follow the same procedure to tune the source impedance Z_S until inserting an extra cable no longer changes the output voltage read by the DUT. Note that for lossless transmission lines the output voltage at any frequency can be taken, so for highest sensitivity the highest frequency of 1 MHz is chosen.
2. The measurement result of the DUT with this tuned value of Z_S is saved as $M_1(f)$ which is equal to
$$|M_1(f)| \approx V_S \frac{R_L}{R_L + Z_C}\left(1 - \frac{1}{2}(2\pi f C_L Z_C)^2\right)|H(f)| \qquad (6)$$
where $H(f)$ denotes the frequency response of the DUT and the resistive ratio factor is introduced to make this equation valid in the DC and low frequency regime as well.
3. Add a series resistor R_X with a value of $(\sqrt{2}-1)Z_C$, at the input port of the DUT, see figure 3. For a 50 Ω cable, this value is about 20.7 Ω. The effect of inserting this resistor is that the deviation is even increased. This measurement result of the DUT is saved as $M_2(f)$, which is equal to
$$|M_2(f)| \approx V_S \frac{R_L}{R_L + Z_C + R_X}\left(1 - \frac{1}{2}(2\pi f C_L \sqrt{2} Z_C)^2\right)|H(f)| \qquad (7)$$
Note that a similar resistive ratio factor is introduced here as in equation (6).
4. By using the ratio of the measurements performed in the previous two steps one can find that the voltage $V(L)$ provided at the input port of the DUT can be calculated using:

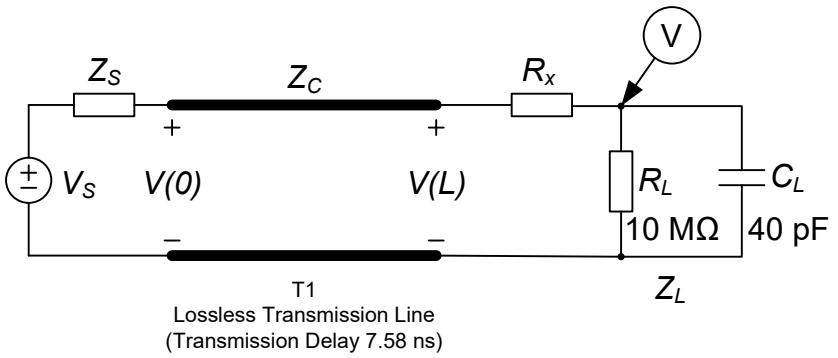

Figure 3. Transmission line model considering the capacitive input impedance of the DUT.

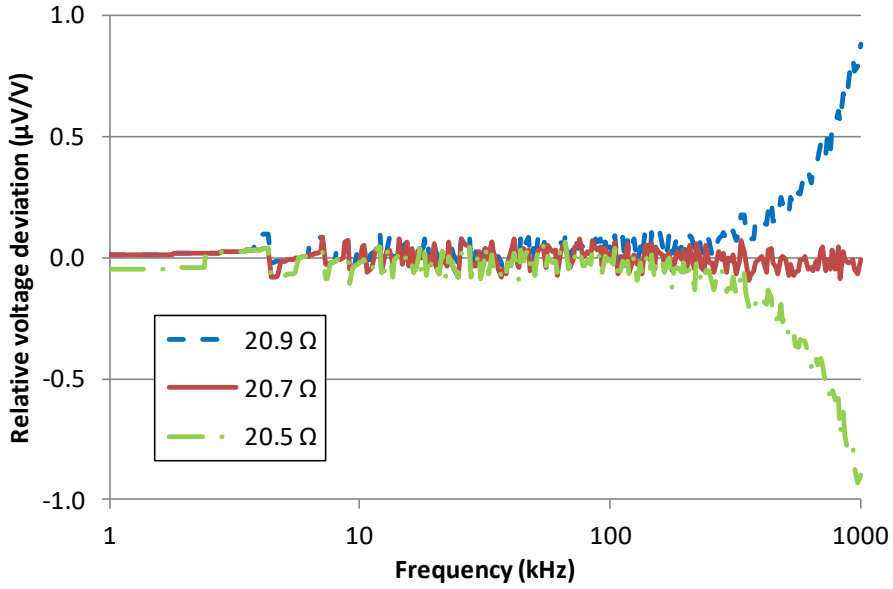

Figure 4. Evaluation of the error caused by the tolerance of the inserted resistor R_X used to correct for the influence of the capacitance at the input of the DUT. The y-axis shows the deviation after the correction in step 4 for different values of the inserted resistor R_X for perfectly matched Z_S.

$$V(L) \approx V_S \frac{R_L}{R_L + Z_C} \left| \frac{M_2(f)}{M_1(f)} \right| \left(1 + \frac{R_X}{R_L + Z_C} \right) \tag{8}$$

The key advantage of this method based on ratio measurements is that apart from the effect of the capacitive input impedance of the DUT, other errors such as the offset due to the matching impedance (equation (5)) and the intrinsic frequency response of the DUT itself are cancelled out. This approach avoids the characterization work of the cable and connectors [12], which was only successful for frequencies up to about 100 kHz.

The tuned value of Z_S is still in the range between 49.98 Ω and 50.02 Ω after step 1. Simulations show that the final result after the procedure including steps 2-4 is that the voltage deviation at 1 MHz is at most 1.5 ppm if the impedance matching at the source side is fulfilled. The error caused by the allowed tolerance of the inserted resistor R_X in step 3 is evaluated and shown in figure 4. From this figure it can be seen that if the inserted resistor has a tolerance of 1 %, the residual error after correcting the influence caused by the input impedance of the DUT is less than 1 ppm at 1 MHz. Note that this residual error does not depend on the cable length, and is additional to the error due to the tolerance of the matching impedance at the source side.

3.3. Lossy transmission line

In the theory and simulations presented above, to simplify our calculation, we have used a lossless transmission line model. In reality, all cables are lossy. Instead of using the specifications of the commonly used RG-58A cable [10], a low-loss coaxial cable is chosen. Using the attenuation formulae and cable specifications from [13], one can find that the signal attenuation is around 0.32 dB per 100 m length for an LMR-500 flexible low-loss cable at 1 MHz. This attenuation means that the voltage at the load side is lower than the voltage at the source side by 0.056 % at 1 MHz for a 1.5 m long cable, which is already a huge discrepancy. However, when terminating the cable with a 10 MΩ resistor with 40 pF capacitor in parallel instead of 50 Ω, limited current is flowing through the lossy line, and the attenuation is only 4 ppm for 1.5 m cable at 1 MHz. Note that the propagation velocity in this cable is equal to 86 % of the speed of light in vacuum at 1 MHz, whereas for the RG-58A it is equal to 66 %.

The effect of the cable losses will be reduced even further when using the procedures mentioned in the previous Section. First, the tuning procedure described in step 1 in Section 3.2 was done by inserting a 1 m long cable and checking the deviation at 1 MHz to determine the matching impedance, which is now in the range between 49.90 Ω and 49.96 Ω due to the cable losses. The result of the tuning procedure for different matching resistors is illustrated in figure 5. The offset of 0.5 ppm is due to the distributed resistance and conductance of the dielectric material of the inserted 1 m long lossy line.

As a next step, correction for the influence of the input impedance of the DUT as described in steps 2-4 in Section 3.2 is carried out. By taking the ratio of the two measurement results which is done in the last step, the effect of the losses is suppressed intrinsically. The residual error is shown in figure 6, which indicates that the final error is less than 2 ppm at 1 MHz. Note that when using for instance the specification of a RG-58A cable with 1.4 dB per 100 m length, calculations show that this number increases to 40 ppm. Hence, from these simulations we conclude that using low-loss coaxial cables is important to keep the loss corrections small.

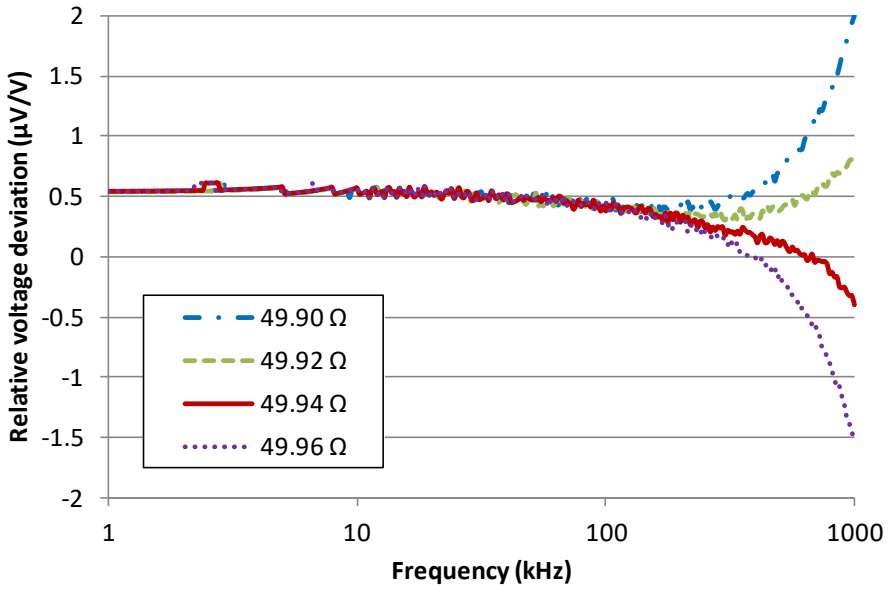

Figure 5. Tuning Z_S to obtain impedance matching when taking into account a parallel input capacitance and a lossy line. The y-axis shows the ratio between the voltage measured with and without inserting the extra 1 m cable, respectively.

Furthermore, from figure 6, small frequency dependence can be observed below 1 MHz as well, even with perfectly matched impedance at 1 MHz. It turns out that there is also a small dependence on cable length. Indeed, for a lossy transmission line, the impedance matching is specific for one particular frequency and cable length, resulting in an additional error of significantly less than 1 ppm at other frequencies.

3.4. Non-homogeneous characteristic impedance along the cable

In the previous model, the connection between the ACJVS and the DUT is treated as a single homogeneous transmission line, with identical characteristic impedance. To evaluate the impact of a possible non-homogeneity along the cable we replaced the transmission line in our model by two transmission lines with different characteristic impedance and performed the whole procedure described in Section 3.2. In the calculation we assume a fraction of 10 %

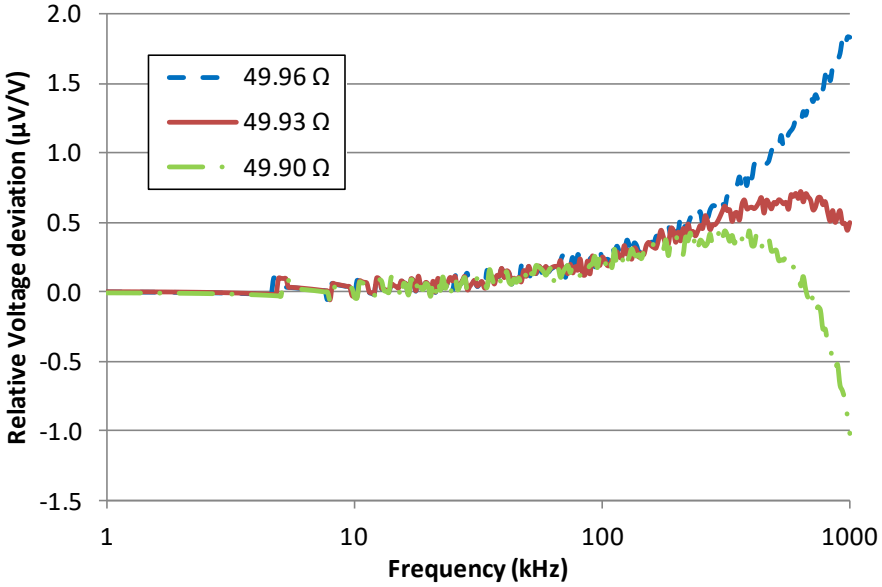

Figure 6. Residual error after correcting the influence caused by the input impedance of the DUT and transmission line losses.

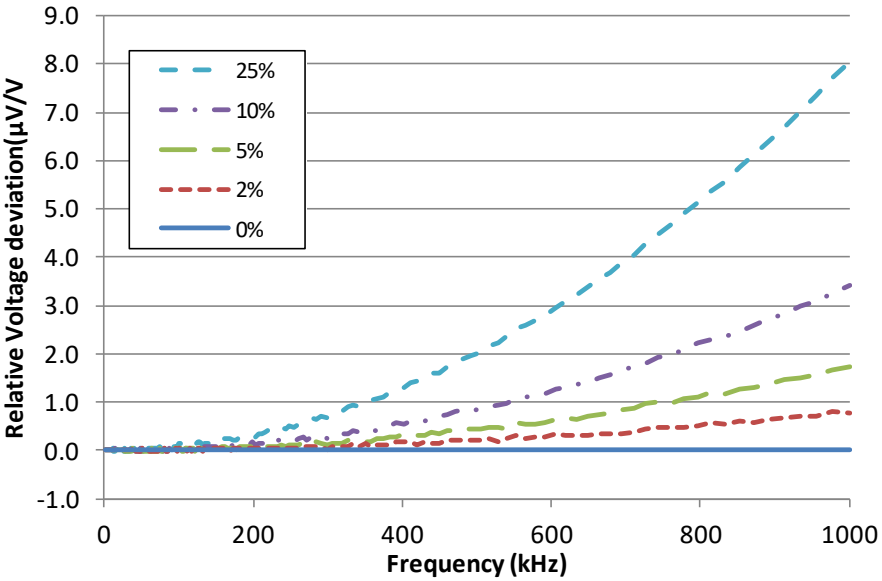

Figure 7. Relative voltage deviation caused by a 1 % change of the characteristic impedance in different fractions of the cable length.

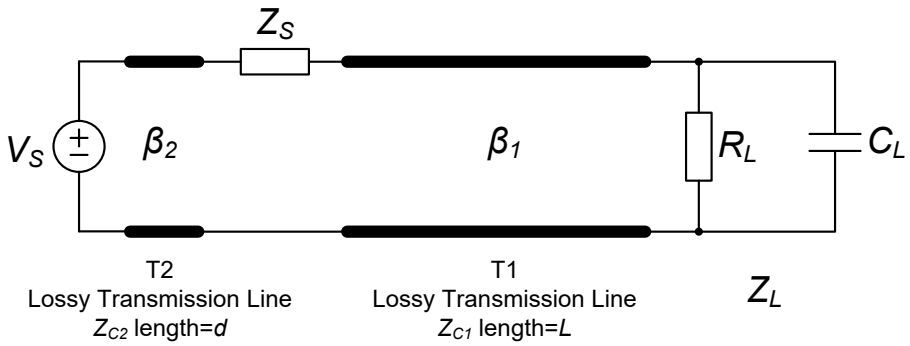

Figure 8. Transmission line model implemented in PSpice including the discontinuity on the ACJVS chip. The indices 1 and 2 used for cable parameters refer to the transmission lines T1 and T2, respectively.

of the 1.5 m coaxial cable immersed in the low temperature environment, causing a 1 % change of the characteristic impedance of this part of the line. This discontinuity is an approximation of the real situation in which a temperature gradient will occur inside the cable causing a more gradual change of characteristic impedance. From the calculation we find that the influence on the relative voltage deviation is around 3.5 ppm at 1 MHz and 0.04 ppm at 100 kHz. The calculations are also carried out for other fractions of the 1.5 m coaxial cable and the results are illustrated in figure 7.

Note that the 1 % change of the characteristic impedance is a rough estimate. First, the dielectric permittivity may change only very little when the cable is immersed in low temperature environment [14], such that the characteristic impedance is most likely more or less identical to the part at room temperature and this deviation is probably much smaller. Second, the other parameter that may be influenced is the diameter of the materials in the cable. The capacitance scales with the logarithm of the ratio of the inner and outer diameter, which should not change when they have the same thermal expansion coefficient. However, if the dielectric material contracts stronger than the surrounding metal when immersed in helium, a gap between metal and dielectric might occur influencing the characteristic impedance of the cable. In conclusion, the cable needs to be carefully selected and tested not only for its loss coefficient but also for its temperature behavior, or even to be specially developed for this application.

3.5. Characteristic impedance discontinuity on the ACJVS chip

The on-chip connection between the Josephson junction array and the transmission line is a strip line which normally has a characteristic impedance different from 50 Ω. The challenge is the finite length of the Josephson junction array itself and the on-chip inductors preventing the high-speed pulses (necessary to drive the Josephson junction array) to directly enter the voltage leads.

A typical setup uses 1.5 m coaxial cable with 3 cm connection between Josephson junction array and cable, including path length on the chip and the matching impedance. The influence of the discontinuity caused by the chip layout and the matching impedance is investigated by modeling the connection between Josephson junction array and coaxial voltage lead as a transmission line T2 of 100 Ω characteristic impedance, see figure 8.

Following the tuning procedure described as step 1 in Section 3.2, a 1 m long 50 Ω coaxial cable is inserted and the deviation at 1 MHz is monitored to determine the matching impedance. Then correction for the influence of the input impedance of the DUT in steps 2-4 of Section 3.2 is carried out. We find that the matching resistor is now in the range between 50.62 Ω and 50.70 Ω, resulting in a deviation of 60 ppm. Note that this depends on the length of the extra cable, for example using 1.5 m instead of 1 m long extra cable results in a smaller range between 50.58 Ω and 50.62 Ω and 62 ppm deviation. The deviation at 100 kHz in this case is 0.5 ppm, which is an enormous improvement with respect to earlier results [7], and

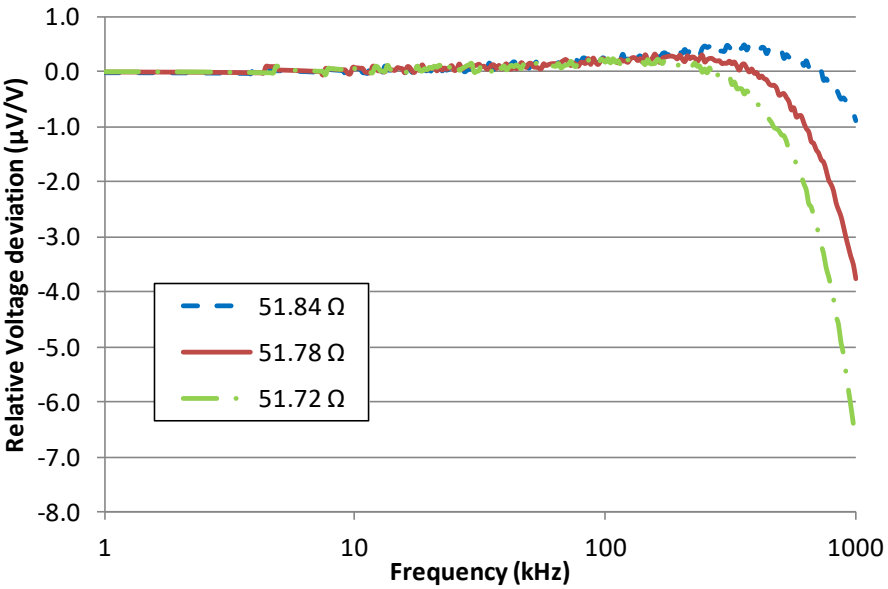

Figure 9. Residual error after correcting the influence caused by the input impedance of the DUT, transmission line losses and discontinuity in a realistic situation.

with respect to results obtained with conventional AC-DC transfer standards. The residual error of the influence at 10 kHz is below one part in 10^7 which is the noise floor of the simulation results.

If further improvement on these numbers is needed, one can perform the following adjustments in the procedure. In the tuning procedure described as step 1 in Section 3.2, the path length should be doubled, so the length of the extra cable should be equal to the apparent path length $L + Z_{C1}C_L v_1$, which is 2.02 m in this case. Now the matching resistor is found to be in the range between 50.52 Ω and 50.56 Ω. This matching resistor cannot be used directly in steps 2-4 of Section 3.2. The divergence of Z_S from Z_{C1} defined as $\frac{Z_S - Z_{C1}}{Z_{C1}}$ needs to be scaled by a factor of 3 (see Appendix A). Hence, for an apparent characteristic impedance of 49.92 Ω (due to the losses, also see figure 5), the matching resistor needs to be set to a value between 51.72 Ω and 51.84 Ω to compensate for the mismatch of the strip line. To perform the above adjustments one needs to know the value of the characteristic impedance of the transmission line T1 and the apparent cable length offset $\Delta L = Z_{C1}C_L v_1$. The characteristic impedance of the cable can be measured using a TDR (time-domain reflectometer) or a network analyzer. To obtain the apparent cable length offset ΔL, the inserted Z_S is removed first, then $V(L)$ is measured with different cable lengths. After that, the results are curve fitted using equation (4) to derive ΔL. After the correction for the influence of the input impedance of the DUT in steps 2-4 of Section 3.2, the final calculation results for this situation are presented in figure 9, showing that the influence of the discontinuity on the ACJVS chip will be reduced to 4 ppm at 1 MHz and 0.3 ppm at 100 kHz. The uncertainty related to finding the proper matching resistance is about 3 ppm for both inductance values (as can be seen in figure 9).

This remaining piece of cable might be improved upon by redesigning the chip with the Josephson junction array to have on-chip output leads that approach a 50 Ω strip line and integrating the matching impedance on-chip as well. This way the discontinuity is avoided as much as possible and the influence can possibly be reduced even further.

3.6. Non-zero Josephson junction array output impedance

So far, we assumed the output impedance of the Josephson junction array to be zero. However, in practice the ACJVS chip can have a total inductance as large as 125 nH [12] between the array and the transmission line, which includes the array intrinsic inductance of about 7 nH [4] and the on-chip inductors preventing the high-speed pulses to enter the voltage leads [15].

The influence of the on-chip inductance is investigated by inserting a 125 nH inductor between Josephson junction array and transmission line T2 in figure 8. Following the procedures described in Section 3.2, a 1.5 m long 50 Ω coaxial cable is inserted and the deviation at 1 MHz is monitored to determine the matching impedance. Now the matching resistor is found to be in the range between 55.52 Ω and 55.58 Ω. The deviation will be as large as 570 ppm at 1 MHz and 5.5 ppm at 100 kHz. If further improvement on these numbers is needed, a 2.02 m long 50 Ω coaxial cable is inserted as in Section 3.5 and the matching resistor is found to be in the range between 55.50 Ω and 55.54 Ω. The divergence of Z_S from Z_{C1} defined as $\frac{Z_S - Z_{C1}}{Z_{C1}}$ needs to be scaled by a factor of 3 as discussed in the previous section. Hence, for an apparent characteristic impedance of 49.92 Ω as before, the matching resistor needs to be set to a value between 66.66 Ω and 66.78 Ω to compensate for the mismatch of the strip line and the influence of the chip inductance. After the correction for the influence of the input impedance of the DUT in steps 2-4 of Section 3.2, the final calculation shows that the combined influence of the chip inductance and the discontinuity on the ACJVS chip will become 54 ppm at 1 MHz and 0.9 ppm at 100 kHz.

For a somewhat lower but still realistic total chip inductance of about 72 nH in parallel with a 300 Ω resistor [15] to damp the self-resonances we find that the matching resistor is in the range between 53.44 Ω and 53.48 Ω. After scaling by a factor of 3 we find that the matching resistor needs to be set to a value between 60.48 Ω and 60.60 Ω. The final calculation results for this situation are presented in figure 10, showing that the influence of the chip inductance in the presence of a discontinuity on the ACJVS chip will become 12 ppm at 1 MHz and 0.5 ppm at 100 kHz.

From the latter result we find that the final error strongly depends on the actual chip inductance. We conclude that the ACJVS chip should be designed with low enough inductance, though without deteriorating the operating margins of the ACJVS too much.

The uncertainty related to finding the proper matching resistance is about 4 ppm for both inductance values (as can be seen in figure 10 for the lower inductance). Furthermore, the residual error found in the simulations is a systematic error that can be corrected for. Calculations show that a 10 nH change of the inductance value changes this error by about 6 ppm at 1 MHz and 0.06 ppm at 100 kHz. In other words, assuming we can determine the actual on-chip inductance with an accuracy of 10 nH, the uncertainty of the error correction will be about 6 ppm at 1 MHz for a 3 cm connection between Josephson junction array and coaxial cable with 100 Ω characteristic impedance (as in Section 3.5).

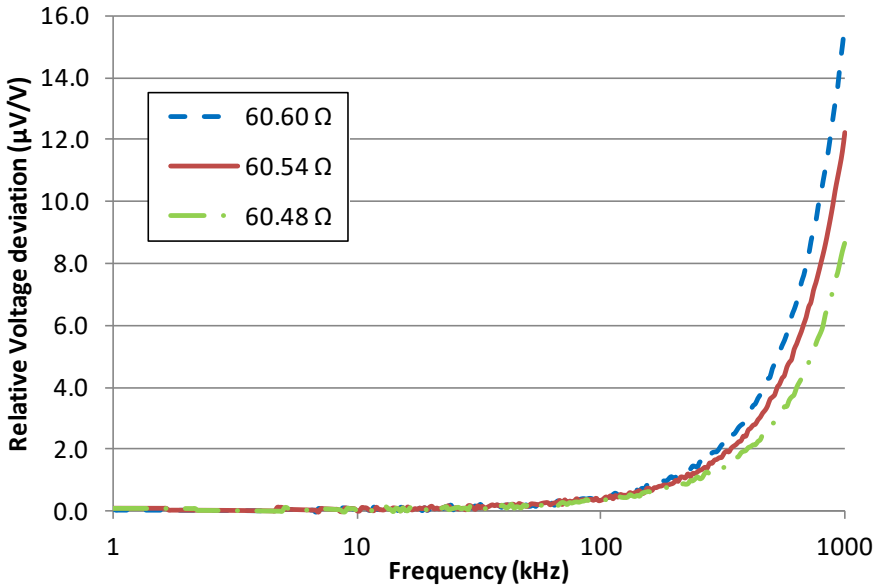

Figure 10. Residual error after correcting the influence caused by the input impedance of the DUT, transmission line losses and discontinuity and the influence of the chip inductance in a realistic situation.

3.7. The instability of the matching resistor

When the resistor is subsequently immersed in low temperature environment, aging will cause the resistance value to drift. Assuming a maximum variation of 0.2 % of the impedance value due to thermal cycling, calculations show that a 5 ppm deviation at 1 MHz and a 0.05 ppm deviation at 100 kHz will be introduced to the final voltage $V(L)$ measured at the end of a 1.5 m coaxial cable. This value is comparable to the 1 ppm change at 1 MHz with 0.02 Ω tolerance mentioned in Section 3.1 and does not seem to depend on the other imperfections discussed in Sections 3.2–3.5.

If remotely adjusting the resistance value at low temperatures would be possible, this would be a big advantage both for practical reasons and for the thermal aging problem. Implementing an on-chip fixed resistor of approximately 50 Ω with a second much smaller tuning resistor in series would be helpful in this case, since the allowed tolerance of the small tuning resistor (in terms of a percentage of its resistance value) would be much higher.

3.8. Frequency dependence of the components

The components in the models so far are frequency independent. This description is usually sufficient for frequencies between approximately 20 kHz and a few MHz. For frequencies above a few MHz, parasitic elements of the matching resistor need to be included. The first one is the lead inductance L_{lead} in series with the resistor model representing the inductance of the loop area bounded by the two leads. The second one is the parasitic capacitance C_{par} in parallel with the resistor representing the parallel combination of the lead and leakage capacitances. Typical values are L_{lead} = 14 nH and C_{par} = 2 pF [11], leading to a resonance at a frequency of approximately 950 MHz. Calculation shows that the impedance magnitude of the resistor changes by only 13 μΩ at 1 MHz and the influence on tuning results is negligible.

For frequencies below about 20 kHz, due to factors such as the local electromagnetic field distribution and the related skin effect and proximity effect, the characteristic impedance value of the cable is frequency dependent, and its value will also contain a reactive component. The value can be as high as (175.7 – j 165.8) Ω for a cable with characteristic impedance of 50 Ω at 1 kHz [16]. Since the matching resistor is tuned at 1 MHz, obviously at 1 kHz matching will not be achieved. However, the influence on the final measurement result is very small, since at low frequencies the error that needs to be mitigated is very small already. Through calculation, the influence of the non-perfect matching on the final result is found to be 0.002 ppm at 1 kHz and 0.1 ppm at 10 kHz, so that the model still works in this regime as well.

4. Summary and conclusion

The voltage lead errors observed before in pulse-driven ACJVS systems at frequencies above 10 kHz can be understood in terms of reflected waves. In this paper we propose to use impedance matching as an accurate method to mitigate these errors. An approach in which a series resistor matching the characteristic impedance of the cable is put as close as possible to the Josephson junction array seems to be promising. The influence of non-ideal characteristics of components, which include tolerance of the matching resistor, the capacitance of the load input impedance, losses and non-homogeneity in the voltage leads, a non-ideal on-chip connection and inductors between Josephson junction array and voltage leads, is discussed and evaluated by simulations.

From the results of these simulations, solutions for improvement with specific measurement procedures are proposed. Calculations show that after correction of the error caused by the on-chip inductors and cable mismatch as described in Section 3.6, the combined influence of the different uncertainty sources leads to a total uncertainty (k = 2) of 12 ppm at 1 MHz or 0.5 ppm at 100 kHz for AC/DC measurements with a F792A is within reach. Note that this result is dependent on the details of the experimental configuration. To obtain these uncertainties the procedures described in Sections 3.2 and 3.5 should be followed, in specific doubling the apparent path length and multiplying the divergence of Z_S from Z_{C1} by a factor

of 3. For users only interested in uncertainties of about 6 ppm at 100 kHz and for whom the lowest uncertainties at 1 MHz are not needed, following the procedure described in Section 3.2 only is sufficient. The stability of 0.2 % for the matching impedance could be obtained by using a fixed (on-chip) resistor of approximately 50 Ω in combination with a much smaller tuning resistor having a much higher allowed tolerance.

The ACJVS on-chip inductors and the cable discontinuity caused by the connection to the Josephson junction array seem to be the largest source of uncertainty. It is proposed to redesign the chip to reduce the on-chip inductance and to have on-chip output leads that approach a 50 Ω strip line and if possible to integrate the matching impedance on-chip as well.

It should be noted that the method proposed in this paper only works for devices under test with high input impedance, such as for the lower ranges of the F792A. For input impedance values of 1 MΩ for example, the method is already less effective and results in higher uncertainties. Thermal converters, which are used at the highest level of accuracy in calibration laboratories, usually have even much lower input impedance. Fur such devices an ACJVS cannot be used directly because it should provide a considerable amount of current.

In conclusion, the results obtained using the method proposed in this paper based on impedance matching suggest that the operating frequency range of ACJVS systems can be extended to 1 MHz with very low uncertainties. Furthermore, the uncertainty at 100 kHz and below can be improved by an order of magnitude as compared to previous work [7]. Future work needs to concentrate on the experimental implementation of the method.

Appendix A

In section 3.5, a final improvement to compensate for the discontinuity caused by the strip line on the chip was introduced. When tuning the matching resistor by adding an extra cable and monitoring the reading of the DUT it was proposed to double the apparent path length $L + Z_{C1}C_L v_1$. After the tuning procedure, the value of the matching resistor Z_S is adjusted such that the divergence of from the characteristic impedance of the cable Z_{C1}, defined as $\frac{Z_S - Z_{C1}}{Z_{C1}}$, is scaled by a factor 3. This factor of 3 is explained below.

The input impedance of a typical DUT is modeled as a resistor R_L in parallel with a capacitor C_L. The simplified circuit diagram is shown in figure A1. First, the input impedance of the transmission line T1 terminated with the load Z_L can be written as [11]

$$Z_{\text{in}} = Z_{C1}\frac{Z_L + jZ_{C1}\tan(\beta_1 L)}{Z_{C1} + jZ_L\tan(\beta_1 L)} \approx -\frac{Z_{C1}}{\beta_1(L + Z_{C1}C_L v_1)}j \tag{A.1}$$

where the approximation is valid for wavelengths $\lambda \gg L$ and for $Z_L \gg Z_{C1}$, and it is now treated as purely capacitive; the resistive part will be treated separately below, just as in equations (6) and (7). The reflection coefficient at the output of the transmission line T2 can be expressed as

$$\Gamma_{L2} = \frac{(Z_{\text{in}} + Z_S) - Z_{C2}}{(Z_{\text{in}} + Z_S) + Z_{C2}} \approx 1 - 2\left(\frac{Z_{C2}\beta_1(L + Z_{C1}C_L v_1)}{Z_{C1}}\right)j \tag{A.2}$$

Thus, the ratio between the voltage V_2 at the end of the on-chip voltage leads and the source voltage V_S becomes

$$\left|\frac{V_2}{V_S}\right| = \left|\frac{1 + \Gamma_{L2}}{1 + \Gamma_{L2}\exp(-j2\beta_2 d)}\right| \approx 1 + \frac{Z_{C2}\beta_1\beta_2 d(L + Z_{C1}C_L v_1)}{Z_{C1}} \tag{A.3}$$

The ratio between the load voltage V_1 and V_2 is

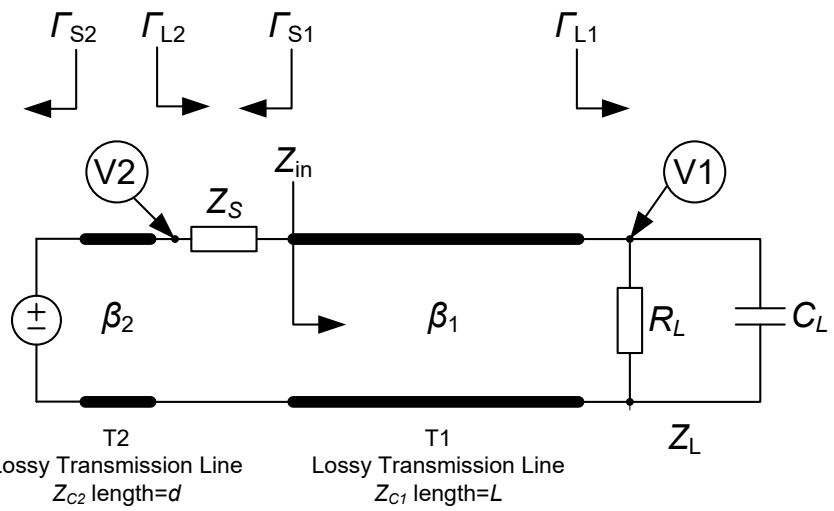

Figure A1. Transmission line model implemented in PSpice including the discontinuity on the ACJVS chip.

$$\left|\frac{V_1}{V_2}\right| = \left|\frac{1+\Gamma_{L1}}{1+\Gamma_{S1}\Gamma_{L1}\exp(-j2\beta_1 L)}\frac{Z_{C1}}{Z_{C1}+Z_S}\right| \approx 1 - \frac{(\omega C_L Z_{C1})^2}{2} - r(\omega C_L Z_{C1} + \beta_1 L)^2 \tag{A.4}$$

where $r = \dfrac{Z_S - Z_{C1}}{Z_{C1}}$.

Combining equation (A.3) and equation (A.4), the voltage at the DUT can be written as

$$|V_1| \approx \left(1 + \frac{Z_{C2}\beta_1\beta_2 d(L + Z_{C1}C_L v_1)}{Z_{C1}} - \frac{(\omega C_L Z_{C1})^2}{2} - r(\omega C_L Z_{C1} + \beta_1 L)^2\right)|V_S| \tag{A.5}$$

In step 1, now an extra cable with length $L + Z_{C1}C_L v_1$ is inserted. Tuning Z_S until $|V_1|$ does not change means that equation (A.5) should give the same result with or without adding the extra cable. This extra cable with no change in output voltage leads to the following condition:

$$\begin{aligned}\frac{Z_{c2}\beta_1\beta_2 d(L + Z_{C1}C_L v_1)}{Z_{c1}} &= r\left((\omega C_L Z_{C1} + \beta_1(L + L + Z_{C1}C_L v_1))^2 - (\omega C_L Z_{C1} + \beta_1 L)^2\right) \\ &= 3r(\omega C_L Z_{C1} + \beta_1 L)^2\end{aligned} \tag{A.6}$$

Now *another* matching resistor with deviation $3r$ is used. Using the condition in equation (A.6), equation (A.5) leads to

$$\begin{aligned}|V_1| &\approx \left(1 + \frac{Z_{c2}\beta_1\beta_2 d(L + Z_{C1}C_L v_1)}{Z_{c1}} - \frac{(\omega C_L Z_{C1})^2}{2} - 3r(\omega C_L Z_{C1} + \beta_1 L)^2\right)|V_s| \\ &= \left(1 - \frac{(\omega C_L Z_{C1})^2}{2}\right)|V_s|\end{aligned} \tag{A.7}$$

As can be seen here, after introducing a resistive ratio factor to cover the DC and low frequency regime the same equations as in Section 3.2 are recovered.

In conclusion, inserting a resistor with a 3 times larger deviation from the characteristic impedance as compared to the value obtained from the original tuning procedure causes several terms to be cancelled, which leads to the same expressions as obtained before in

Section 3.2 without cable discontinuity due to the on-chip connections. The remarkable result is that this factor of 3 neither depends on the characteristic impedance of the on-chip voltage leads, nor on their length, as long as it is short compared to the main voltage leads in the probe.

Acknowledgment
This work is carried out with funding by the European Union within the EMRP JRP SIB59 Q-WAVE and EMPIR JRP 15SIB04 QuADC. The EMRP and EMPIR are jointly funded by the EMRP participating countries within EURAMET and the European Union. We would like to thank J.M. Williams (NPL) for valuable discussions on understanding the observed ACJVS voltage lead errors in terms of reflected waves and T. Bergsten (SP) for pointing out the relation between cable length offset and input capacitance.

References

[1] Benz S P and Hamilton C A, 1996 A pulse-driven Programmable Josephson voltage standard, *Appl. Phys. Lett.* 68 3171 – 3
[2] Kieler O F, Behr R, Wendisch R, Bauer S, Palafox L, and Kohlmann J 2015 Towards a 1 V Josephson arbitrary waveform synthesizer, *IEEE Trans. Appl. Supercond*. 25 1400305
[3] Flowers-Jacobs N E, Fox A E, Dresselhaus P D, Schwall R E, and Benz S P 2016 Two-Volt Josephson Arbitrary Waveform Synthesizer Using Wilkinson Dividers, *IEEE Trans. Appl. Supercond*. 26 1400207
[4] van den Brom H E and Houtzager E 2012 Voltage lead corrections for a pulse-driven ac Josephson voltage standard *Meas. Sci. Technol.* 23 124007
[5] Lipe T E, Kinard J R, Tang Y H, Benz S P, Burrroughs C J, and Dresselhaus P D 2008 Thermal voltage converter calibrations using a quantum AC standard *Metrologia* 45 275 – 80
[6] Filipski P S, Boecker M, Benz S P and Burroughs C J 2011 Experimental determination of the voltage lead error in an ac Josephson voltage standard *IEEE Trans. Instrum. Meas.* 60 2387 – 92
[7] Filipski P S, van den Brom H E, and Houtzager E 2012 International comparison of quantum AC voltage standards for frequencies up to 100 kHz *Measurement* 45 2218 – 25
[8] van den Brom H E, Zhao D, and Houtzager E 2016 Voltage Lead Errors in an AC Josephson Voltage Standard: Explanation in Terms of Standing Waves *Proc. Conf. on Precision Electromagnetic Measurements* CPEM 2016
[9] van den Brom H E, Kieler O F, Bauer S, and Houtzager E, AC-DC Calibrations With a Pulse-driven AC Josephson Voltage Standard Operated in a Small Cryostat *IEEE Trans. Instrum. Meas.* 66 1391 – 6
[10] Straw R D 1998 *The ARRL antenna book* American Radio Relay League
[11] Paul C R 2006 *Introduction to Electromagnetic Compatibility* John Wiley & Sons
[12] Filipski P S, Kinard J R, Lipe T E, Tang Y H, and Benz S P 2009 Correction of systematic errors due to the voltage leads in an ac Josephson voltage standard *IEEE Trans. Instrum. Meas.* 58 853-8
[13] Pasternack 2017 LMR-500 Flexible Low Loss Communications Coax, See https://www.pasternack.com/images/ProductPDF/LMR-500.pdf
[14] Perepechko I 2013 *Low-temperature properties of polymers* Elsevier
[15] Watanabe M, Dresselhaus P D, and Benz S P 2006 *Resonance-free lowpass filters for the AC Josephson voltage standard* IEEE Trans. Appl. Supercond. 16 49–52
[16] Gallant M I, *Coaxial Cable Calculator* see http://www.jensign.com/CoaxCalc/index.html