D1.3

Integration specifications

Project number:	779305
Project acronym:	SERENA
Project title:	gan-on-Silicon Efficient mm-wave euRopean systEm iNtegration plAtform
Start date of the project:	1st January, 2018
Duration:	36 months
Programme:	H2020-ICT-2017-1

Deliverable type:	Report
Deliverable reference number:	ICT-31-779305 / D1.3/ 1.0
Work package contributing to the deliverable:	WP1
Due date:	Jun 2018 – M06
Actual submission date:	2nd July, 2018

Responsible organisation:	Fraunhofer
Editor:	Ivan Ndip
Dissemination level:	PU
Revision:	1.0

Abstract:	5G mmWave packaging requirements are given, and the specifications of the packaging platform proposed in SERENA to meet these requirements are presented. The platform is specified to meet the performance, reliability, size and cost requirements.
Keywords:	PCB embedding packaging platform, 5G mmWave, 39 GHz band, antennas, RF, thermal, reliability, cost

The project SERENA has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 779305.

Editor

Ivan Ndip (Fraunhofer)

Contributors (ordered according to beneficiary numbers)

Kristoffer Andersson (EAB)

Franz Dielacher, (IFAT)

Yannis Papananos, (IFAT)

Ivan Ndip (FHG)

Jacob Reyes (FHG)

Christian Tschoban (FHG)

Uwe Maaß (FHG)

Andreas Ostmann (FHG)

Stefan Kosmider (FHG)

Reviewer

Kristoffer Andersson (EAB)

Rémy Leblanc (OMMIC)

Executive Summary

Electronic packaging plays a key role in the development of hardware modules for future 5G systems. In this report, the requirements of packaging platforms to be used for system-integration of 5G RF transceivers and antennas are given. The specifications of the PCB-embedding packaging platform proposed in SERENA to meet these requirements are presented. The PCB-embedding packaging platform to be designed, fabricated and demonstrated in SERENA will enable the development of miniaturized, high-performance, reliable and low-cost mmWave wireless systems, especially for future 5G wireless communication and radar sensor applications.

Contents

List of Figures

List of Tables

Chapter 1 5G mmWave Packaging Requirements

3GPP recently defined new mmWave frequency bands for future 5G mobile communication applications. One of these bands is the 39 GHz band. This band provides enormous bandwidth, unparalleled with the bandwidth available in the sub 6 GHz band currently used for 4G systems. In addition to enabling more bandwidth, the 39 GHz band also enables a higher degree of system miniaturization because most system components scale with the wavelength.

However, mobile communication at mmWave frequencies is extremely challenging, particularly because of propagation issues such as severe path loss, multipath fading and shadowing. To overcome these challenges, very high gain antennas and efficient RF transceiver components which enable the implementation of new MIMO and beam-forming schemes must be used. In order to develop 5G mmWave systems, these antennas and transceiver components must be integrated together using an advanced packaging platform. Since this platform plays a crucial role in system development, it must meet some key requirements which ensure high-performance, reliability, miniaturization and cost-effectiveness of the 5G mmWave hardware system.

In this chapter, a brief summary of some of the fundamental requirements that must be met by packaging platforms used for 5G mmWave applications are given. These requirements are adapted from [1].

1.1 Integration of High Gain Antennas

Free space losses at the 39 GHz band are extremely large, in comparison to losses at frequencies used by mobile communication systems today. These losses degrade the signal-to-noise ratio (SNR), and may lead to a reduction in the channel capacity of 5G mmWave systems. High gain antennas are key components of 5G systems, because they play a significant role in overcoming free space and atmospheric losses, and thus make mobile communication possible at mmWave frequencies. The gain of an antenna varies proportionally with its directivity and efficiency. The dielectric material and metallization used for antenna integration determines the dielectric and conduction efficiencies of the antenna.

Therefore, the packaging platform used for the integration of 5G mmWave antennas must provide the flexibility of choosing dielectric material and metallization which yield high dielectric and conduction efficiencies of the antenna, so as to ensure high gain.

1.2 Signal Integrity

Signal integrity (SI) problems (e.g., reflection, attenuation, cross-talk) caused by packaging interconnects between the front-end chips and the antenna **(chip-to-antenna SI)** have significant effects on the antenna gain and the EIRP (Equivalent Isotropically Radiated Power) of the entire system. Reflections along these interconnects cause a reduction of the mismatch efficiency of the antenna, and thus lead to a deterioration of the antenna gain. Furthermore, these reflections may severely degrade the performance of the power amplifier. Attenuation along these interconnects cause losses in the signal power and thus leads to a reduction in the EIRP of the entire system.

In most cases (e.g., in SERENA), the building blocks of an RF front-end are not monolithically integrated. They are realized as discrete chips which are then interconnected using electronic packaging interconnects. SI issues along interconnects between these chips (i.e., **chip-to-chip SI**) may severely degrade the functionality of the entire RF transceiver. Lastly, SI issues along packaging

interconnects between RF front-end chips and components required, for example, for analogue beamforming (**chip-to-component SI**), may also deteriorate the performance of the entire system.

To ensure chip-to-antenna SI, chip-to-chip SI and chip-to-component SI, the packaging platform must provide short and low-loss interconnect paths with few geometrical discontinuities between the chip and antenna, between the building blocks of the front-end and between the chips and other integrated components

1.3 Power Integrity

The 39 GHz RF front-end chips can only function if they are supplied with the required voltages and currents. To ensure stable power supply to, and proper functioning of, the RF front-end chips, the packaging platform used for future mmWave 5G systems must ensure the following:

- Integration of capacitors in close proximity to the RF front-end chips.
- Provide low inductive interconnect paths between the capacitors and chips, thereby minimizing the possibilities of power integrity problems such as simultaneous switching noise (SSN).

1.4 Intra-System Electromagnetic Compatibility (EMC)

Undesired electromagnetic interaction between the antennas integrated in a packaging platform and other integrated components (e.g., RF front-end ICs, signal lines) has significant effects on the performance of antennas, the components and the entire 5G system. During such an interaction, electromagnetic power to be radiated by the antenna couples into the components, and causes a reduction in the antenna gain as well as deformation of its radiation pattern. Current and voltages induced by the antenna may cause EMI issues on the components and thus lead to system malfunctioning or even failure.

Therefore, the packaging platform used for the integration of 5G antennas must provide adequate shielding between the antennas and other integrated components.

1.5 Reliability

To implement the mmWave massive MIMO and hybrid digital-analogue beamforming techniques for 5G systems, multiple power amplifiers are required in the RF front-end. Since most of these amplifiers have low power added efficiencies (PAE), they dissipate much power, which must be conducted out of the chip to prevent thermo-mechanical reliability issues.

Therefore, the packaging platform must provide a good thermal path for the conduction of heat from the chip either directly to the heatsink or through the system-board and then to the heatsink.

1.6 Miniaturization, Scalability & Cost

In traditional “interposer”-based packaging platforms, chip interconnection methods (e.g., flip chip interconnects, bond wires), are used to assemble the chips onto interposers, which could be made up of silicon, glass or organic materials. These interposers are then mounted on a carrier, which is then attached to the system-board using BGA balls or other interconnect technologies. However, these interposers increase the size and cost of the entire system. To reduce system cost and ensure a high degree of miniaturization, the platform must apply a packaging architecture which does not use an interposer. Examples of such platforms are the die-embedding platforms in polymer, silicon and PCB.

Another way to reduce cost is to ensure scalability. The packaging platform must enable the integration of the RF front-end ICs, including beam-forming components and antennas to form a basic module e.g., with 1X2 or 2X2 arrays. Such a module forms the fundamental building block of a 5G mmWave system, which can be extended to form larger modules and systems to address different power requirements. This reduces the manufacturing cost tremendously, because this basic module must not always be designed from scratch.

Chapter 2 Specifications of SERENA Packaging Platform to meet 5G mmWave Requirements

In [2] a comparative analysis of packaging platforms in published literature that can be used for the integration of 39 GHz 5G RF front-end components and antennas is presented. Based on the results of this analysis, the die-embedding packaging architecture, based on low-cost printed circuit board (PCB) materials was proposed to be designed, fabricated and demonstrated in the SERENA project. Figure 1 shows an example of such a platform that will be investigated in this project.

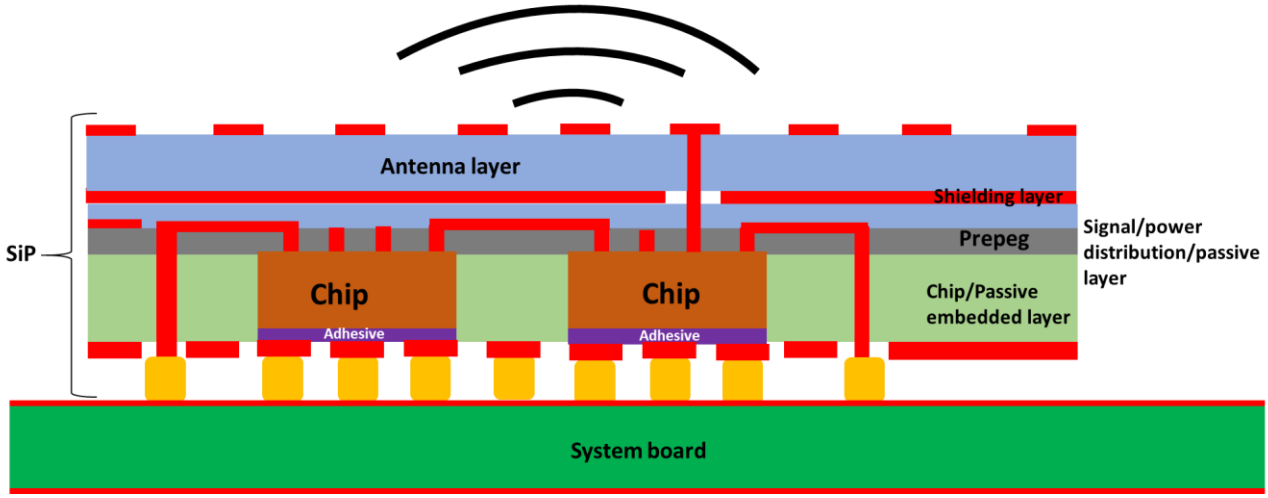


Figure 1: Schematic representation of an example of PCB-embedding-based system-integration platform [Deutsche Patentanmeldung Nr. 102017200127.5].

It comprises of an antenna layer (with integrated shielding), a chip/passive embedding layer, the routing layer for signal and power distribution, and optionally a thermal layer, not shown in figure 1. The antenna layer could be interconnected with the chip/passive embedding layer using vertical interconnects. Such interconnects could also be used for interconnecting the platform onto the system-board.

In this chapter, the specifications of this platform defined so far in the project, so as to meet the 5G packaging requirements given in the previous chapter are given. The different layers which form the building block of this platform as well as the interfaces between the layers will be separately discussed.

2.1 Antenna Layer

The antenna layer is chosen to enable the integration of a planar antenna array configuration with spacing of approximately half the wavelength at 39 GHz. As can be seen in figure 2, the arrays are vertically fed, and power dividers are used to distribute power to the patch elements.

To meet the low-cost requirements, FR4 is chosen as the dielectric material to be used in the antenna layer. It has relative dielectric constant of around 4.8 and loss tangent of around 0.01.

However, as a result of the lossy nature of the FR4 substrate, a second PCB-based substrate material has been chosen, as an alternative. This material is Megtron 7N. It has a relative dielectric constant of 3.3 and loss tangent of $4 \bullet 10^{-3}$.

In order to achieve the bandwidth requirements, the antenna layer is specified to have a dielectric thickness of at least 300 µm. The metal layers are specified to have thicknesses, which vary between 17 µm and 35 µm.

To meet the intra-system EMC requirements, the antenna layer is specified to have a backside metallization, which shields the stray fields of the antenna from interacting with other integrated components.

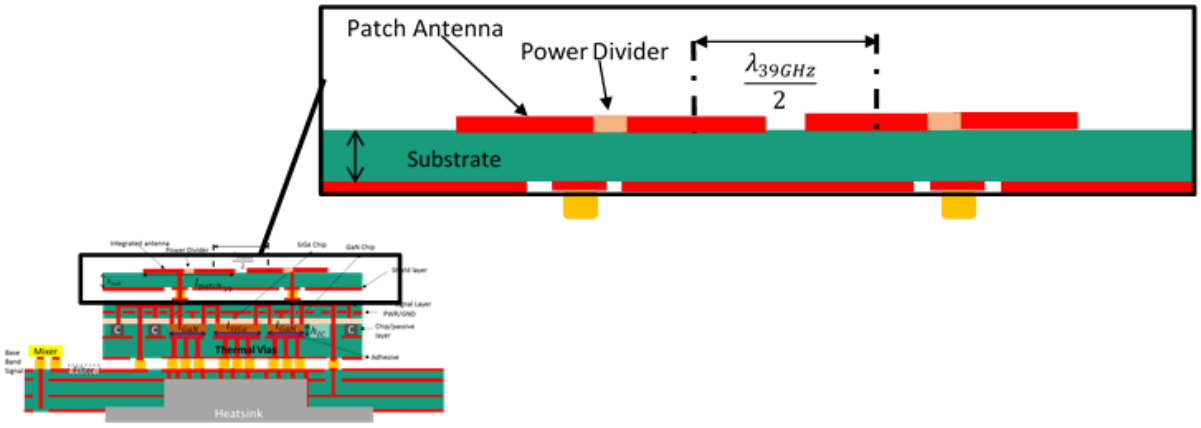


Figure 2: Example of antenna layer in the packaging platform.

2.2 Chip Embedding/Passive Integration Layer

This layer will also be fabricated using both FR4 and Megtron 7N substrates, so as to meet the cost/performance requirements. The thickness of the layer will vary from 100 µm to 350 µm. Depending on the final dimensions of the beamforming chip, T/R module and capacitors to be integrated, this layer could be made up of multiple dielectric and metallization layers. The minimum line/space specifications for this layer are 100 µm.

The chip-embedding/passive integration layer will be designed to ensure a very short thermal path to the heat sink.

Table 1 shows an example of some key parameters of this layer as well as the specified number of components.

Parameter	Unit	Value	Comment
Min. line / space	[um]	100	
Die / component height	[um]	100	
Package size (length X width)	[mm]	15,6 x 7,8	
Number of packaged ICs		5	ICs (+decoupling capacitors)
Interface		Soldered/ sintered	BGA or LGA
Preferred IC pad metallization		Cu	10um thickness

Table 1: Geometrical and package specifications

2.3 Routing Layer

This is the layer directly above the chip embedding/passive integration layer. It plays the key role of interconnecting the chips, the capacitors, the T/R module and the antenna. To meet the signal integrity and power requirements, this layer must enable very short paths with few geometrical discontinuities between these components. To prevent degradation of the antenna gain, this layer must ensure a minimization of signal reflections in the path which link the antenna and the amplifiers. The minimum line / space allowed in this layer is 100 µm and metallization thickness range from 17 µm to 35 µm.

2.4 Interfaces

The interfaces between the antenna and the routing layer as well as between the entire packaging platform and the system-board are the bottleneck of the performance of the entire system. These interfaces may degrade chip-to-antenna SI and component-to-component SI beyond acceptable limits.

One possibility currently being discussed in the project to minimize/prevent chip-to-antenna SI problems is to apply an “all integrated” solution as shown in figure 1, where the antenna is integrated directly on the routing layer. Since the interconnection path from the routing layer to the antenna layer is very short, chip-to-antenna SI is guaranteed. Alternative approaches also discussed in the project include the use of interconnects e.g., solder balls to attach the antenna layer onto the routing layer. Such interconnects will also be used for mounting the packaging platform onto the system-board.

Two possibilities have been identified for the solderable/sinterable interfaces: ball grid array (BGA) and fine-pitch land grid array (FLGA). The general specifications of these based on JEDEC standards are outlined in the Appendix.

2.5 System Board

The system board has different requirements based on the electrical parameters of the demonstrator (see D1.1) and the requirements of the thermal management of the R front-end. Based on this functionality the integration specifications for the system board were derived. For a general overview over the system board figure 3 depicts an example of a cross section.

Parameter	Min. [um]	Typ. [um]	Max. [um]	Remark
t_{M1-3}	3	18		s_{trace} 20um/50um respective
t_{Core1}		750		
$t_{Core2-4}$		100		Other thickness possible
$t_{cu\ core}$		1000		Other thickness possible

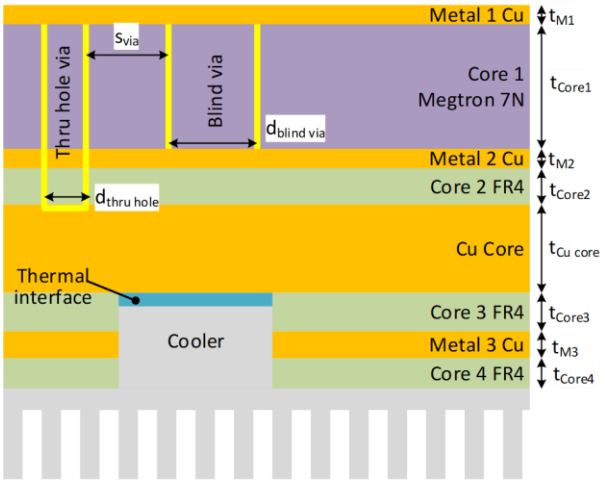
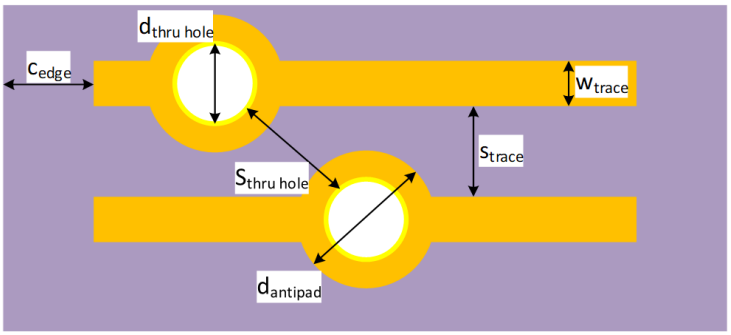


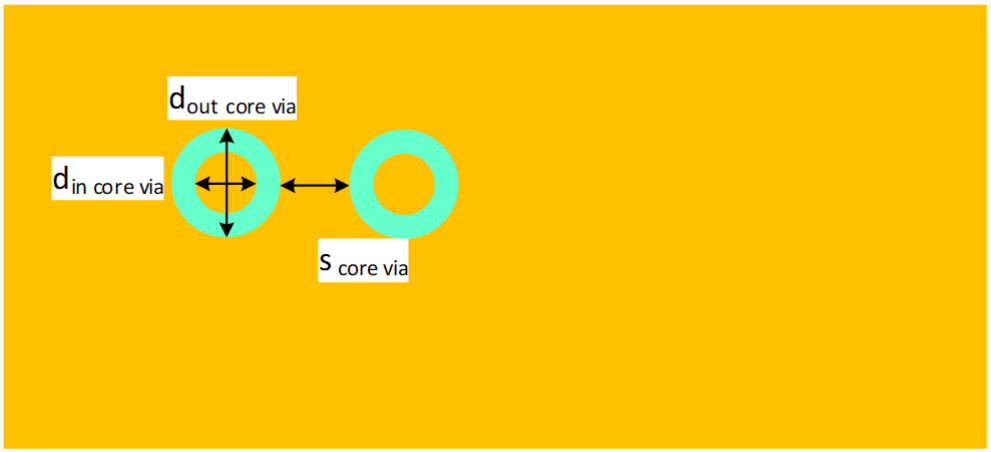
Figure 3: Cross section and parameters for the stack up of an example of a system-board.

In the top area, the substrate thickness is specified based on the requirements of the integrated filter structure. Initial investigations have shown that to fulfil the filter specifications based on a transmission line design a substrate thickness of 750 µm, a substrate with good high frequency electrical performance (small dielectric loss factor < 0.005) and line/space dimensions of 50/50 µm are required. Below the RF-material a copper core is needed as heat spreader. The copper core must be connected via a thermal interface with the system's heat sink. All RF-signal will be routed in the top layer on the RF material and all digital signals in lower layers in low cost standard FR4 material. The via geometries for different via types (through-hole via, blind via; copper core via) are presented in figure 4 to figure 4. In the digital area the line/space dimensions are larger than 75 µm.



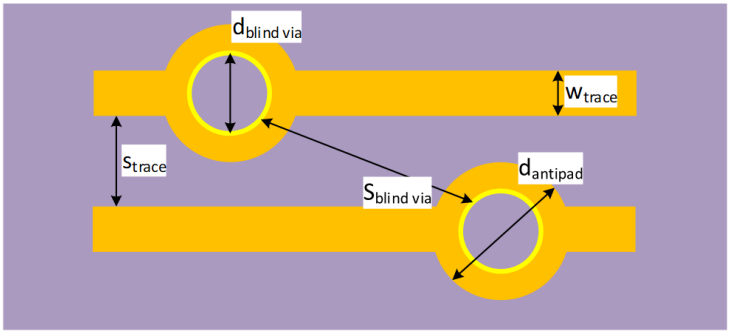
Parameter	Min. [um]	Remark
$d_{thru\ hole}$	150	aspect ratio *height:diam*=1:8
$d_{anti\ pad}$	+180	outer layers, + 300um else
c_{edge}	?	
$s_{thru\ hole}$	?	
w_{trace}	50	depends on Cu thickness
s_{trace}	50	depends on Cu thickness

Figure 4: Sketch of through-hole vias (top view) with design rules



Parameter	Typ. [um]
$d_{out\ core\ via}$	1000
$d_{in\ core\ via}$	200
$s_{core\ via}$	500

Figure 5: Sketch of copper core vias (top view) with design rules



Parameter	Min. [um]	Remark
$d_{blind\ via\ hole}$	60	aspect ratio *height:diam*=1:1
$d_{anti\ pad}$	+100	
c_{edge}	?	
$s_{thru\ hole}$	?	other thickness possible
w_{trace}	50	depends on Cu thickness
s_{trace}	50	depends on Cu thickness

Figure 6: Sketch of blind vias /top vew) with design rules

Chapter 3 Summary and Conclusion

The deliverable contains the specifications of the integration platform to be developed in the project to meet the demands of high gain antennas, signal integrity and power integrity, intra-system EMC as well as reliability and miniaturization issues. The technology for the realization of the integration platform is based on advanced PCB processes. The integration platform was conceptually separated into functional blocks for antenna, chip and passive component embedding and routing each having their own set of specifications. In addition to the RF front-end package the integration platform will incorporate a system-board with a defined interface to the package.

The specifications include the geometrical parameters to be met in the development of the technology for the integration platform and the choice of materials to be used in the research tasks.

Appendix

Ball Grid Array (BGA): JEDEC publication 95 (JEP95), February 2018, Item: 11.2-945

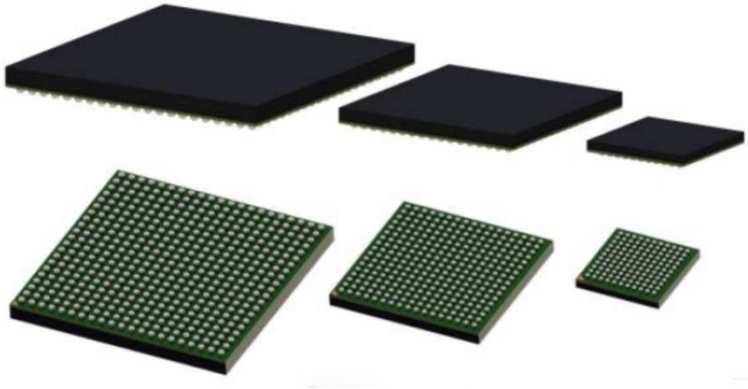


Figure 7: BGA package examples from JEDEC publication 95 (JEP95), February 2018, Item: 11.2-945

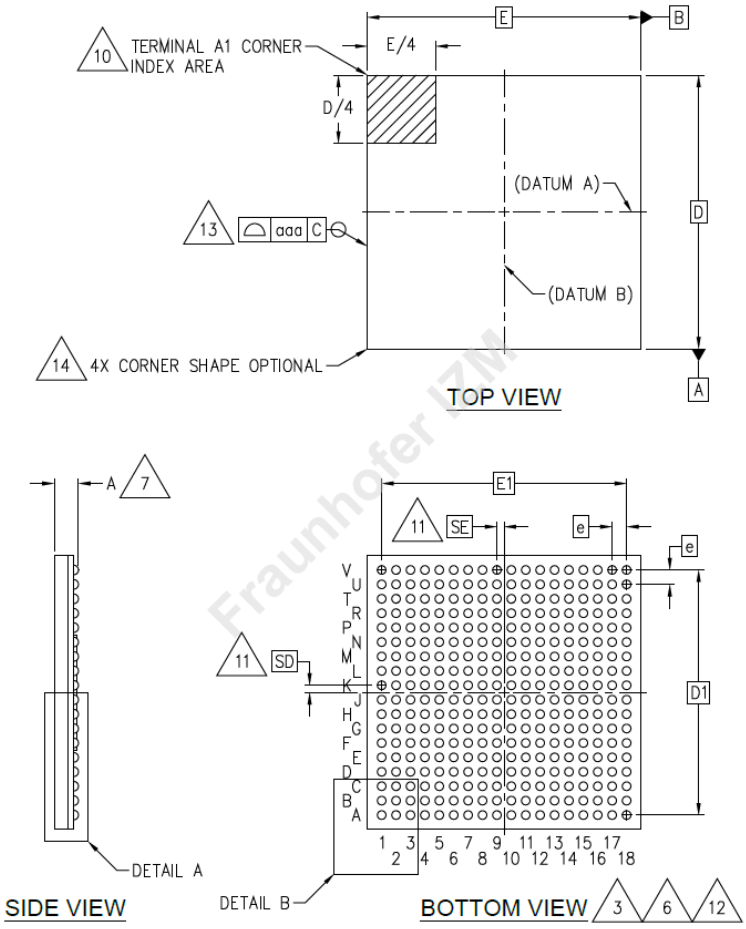


Figure 8: Definition of interface dimension definition from JEDEC publication 95 (JEP95), February 2018, Item: 11.2-945

BGA diameters: The BGA diameters that can be used depend on the pitch between the BGAs. There is a maximum BGA diameter and minimum BGA diameter defined for each pitch.

BGA Pitch [mm]	BGA Diameter [mm]		
	Min	Nom	Max
0.80	0.45	0.50	0.55
	0.40	0.45	0.50
	0.35	0.40	0.45
	0.30	0.35	0.40
	0.25	0.30	0.35
0.75	0.45	0.50	0.55
	0.40	0.45	0.50
	0.35	0.40	0.45
	0.30	0.35	0.40
	0.25	0.30	0.35
0.65	0.40	0.45	0.50
	0.35	0.40	0.45
	0.30	0.35	0.40
	0.25	0.30	0.35
0.50	0.25	0.30	0.35
	0.20	0.25	0.30
0.40	0.20	0.25	0.30
	0.15	0.20	0.25

Table 2: BGA diameters as function of BGA pitch

Maximum number of BGA contacts: The maximum number of BGAs for the package depends on the BGA pitch and the package dimensions. For a package size of 15.6mm x 7.8mm this translates to the following maximum number of BGAs as function of BGA pitch.

BGA pitch [mm]	Maximum number of BGAs
0.80	168
0.75	198
0.65	260
0.50	420
0.40	629

Table 3: Maximum number of BGAs for given package size as function of BGA pitch

Diameter of landing pad on substrate as function of BGA diameter: Both on the package and the system board, a solderable substrate surface will need to be provided for each position where a BGA interconnection will be placed. There are two possibilities to define the diameter of this substrate surface depending on how the solder resist is designed.

Type 1: The diameter of the solderable substrate surface is defined by an opening in the solder resist as shown in Figure 9.

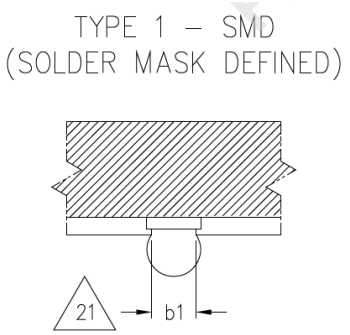


Figure 9: Type 1 diameter of solderable substrate surface definition from JEDEC publication 95 (JEP95), February 2018, Item: 11.2-945

Type 2: The diameter of the solderable substrate surface is defined by the pad size as shown in Figure 10.

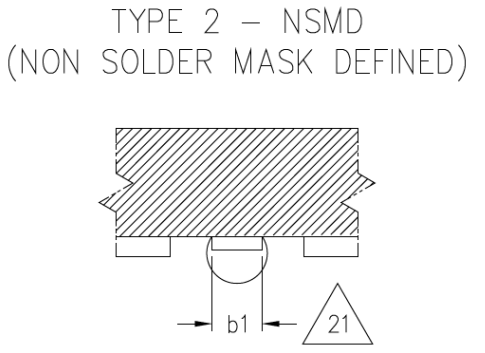


Figure 10: Type 2 diameter of solderable substrate surface definition from JEDEC publication 95 (JEP95), February 2018, Item: 11.2-945

BGA diameter (nom) [mm]	Minimum diameter solderable substrate surface type 1 [mm]	Minimum diameter solderable substrate surface type 2 [mm]
0.50	0.35	0.35
0.45	0.30	0.30
0.40	0.30	0.30
0.35	0.25	0.25
0.30	0.20	0.20
0.25	0.17	0.17
0.20	0.14	0.14

Table 4: Minimum diameter of solderable substrate surface as function of BGA diameter

Land Grid Array (BGA): JEDEC publication 95, Design guide 4.25, February 2016, Item: 11.2-896S

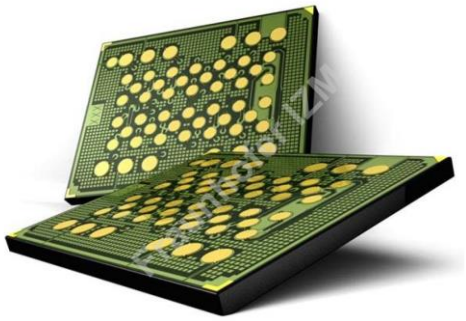


Figure 11: Example for LGA package interface from JEDEC publication 95, Design guide 4.25, February 2016, Item: 11.2-896S

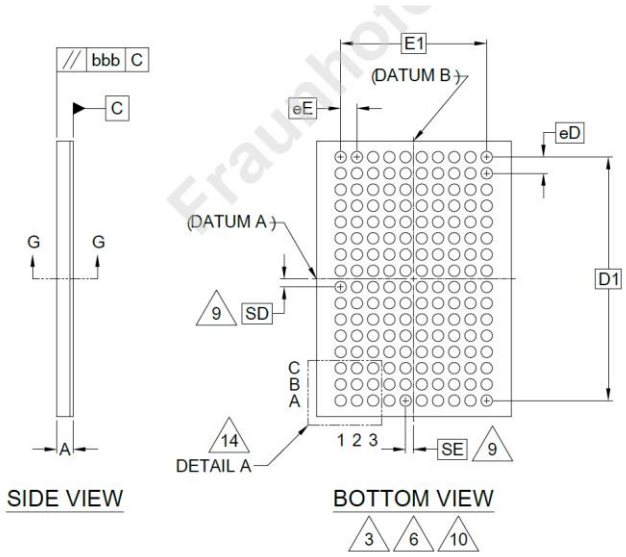


Figure 12: Interface dimensions definitions for sawn-type fine-pitch land grid array (FLGA) package from JEDEC publication 95, Design guide 4.25, February 2016, Item: 11.2-896S

Diameter of solderable substrate surface: There are two ways to define the solderable substrate surface for an LGA interface.

Type 1: The solder resist opening defines the diameter of the solderable substrate surface as illustrated in Figure 13. A minimum of 0.15 mm of solder resist needs to be kept between adjacent lands.

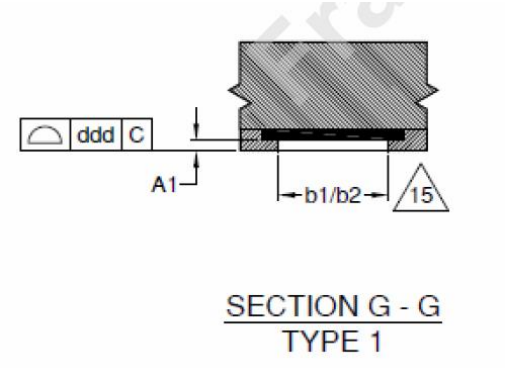


Figure 13: Type 1 definition for solderable substrate surface from JEDEC publication 95, Design guide 4.25, February 2016, Item: 11.2-896S

Type 2: The diameter of the landing pad is used to define the solderable substrate surface as depicted in Figure 14. A clearance between the landing pad and the solder resist of 0.075 mm is required.

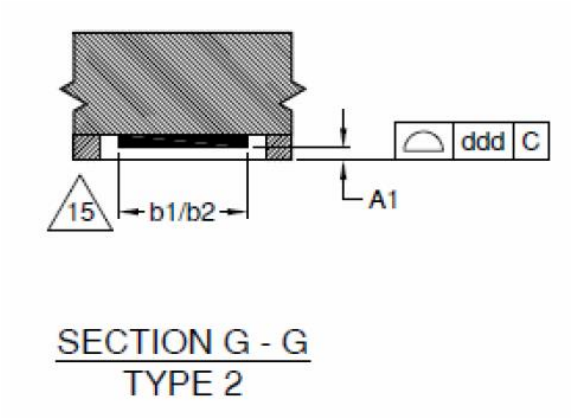


Figure 14: Type 2 definition for solderable substrate surface from JEDEC publication 95, Design guide 4.25, February 2016, Item: 11.2-896S

Distance between centerlines of any two adjacent rows of lands (eE = eD) [mm]	Minimum diameter solderable substrate surface for inner lands (not on the circumference of the package) [mm]	Minimum diameter solderable substrate surface for outer lands (on the circumference of the package) [mm]
0.80	0.50	0.65
0.65	0.35	0.50
0.50	0.20	N/A

Table 5: Diameter of solderable substrate surface as function of centerline distance

Maximum number of transitions: The maximum possible number of transitions for a given package size depends on the distance between the centerlines of any two adjacent rows. For a package size of 15.6mm x 7.8mm this translates to the following maximum numbers of transitions.

Distance between centerlines of any two adjacent rows of lands (eE = eD[mm]	Maximum number of transitions
0.80	171
0.65	253
0.50	420

Table 6: Maximum number of transitions as function of centerline distance

Further details on the BGA and FLGA interfaces can be found in the respective JEDEC publication.

Bibliography

[1] Ivan Ndip, Klaus-Dieter Lang, “Role and Requirements of Electronic Packaging in 5G”, accepted for oral presentation at the *2018 IEEE Electronics System-Integration Technology Conference (ESTC)*, Dresden, Germany, September 18-21, 2018.
[2] SERENA Proposal NUMBER — 779305 — SERENA
[3] SERENA project: ‘39 GHz Proof-of-concept platform and front-end specifications’, Deliverable 1.1
[4] JEDEC publication 95, Design guide 4.25, ‘Fine-Pitch, Land Grid Array Package, Square and Rectangular’, August 2016, Item 11.2-896S, Issue B
[5] JEDEC publication 95, Design registration 4.5, ‘Ball Grid Array Package and Interstitial Ball Grid Array Package Ball Pitch = 0.40, 0.50, 0.65, 0.75 and 0.80mm, Body sizes = ≤ 21mm’, February 2018, Item 11.2-945, Issue N