D1.1

39 GHz Proof-of-concept platform and front-end specifications

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Abstract:	This document reports on the architecture and specifications of the 5G 39 GHz proof-of-concept demonstrator system. The aim of the report is to set the scene for the development of the constituent sub-systems (e.g. antennas, front-end circuits, signal processing etc.).
Keywords:	Specification, front-end, system

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Executive Summary

This report introduces the system architecture of the SERENA 5G 39 GHz proof-of-concept demonstrator and associated system requirements. Both the architecture and the requirements are heavily influenced by the technology that is available to the SERENA consortium. Hence, the system architecture does not aspire to be an optimum 5G system but rather a reflection of current state-of-the-art as available to the SERENA partners.

The proposed system architecture is based on hybrid beamforming. The hybrid beamforming system is built around four building blocks: a multi-channel digital transceiver system from TU Berlin, a four channel analog RF beamformer from Infineon, a single channel GaN-on-Si front-end MMIC from OMMIC and a planar antenna array from Ericsson. The building blocks are then integrated using the embedded die integration platform from Fraunhofer IZM.

The proposed architecture is using a modular approach that enables scaling in terms of number of active antenna branches as well as number of baseband streams. This modularity enables scaling of both the effective isotropic radiated power (EIRP) and the effective isotropic sensitivity (EIS).

Disclaimer

Contents

List of Figures

List of Tables

Chapter 1 Introduction

The objective of this report is to define the hybrid architecture of the SERENA 39 GHz 5G proof-of-concept demonstrator. The main purpose of the proof-of-concept demonstrator is to provide a realistic context for hybrid beamforming, the GaN-on-Si technology and the SERENA integration platform. The system requirements will be as realistic and product like as possible, but the ambition is not to present an optimum mm-wave 5G system. Were appropriate the system will strive to fulfil the emerging NR 3GPP specifications. The system requirements and architecture will then be used in WP2, WP3, WP5 and WP6 to design, build and test the proof-of-concept system.

The report is organized as follows. In Chapter 2 the system requirements and architecture will be presented. The approach is to first outline key system requirements for a typical wide area coverage 5G mm-wave radio base station. The architecture will then be presented given a set of assumptions of the basic building blocks. These assumptions are not requirements per say but rather limitations or simplifications that are necessary to limit the scope of the proof-of-concept system. In Chapter 3 the system requirements and specifications for the proof-of-concept system is given. The proof-of-concept system will be implemented as a subset of the wide area coverage 5G mm-wave base station outlined in Chapter 2. The intent is that the smaller subset should be scalable to the final implementation. Chapter 4 presents the target specifications of the various sub-systems like the GaN-on-Si front-end, SiGe beamformer and antennas. In Chapter 5 we discuss some economical aspects relating to the SERENA architecture. In Chapter 6 the findings will be summarized.

Chapter 2 System architecture

In the standardization of the 5G radio interface (NR) by 3GPP[1], three classes of base stations are identified: wide area base stations, medium range base stations and local area base stations. The deployment scenarios for the wide area base station is a minimum distance (along the ground) of 35m between the base station and the user equipment (UE). The minimum distance for the medium and local area base station is 5m and 2m, respectively.

The system requirements given in section 2.1 are, were appropriate, in agreement with the 3GPP standardization for a wide area class of mm-wave base station.

2.1 System requirements

The below requirements are for a fully implemented system. These requirements will be re-calculated to reflect the performance of the smaller SERENA proof-of-concept system.

2.1.1 Service area

The system should be able to service an area of ±45 degrees in azimuth and ±15 degrees in elevation.

2.1.2 Effective Isotropic Sensitivity (EIS)

The system should have EIS better in the range of -96 dBm to -116 dBm.

2.1.3 Effective Isotropic radiated power (EIRP)

The system should have EIRP higher than 60 dBm.

2.1.4 Area capacity

The system should have an area capacity better than 60 Gbps/km2, for a cell radius of 300 m.

2.1.5 Polarization

The system should support horizontal and vertical polarization.

2.1.6 Modulation

The linearity of the transmitters and receivers should support 800 MHz wide modulation. The modulation could either be either single-carrier QAM64 or OFDM with QAM64 on each sub-carrier. The EVM of QAM16 sub-carrier should be better than 8%.

[1] 3GPP 5G Release 15, 38.104 radio base station specifications

2.1.7 Power consumption

The system should have a power consumption below 350 W.

2.1.8 Volume

The system should have a volume less than 6 litres.

2.1.9 Weight

The weight of the system should be less than 10 kg.

2.2 Assumptions

This section will postulate the assumptions and requisites that will be used as boundary conditions for the SERENA 39 GHz proof-of-concept system and sub-systems. These assumptions are all based on the given state of technology and what is available to the SERENA project. It is important to note that these assumptions do not necessarily reflect an optimum system or a preferred system. These assumptions will naturally limit the scope of the proof-of-concept system.

2.2.1 The antenna element will be single polarized

The antenna elements used for the proof-of-concept platform will be single polarized. The polarization will be either vertical or horizontal.

2.2.2 Each active branch is connected to at least two antenna elements

By using sub-arrays, we increase the real-estate available for active electronics and passive elements. From a system perspective the effect is an increase in the antenna element gain (per active branch) at the cost of less isotropic radiation and an influence on the overall array dimensions. There is thus a trade-off in the steering range in either elevation or azimuth. Furthermore, we may assume that each antenna element occupies an area of λ/2 times λ/2, with an antenna to antenna spacing of λ/2 between elements, where λ is the free space wavelength of the centre frequency. Due to the use of sub-arrays with two elements per array the antenna spacing seen by the beamforming in one direction is λ. The other direction has a spacing of λ/2.

2.2.3 RF analog beamformers with four branches

The beamformers available to the SERENA project will have one bi-directional common port, four bi-directional front-end ports. The beamformer will operate at RF frequency and will not include up/down conversion. The beamformers will provide functionality for programmable phase shifts and gain. For detailed specifications see 4.2.

2.2.4 RF front-end has two bi-directional ports

Each RF front-end is connected to a beamformer port. One front-end bi-directional port is within the front-end connected to the input of the LNA and the output of the PA. This port is connected to the antenna sub-array. The other port is connected to the LNA output and the PA input. This port is connected to one beamformer front-end port.

2.2.5 Antenna elements fed by a beamformer are placed adjacent to each other

To minimize RF losses and complexity of RF routing the antenna elements fed by one beamformer must be arranged adjacent to each other. Examples include stacking four antenna sub-arrays in one column (Figure 1), or arranging four sub-arrays in a rectangular fashion (Figure 2). In the figures the antenna elements have indices x, y, z. x denotes the index of the beamformer in the system, y the index of the RF front-end ($y \in \{1,2,3,4\}$) and z is the element index in the sub-array ($z \in \{1,2\}$).

To form an entire system these groups are rearranged multiple times next to each other. The distance between adjacent antenna elements is hereby always λ/2. The dotted boxes around the groups in Figure 1 and Figure 2 show the resulting limits of the groups. As can be seen in Figure 1 the stacked configuration is not feasible in combination with the planned size of the beamformer (see 4.2). Therefore, the clover-leaf arrangement as shown in Figure 2 will be implemented.

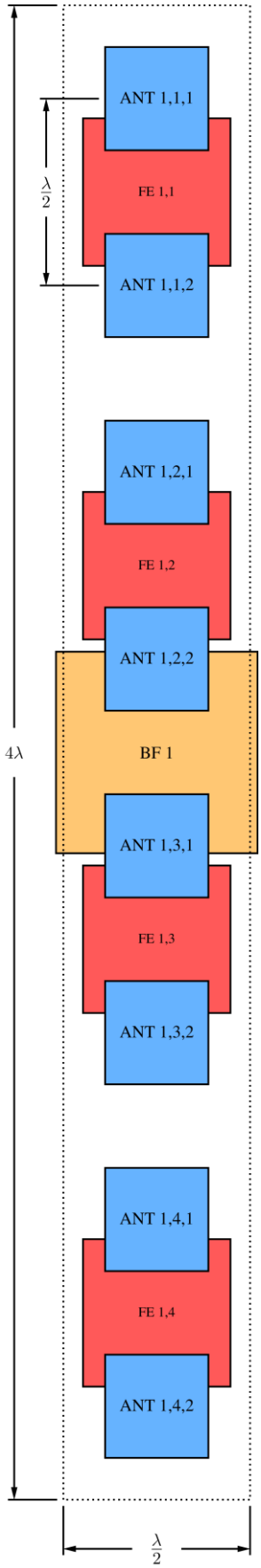

Figure 1: Stacked sub-arrays forming a column

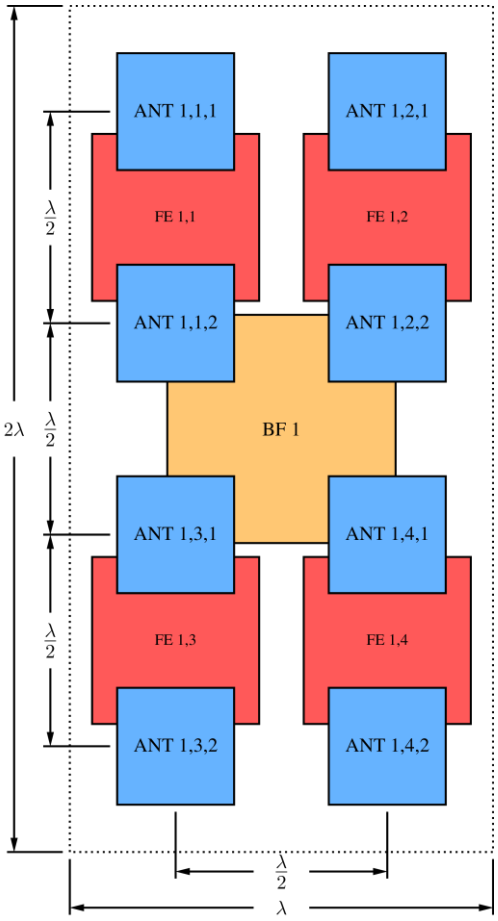

Figure 2: Sub-arrays arranged as clover-leaf

2.2.6 Up/down conversion is provided by an analog front-end

An analog-front end will provide up- and down-conversion from the digital transceiver to the RF beamformer. The analog front-end will be placed on the *system board*.

2.2.7 Each digital transceiver is connected to one or more RF beamformers

By connecting one or more RF beamformers to a digital transceiver we can create digital-to-analog port reduction (multiplication in transmit mode) in increments of four.

2.2.8 The digital transceiver is not integrated to the system board

To increase the testability of the proof-of-concept system the digital transceiver is not to be integrated with the *system board*. The primary candidate for the digital transceiver is the existing system at TU Berlin.

2.2.9 The proof-of-concept is a subset of a full radio base station implementation

A full-scale implementation of a mm-wave radio base station will most likely consist of several hundred antenna elements. From a complexity and yield perspective it is not feasible to build such a large and complex system within the project. Hence, the SERENA proof-of-concept system will consist of a subset of a final wide area radio base station implementation.

2.3 Architecture

Figure 3 shows the proposed system architecture. The architecture is based on the assumptions outlined in Section 2.2. The architecture is based on a scalable concept consisting of RF modules having a four channel SiGe beamformer and four GaN-on-Si front-ends. The module will be implemented using the embedded die integration platform. The antennas will either be integrated with the modules or put on a separate antenna board. One or more such RF modules may then be connected to a frequency converter module. In two RF modules are connected to each frequency converter. The RF modules are mounted to a system board containing the AFE, LO- and clock-generation functionality. The system board will in term be connected to digital base band system. The proposed architecture provides scalability in terms of analog channels as well as the number of digital base band channels.

Figure 4Figure 9 depicts a more detailed view of the proposed implementation of a single digital base band path. Depending on the final requirements of the band pass filter of the frequency convert module it may either be implemented in the frequency converter module or in the RF module.

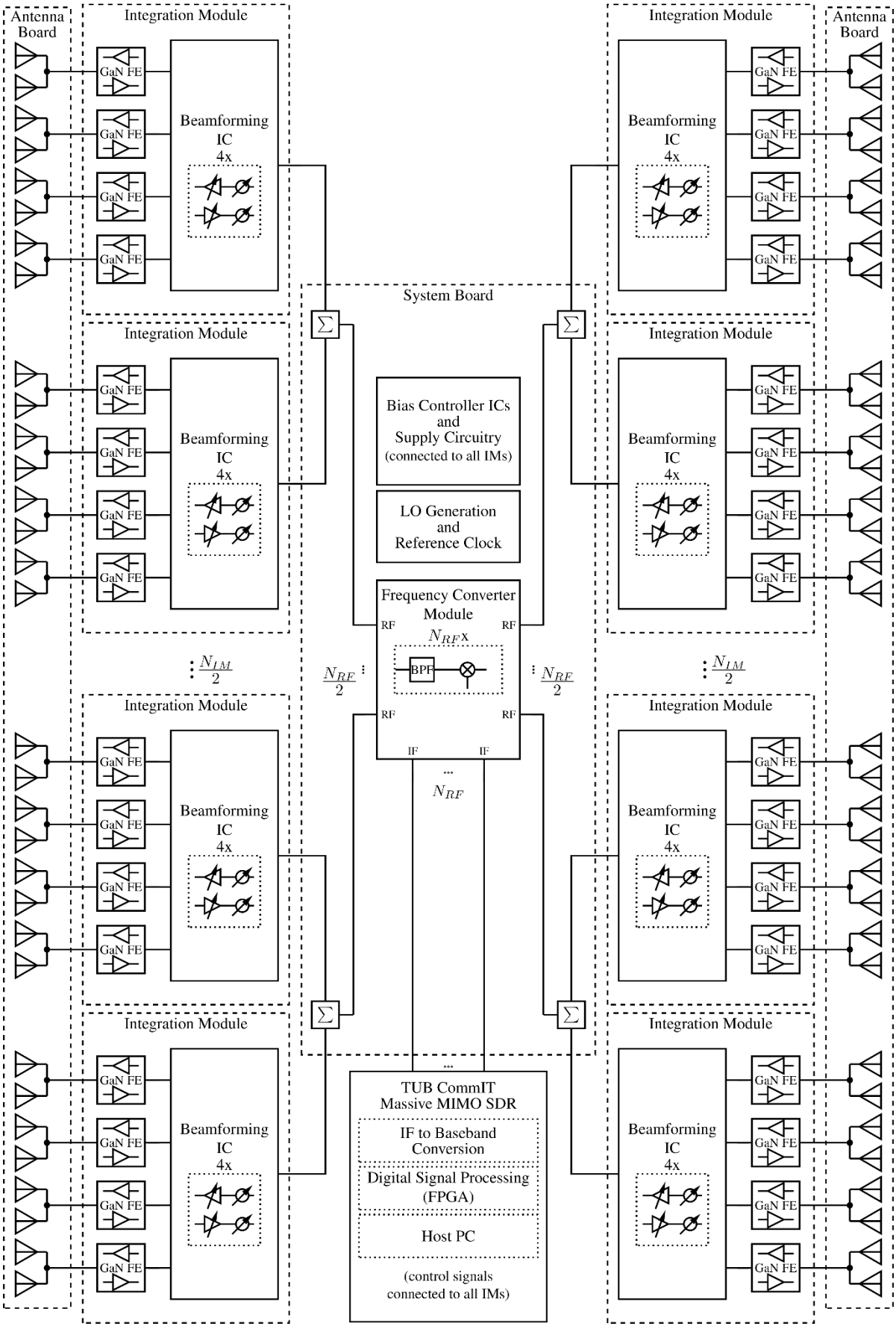

Figure 3: System architecture

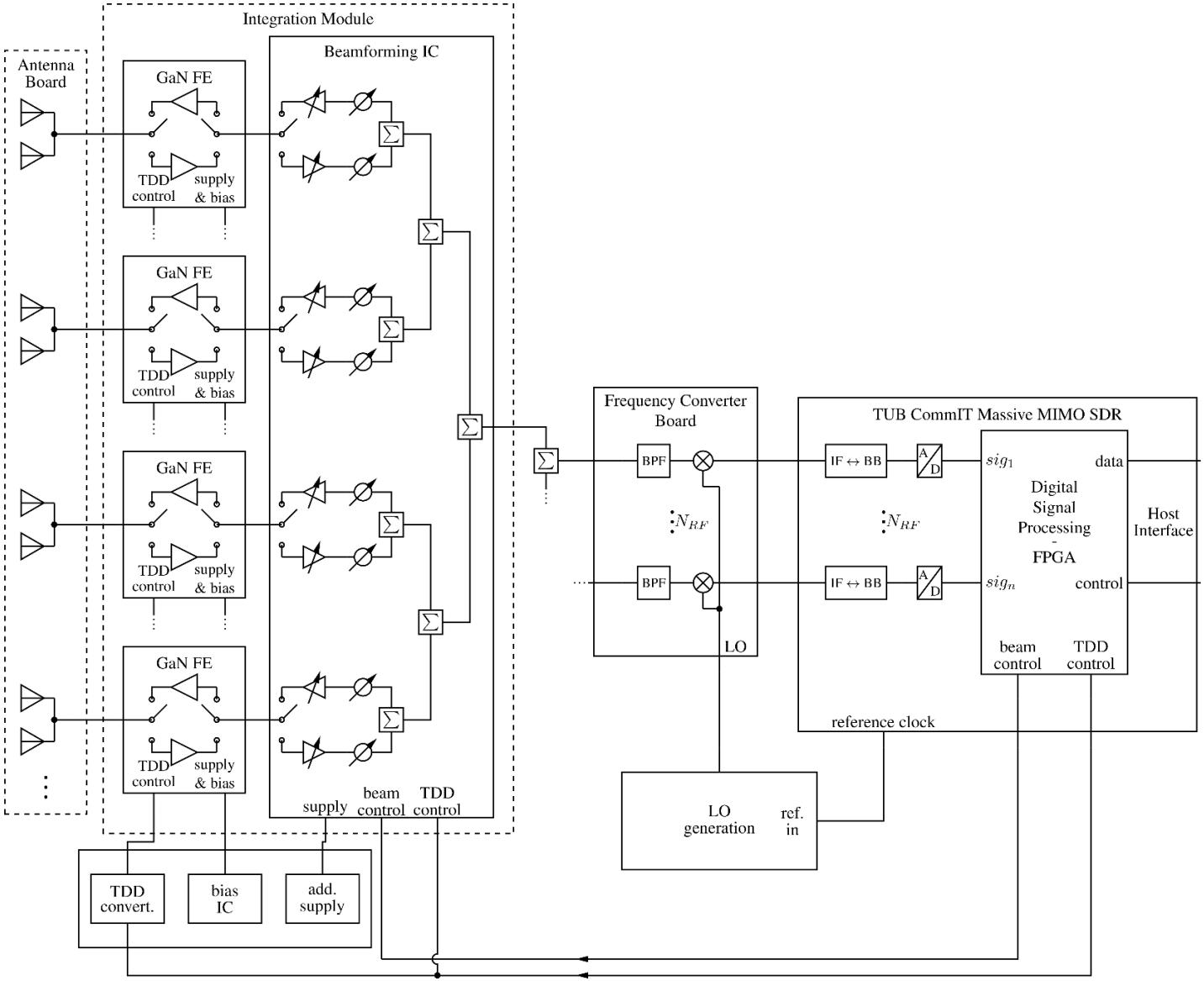

Figure 4: Single path detailed block diagram

Chapter 3 Proof-of-concept system specifications

The below requirements are for the proof-of-concept system. These are a subset of the specifications for the fully implemented system to ease the handling while testing and to minimize the risk of a failure of the proof-of-concept phase.

To provide a meaningful demonstration of the hybrid beamforming capabilities the number of baseband streams should be in the range of four to eight. To further simplify the proof-of-concept system we will omit beamforming in elevation.

3.1 Target specifications for the proof-of-concept system

3.1.1 Service area

The proof-of-concept system should be able to service an area of ±45 degrees in azimuth with beamforming and with fixed beamforming in elevation.

3.1.2 Effective Isotropic Sensitivity (EIS)

There will be no target specification for EIS for the proof-of-concept system. The EIS will be estimated during the design phase and later characterized for the proof-of-concept system.

3.1.3 Effective Isotropic radiated power (EIRP)

The proof-of-concept system should have EIRP higher than 50 dBm.

3.1.4 Area capacity

The proof-of-concept system should have an area capacity better than 60 Gbps/km2, for a cell radius of 100 m. For the proof-of-concept system the targeted cell radius is reduced. This implies that the proof-of-concept system and the full system will operate at the same SNR level at the cell edge.

3.1.5 Polarization

The system should support horizontal or vertical polarization.

3.1.6 Modulation

The linearity of the transmitters and receivers should support 800 MHz wide modulation. The modulation could either be either single-carrier QAM64 or OFDM with QAM64 on each sub-carrier. The targeted linearity for a QAM16 carrier is EVM better than 8%.

3.1.7 Power consumption

The beamformers and front-ends of the proof-of-concept system should have a power consumption below 100 W.

3.2 Transmitter link budget

Table 1 shows gain and power budget for single transmitter channel. The gain and power levels have been adjusted to reflect what can be achieved (beamformer and GaN-on-Si front-end). The gain of the beamformer have been used to adjust the drive level of the GaN-on-Si front-end. Similar gain adjustment needs to later be performed in the analog front-end.

Table 1: Gain and power budget for a single transmitter chain

Transmit main path	Gain @ average power during operation [dB]	Signal level @ average power during operation [dBm]
IF input		-6.00
Coax cable	-2.00	-8.00
Connector (SMP)	-0.50	-8.50
Transmission line	-0.50	-9.00
Upconverter	-10.00	-19.00
Amplifier	15.00	-4.00
Filter	-4.00	-8.00
Transmission line	-0.50	-8.50
Connector (MMPX)	-0.50	-9.00
Coax cable	-2.00	-11.00
Connector (MMPX)	-0.50	-11.50
Splitter (1-to-2)	-4.50	-16.00
Transmission line	-0.50	-16.50
Module connection (soldering)	-1.00	-17.50
Transmission line	-0.50	-18.00
Beamer 39	17.50	-0.50
Transmission line	-1.5	-2.00
GaN F-E (DA + PA + switch)	27.00	25.00
Connection (lines, vias, soldering)	-1.00	24.00
Filter	0	24.00
ARP		24.00

Chapter 4 Sub-system specifications

4.1 Antenna array

Since the actual implementation of the antenna array will be done in WP6 no detailed antenna array specifications will be given. The requirements of the elements of the antenna array is to be either horizontally or vertically polarised and that he implementation should be planar. The radiating element will be implemented either as a radiating patch or slot.

The embedded antenna element should have a return loss better than 10 dB in the frequency range of 37 GHz to 40 GHz. The size of the element should be smaller than half the free space wavelength at 37 GHz. The gain of the embedded pattern should be higher than 4 dBi across the frequency band.

4.2 SiGe Beamformer

The SiGe Beamformer comprises a four channel beamforming transmit receive RFIC featuring over 30dB of amplitude control and phase/ delay control based on digitally programmable delay lines providing 360° of phase control range or 19 ps of true time delay control. The IC will also include built in test equipment for on chip phase and amplitude calibration of the RFIC channels, additionally supporting system calibration. Target applications: Phased Array Transceivers for 5G Communication.

A draft block diagram of the proposed IC is shown in Figure 5. The target dimensions of the RFIC is 4.1 mm x 4.1 mm. The preliminary pin-out is shown in Figure 6.

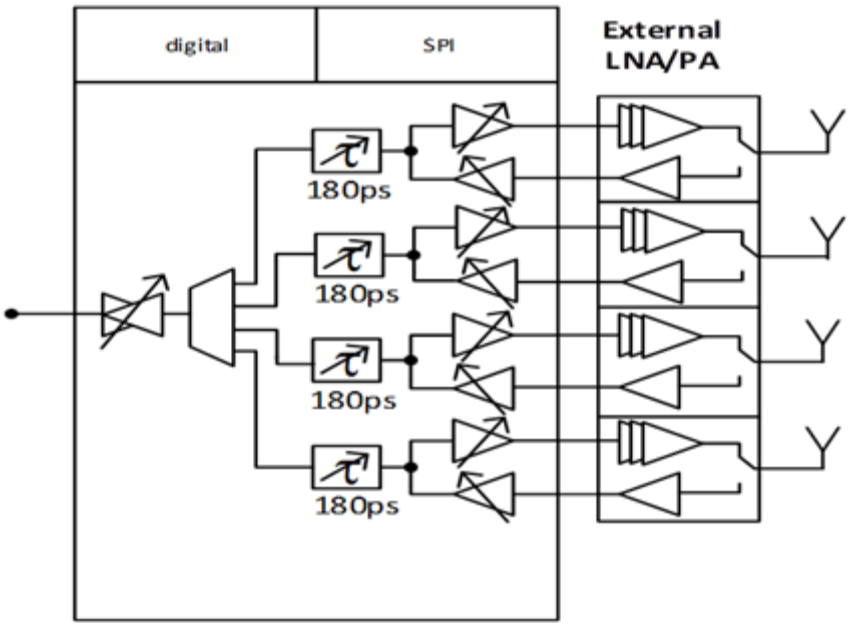

Figure 5: Beamer 39, Beamforming IC block diagram

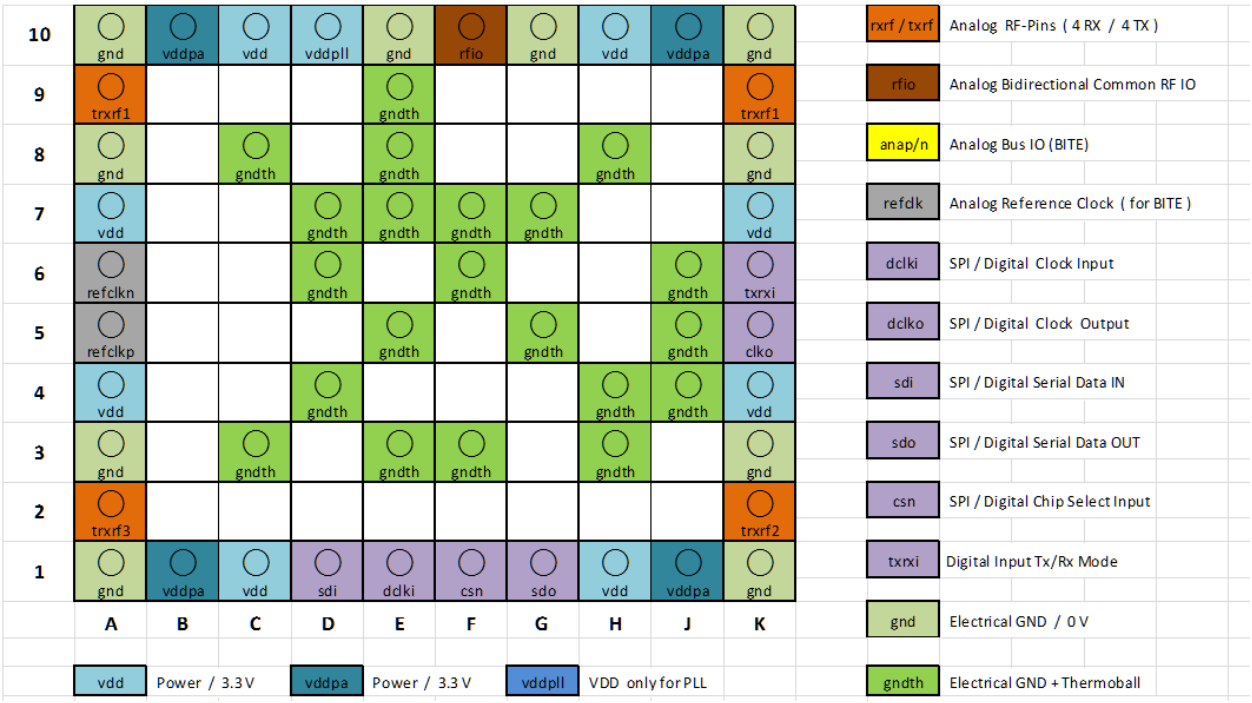

Figure 6: Beamforming IC pin-out

4.2.1 Beamformer electrical target specifications

Table 2: Beamformer electrical target specifications

Parameter	Specification	Comment
Frequency Range	37.0 – 43.5 GHz	
Number of channels	4	
RF to Antenna interface	Single-ended Bi-directional	
RF to Frequency converter interface	Single-ended Bi-directional	
RF instantaneous bandwidth	800 MHz	
RF delay range	19 ps	Used for phase control in combination with inverting amplifier stage. (6 bits)
RF port match	12 dB	
Switch time (RX to TX, RX to TX)	less than 3 us	
Supply Voltage	3.3 V	2W / 2W (Rx / Tx)

4.2.1.1 Transmit mode target characteristics

Table 3: Transmit mode target characteristics

Parameter	Specification	Comment
Gain control range	30 dB	Resolution: 0.5 dB
TX OP1dB	5 dBm	
TX OIP3	16 dBm	
TX NF	15 dB	

4.2.1.2 Receive mode target characteristics

Table 4: Receive mode target characteristics

Parameter	Specification	Comment
RX IIP3	-10 dBm	
RX NF	10 dB	Including 6 dB loss in Wilkinson combiner
Gain control range	30 dB	Resolution: 0.5 dB

4.3 GaN-on-Si RF front-end

This section covers the electrical and mechanical specifications of the GaN RF front-end. The developed front-end will consist of a receive branch and a transmit branch. The branches will be selected by two single-pole-double-throw (SPDT) switches. The transmit branch has a four stage power amplifier whereas the receive branch has a three stage low noise amplifier. The target specifications are listed in Table 5,Table 6, and Table 7.

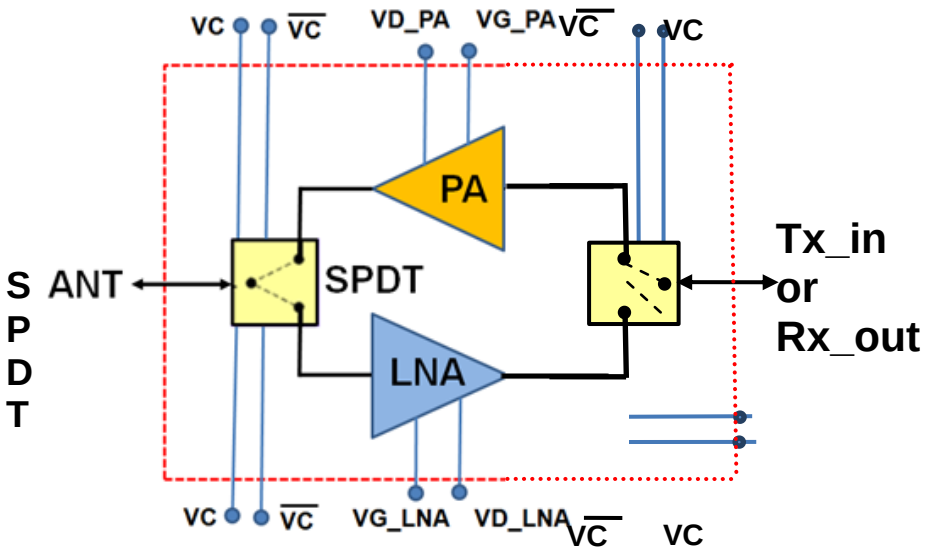

Figure 7: Block diagram of the GaN-on-Si RF front-end MMIC

4.3.1 GaN-on-Si front-end specifications

Table 5: GaN RF front-end general specifications

Parameter	Target	Unit	Comment
MMIC die size	3 x 3	mm x mm	Maximum
MMIC die thickness	100	um	Typical
Pad-size	100 x 100	um x um	Minimum
Switch time (RX to TX)	10	us	Maximum
Switch time (TX to RX)	10	us	Maximum
Switch control voltage (VC, VCQ)	-24	V	Minimum

4.3.2 Transmit mode target specifications

Table 6: GaN RF front-end MMIC TX specifications

Parameter	Target	Unit	Comment
Small-signal gain	27	dB	Minimum
Output power (P3dB)	34	dBm	@10 dBm input power
DC Current at P3dB	1.3	A	@P3dB
Power consumption[2]	7.5	W	@28 dBm Pout
Input return loss	12	dB	Minimum
Output return loss	10	dB	Minimum
Supply voltage (VDD)	12	V	
Gate voltage (VGG)	-4 to 0	V	(-2 V to -1 V)

4.3.3 Receive mode target specifications

Table 7: GaN RF front-end RX specifications

Parameter	Target	Unit	Comment
Small-signal gain	15	dB	Typical
Noise Figure	3.5	dB	Typical
Power consumption	300	mW	Maximum
Input return loss	10	dB	Minimum
Output return loss	12	dB	Minimum
Supply voltage (VDD)	5	V	
Reference voltage (VSS)	-5	V	

4.4 Smart bias controller

The GaN front-end will be controlled by a bias control IC. This IC is in development by Infineon and it will support two PAs with 4 DACs and 2 high-side (HS) switches each. Both channels are supplied by external voltages (typical 3.3V, 28V). The supply of the DACs (typical 6.6 V) is generated by a on chip-internal Charge Pump (CP) with external pumping capacitors.

[2] No simulations of the power consumption at 9 dB back-off from the P3dB compression point have been made yet. The estimated power consumption is below 6 W.

The High Voltage Supply of the PAs is provided through HS-Switches, which also include a current measurement function (8-bit, 0mA to 100mA) and an overcurrent protection. The result is available in registers that can be read out with from the SPI-bus.

The 5V supply of the Low Noise Amplifier (LNA) is provided through another overcurrent protected (>500mA) switch.

Voltage monitoring (e.g. PA Supply) is done with an 8-bit ADC. In addition to supervision functions the voltages can be read out through the SPI-bus.

Default settings will be stored in a One Time Programmable Memory and will be loaded after power-up.

Basic Features of the Bias Control IC:

- Support of 2 independent PAs
- 2 x 4 monotonic 12-bit DACs for bias-adjustment
- 2 selectable ranges (–6V to 0V or 0V to 6 V)
- Driving capability up to 3mA
- Fast clamping for TDD-support
- 2 High-Side Switches <40V
- Very low Ron of 100mv
- Short circuit protection (>2.5 A)
- Special mode for current measurement: 8-bit, Range: 0mA to 100mA
- 2 HS Switches <40V
- Ron of 500mv
- Short circuit protection (>500mA)
- Special mode for current measurement: 8-bit, Range: 0mA to 50mA
- 2 HS Switches 3.3V[3]
- Ron of 200 mOhm
- 8 Bit current measurement and short circuit protection (>500mA)
- 2 Charge-Pumps for generating 6 V, up to 6mA loads
- Voltage monitoring ADC, 8-bit, with internal reference
- SPI or I3C-Interface for configuration and real-time control for TDD support
- On-Chip One Time Programmable Memory (OTP), electrically programmable in Backend
- On-Chip temperature sensing for temperature compensation and over-temperature shutdown
- Operating Temperature Range: –40 C to 125 C

The core block diagram of the bias control IC is shown in

Figure 8. Only one chain is shown. Digital control / SPI not shown.

[3] The original plan was to use these switches to turn the LNA on and off. However, the LNA supply voltage will be 5V which will prohibit the direct use of these switches.

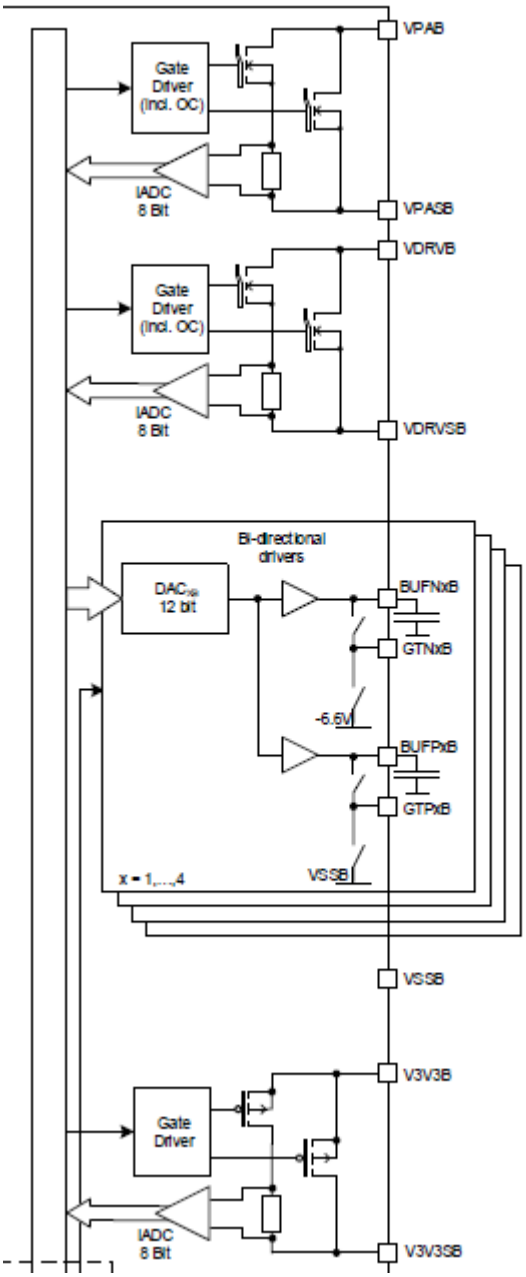

Figure 8: Bias control IC block diagram (core unit)

4.5 Analog front-end

As can be seen in the detailed block diagram of the system architecture in Figure 4, the analog front-end has a transceiver architecture with an intermediate frequency (IF) and an IQ conversion to a complex baseband. The RF signals are down- respectively up-converted to the IF using RF mixers. The IF is 3GHz. The IF signals are converted to the complex baseband and vice versa with IQ modulators and demodulators. Table 8 lists the minimum specifications of the up-/down-conversion and filtering in the analog front-end. The final filtering requirements will depend on the overall transmitter gain and the frequency planning of the up-/down-converter. At this point in time these details are not known and the detailed specification work is referred to WP6 in which is responsible for the detailed design of the proof-of-concept system.

Table 8: Analog Front-End specifications

Parameter	Target	Unit	Comment
RF frequency range	37-40	GHz	Minimum
IF frequency	3	GHz	Typical
Gain	5	dB	Minimum
Power consumption	1.5	W	Typical
Filter passband insertion loss	4	dB	Maximum
Filter stopband attenuation	25	dBc	Minimum
Filter stopband frequencies	TBD	GHz	

The conversion between the IF and the baseband is implemented using the TUB CommIT massive MIMO platform. The system board generating the IF signal is connected with one coax cable per IF signal to the TUB platform. The IF signals are converted to a complex analog baseband which is then converted to digital streams (for RX, for TX the order is reversed). The specifications of the platform are listed in Table 9. It supports up to 192 signal streams with a limited bandwidth of 20 MHz. The bandwidth can be increased up to 56 MHz while decreasing the number of streams to 80. 80 streams are more than sufficient for a hybrid architecture as used in the SERENA proof-of-concept. The TUB platform was developed outside of SERENA. It is used for the proof-of-concept system to enable an efficient and fast implementation. Due to this it limits the proof-of-concept system in some respects for example in the bandwidth but enables a fast way to proof and demonstrate the system for the main applications. The parameters of the SERENA integration system limited by the TUB CommIT massive MIMO platform can and will be characterized separately. In this way the integration system is fully and without limitations characterized but the proof-of-concept can demonstrate the main applications on a higher level.

Table 9: Specifications of the analog part of the TUB CommIT massive MIMO platform

Parameter	Value	Unit	Comment
Carrier frequency	3	GHz	Variable between 0.1 – 6.0 GHz
Number of signal streams	80		With 56 MHz bandwidth each
Bandwidth	56	MHz	
Output power	6	dBm	Maximum
TX power control range	90	dB	
Noise figure	4	dB	Maximum
RX gain range	0 – 65	dB	Typical
Modulation Accuracy (EVM)	-40	dB	Typical

4.6 Digital front-end

The digital signal streams are also processed on the TUB CommIT massive MIMO platform. A block diagram of the platform can be seen in Figure 9 and the parameters of the signal processing part are listed in Table 10. The digital samples of the signal streams are aggregated on intermediate boards of the platform (called MMIB in the block diagram) and transferred to a central signal processing (CSP) module. The CSP is a FPGA module using an Intel Arria 10 FPGA with sufficient processing power to implement real time processing for the communication application of the proof-of-concept system. Furthermore, the CSP is connected via a PCIe interface to a host PC. Through this interface the system can be controlled and signal data can be transferred. It is also possible to directly transfer signal samples between a signal processing software, for example Mathworks Matlab®, on the host PC and the signal converters sampling respectively generating the analog signals. This allows for a very fast development and investigation of signal processing algorithms.

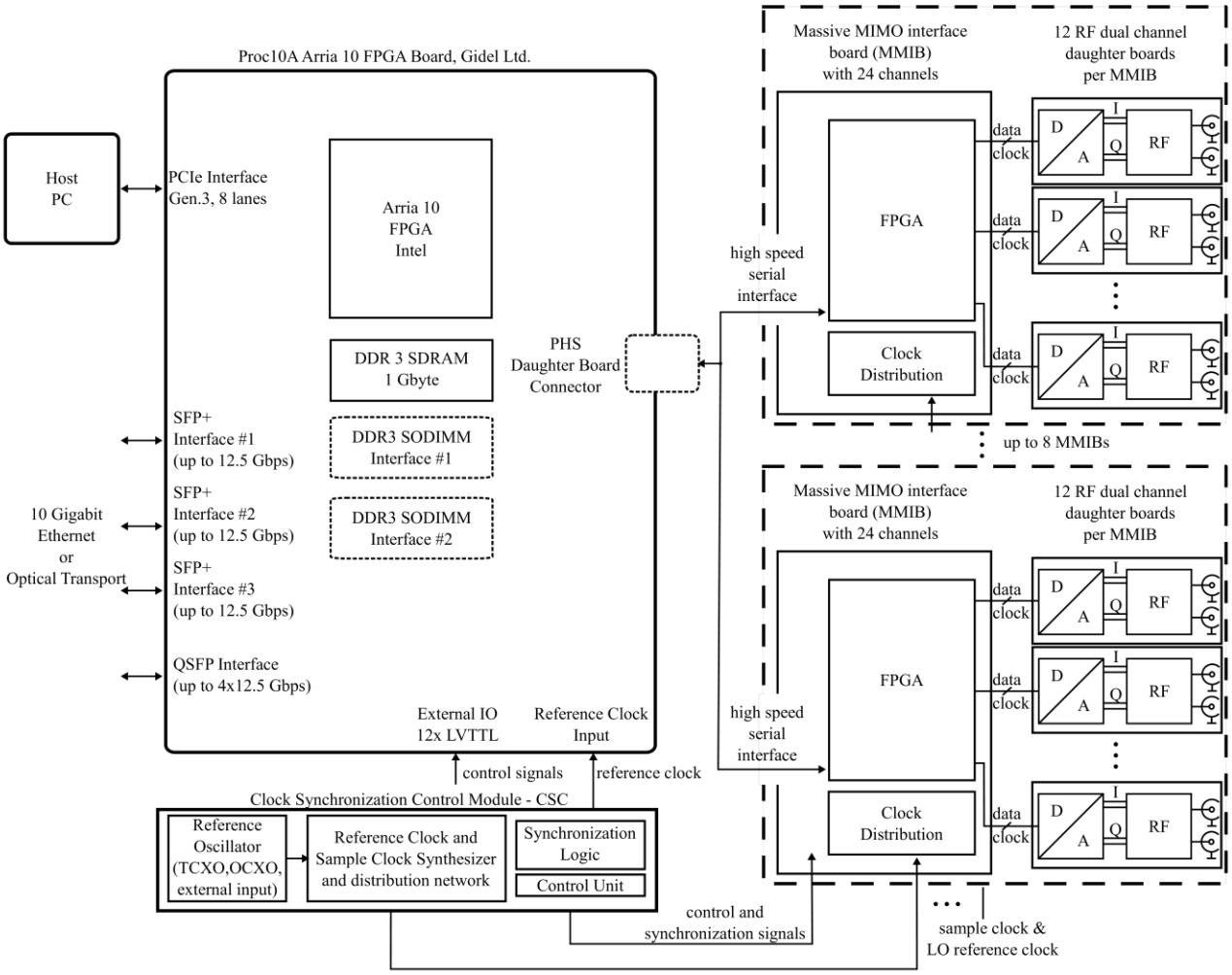

Figure 9: TUB CommIT massive MIMO platform architecture

Table 10: Parameters of the digital front-end

Parameter	Value	Unit	Comment
Sample rate	56	MSPS	
ADC / DAC resolution	8	bit	
Aggregated bit rate to the CSP	80	Gbit/s	Maximum
CSP logic elements	1.1 Million		
CSP 18 bit floating point multipliers	3036		

The digital signal processing respectively the algorithms which are run on the platform for the communication application of the proof-of-concept are investigated in task T1.2 and presented in the deliverable D1.4.

Chapter 5 Economical aspects

Mm-wave 5G systems depend on active antennas with beamforming. The cost of active phased array antennas at mm-wave frequencies have historically been very high. The main contributing factors to the high cost is the semiconductors, packaging, antennas and testing. One of the main objectives of the SERENA project is to substantially lower the cost of active mm-wave antennas. The main focus of SERENA is the front-end electronics and the integration towards antenna and control circuits.

SERENA approaches the high cost of semiconductors (GaAs and GaN-on-SiC) by exploring GaN-on-Si technology. Moving to Silicon substrates provides a path to increased wafer sizes (from 100 mm diameter to at least 200 mm) and hence a more efficient utilization of the wafer fabrication facilities. In the long run GaN-on-Si integrated circuits fabricated in a modern Si-fab should have the same cost as SiGe. The projected cost of the 5G mm-wave front-end (compared to GaN-on-SiC) could be lowered by a factor of 10. Furthermore, due to the high-power density of GaN the actual cost per delivered watt of output power would then be 10 times lower than that for CMOS or SiGe.

The second cost factor, that SERENA is addressing, is the packaging cost. By using embedded die PCB packaging there will be no additional cost for packaging each integrated circuit. Furthermore, by employing a modular concept each module can be tested prior to final assembly (known-good-module) and the yield of the antenna array can be increased.

It is not within the scope of SERENA to provide a detailed cost analysis of the full active antenna system. The approach is to use as low-cost techniques as possible. This will be a guiding principle for the system designs in WP5 and WP6.

Chapter 6 Summary and Conclusion

High-level target specifications for a typical wide area radio base station were presented. A hybrid beamforming system architecture fulfilling the specifications were then proposed. The proposed architecture are based on sub-systems and integration platforms being developed in WP2, WP3 and WP5. The architecture is based on four channel modules consisting of a SiGe analog beamformer RFIC and four GaN-on-Si front-end MMICs. This modular concept makes it possible to scale the number of analog and digital channels.

A first order analysis of necessary sub-system performance at the circuit level have also been made. Compared to initial assessment in the SERENA proposal the output power per channel have been reduced by 6 dB. The main reason is to minimize the size of each GaN-on-Si front-end. Furthermore, to increase the available area each front-end will drive a sub-array of two antennas.

A simplified proof-of-concept system is proposed. The simplified system is a representative subset of the wide area radio base station. The proof-of-concept system have the same area capacity as the full system but for a smaller cell radius. The design and evaluation of the proof-of-concept system will be made towards these target specifications.

Chapter 7 List of Abbreviations

Abbreviation	Translation
ADC	Analog to digital converter
CSP	Central signal processing
CMOS	Complementary metal oxide semiconductor
DAC	Digital to analog converter
dB	decibel
dBi	Decibel relative isotropic radiation
dBm	Decibel relative to 1 mW
DC	Direct current
EIRP	Effective isotropic radiated power
EIS	Effective isotropic sensitivity
EVM	Error vector magnitude
FPGA	Field programmable gate array
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Gbps	Giga bits per second
GHz	Giga Hertz
IF	Intermediate frequency
LNA	Low noise amplifier
MHz	Mega hertz
MIMO	Multiple input multiple output
MMIC	Microwave monolithic integrated circuit
MSPS	Mega samples per second
OFDM	Orthogonal frequency division multiplex
PA	Power amplifier

Abbreviation	Translation
PCB	Printed circuit board
QAM	Quadrature amplitude modulation
RF	Radio frequency
RFIC	Radio frequency integrated circuit
Si	Silicon
SiC	Silicon carbide
SiGe	Silicon Germanium
SPDT	Single pole double throw
SPI	Serial periphery interface
TBD	to be determined
TDD	time division duplex
TX	Transmitter
RX	Receiver