A Non-Isolated Asynchronous Low Power High Voltage Boost Converter for Discontinuous Conduction Mode and Portable Applications

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***Abstract*— This paper demonstrates the feasibility of a non-isolated single inductor asynchronous boost converter for driving piezoelectric actuators up to 100 V. The realized device is using a novel 700V bulk 0.35um CMOS XFAB technology. The control scheme for the boost converter, working in discontinuous conduction mode (DCM) only, is using a peak-current control scheme with adaptive off-time. For an input voltage range between 2.5V and 6V and output voltage up to 100V it achieves a peak-efficiency of 70% by using a die area of 22.9 mm^2.**

Keywords—DCM; High Voltage Boost Converter; DCDC converter; Peak Current Control

I. INTRODUCTION

Emerging new applications for battery powered IoT (Internet of Things) sensors and actuators are expected to be one of the key drivers for the growth of the electronic and semiconductor markets. Besides the most commonly used buck and buck-boost converters several challenging new applications like chemical and biological IoT sensor nodes will have a high demand for energy efficient and especially highly integrated boost converters. In [1] an ultra-low-power boost converter for micro-scale energy scavenging using a dual-output boost converter and a capacitor as energy storage element is presented. An RF-energy harvesting system for biomedical implants is shown in [2]. New sensor nodes will require electronics to efficiently control MEMS (Micro Electrical Mechanical Systems) structures build up with e.g. piezoelectric actuators in micropumps [3]. For these MEMS supply voltages up to several hundred 100 V are required but with output power levels up to a few mW's.

The objective of this work is to show that high voltage gain can be achieved by using a single-stage inductive boost converter without transformers and using a dedicated cost-effective bulk CMOS technology. For the envisaged input and output voltage range the converter is designed for an operation in discontinuous conduction mode (DCM).

The remainder of this paper is organized as follows. A brief review of the state of the art of high-voltage high gain boost converters for DCM, together with the boost converter analysis is presented in Section II. The design of the converter with a technology description of the high voltage bulk CMOS devices is given in Section III. Experimental measurements of the converter under different load conditions are shown in Section IV. Finally, conclusions are presented in Section V.

II. HIGH VOLTAGE BOOST IN DCM

A. GENERAL

In [4] a transformerless boost converter with high step-up voltage gain is presented. The system is using 2 inductors and 3 additional diodes to reduce component stress and can operate in CCM (continuous conduction mode) and DCM. In [5] a current fed resonant topology is used to mitigate the transformer but is using one additional inductor and an H-bridge as switching module. This system is also targeting medium to high power applications.

In general DC-DC boost converters with high gain are broadly using transformer and coupled inductor based topologies

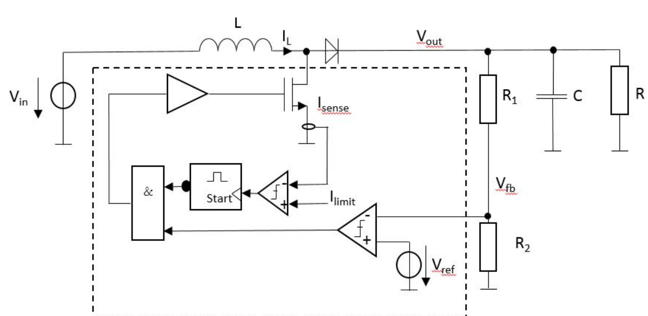

Fig. 1 System Overview

although there are difficulties involved in creating a transformer for high voltage switching applications. Parasitic

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capacitance can be a large source of loss in a transformer. The leakage inductance of a transformer often causes voltage spikes during switching events, which can become more severe as the operating voltage rises. In addition, reducing the size of magnetics through higher operating frequency is hindered for low power applications by the DCM mode. While use of transformers can facilitate high conversion ratios, if galvanic isolation is not necessary then a transformerless converter should be considered to avoid the difficulties of high voltage transformers.

B. DC gain of power stage in DCM

The theoretical DC gain, M, of a boost converter in CCM (continuous conduction mode) is well known and given by

$$D = \frac{M-1}{M} \qquad \text{and } M = \frac{V_{out}}{V_{in}} \quad , \tag{1}$$

where D is the duty cycle.

For a high transformation ratio with an output voltage up to and higher than 100 V and an input voltage defined by a Li-Ion battery the duty cycle D will need to be close to 1, which is difficult to achieve (Fig. 3). For low output power requirements the boost converter can also be operated in DCM.

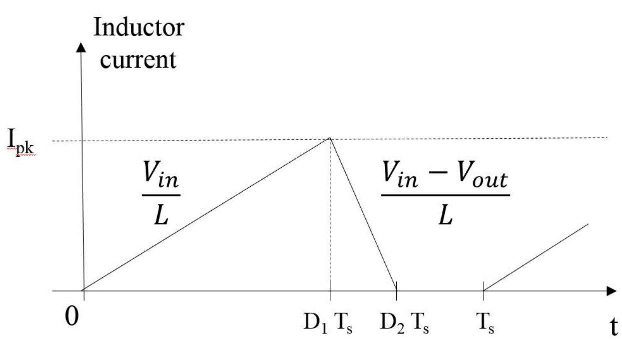

Fig. 2 Inductor current waveform for DCM

Following closely [6] and using the unified state-space representation we get the following set of equations with the waveforms shown in Fig. 2:

$$\dot{x} = \begin{bmatrix} \frac{V_{in}}{L} \\ -\frac{V_{out}}{RC} \end{bmatrix} \qquad \text{for } 0 <= t < D_1 T_s$$

$$\dot{x} = \begin{bmatrix} \frac{V_{in}-V_{out}}{L} \\ -\frac{V_{out}}{RC} + \frac{i}{C} \end{bmatrix} \qquad \text{for } D_1 T <= t < (D_1 + D_2) T_s$$

$$\dot{x} = \begin{bmatrix} 0 \\ -\frac{V_{out}}{RC} \end{bmatrix} \qquad \text{for } (D_1 + D_2) T_s <= t < T_s \tag{2}$$

With the state vector

$$\bar{x} = \begin{bmatrix} i_L \\ v_{out} \end{bmatrix} \tag{3}$$

and the generalized state-space averaging step for a three-state converter the single state-space description is

$$\dot{x} = \begin{pmatrix} 0 & -\frac{D_2}{L} \\ \frac{D_2}{C} & -\frac{1}{RC} \end{pmatrix} * x + \begin{pmatrix} \frac{D_1+D_2}{L} \\ 0 \end{pmatrix} * V_{in} \tag{4}$$

With (1) and using the derivation in [6] the quadratic formula for the DC gain in DCM is defined by:

$$M^2 - M - \frac{R\, D_1{}^2 T_s}{2\, L} = 0 \tag{5}$$

In a peak-current limit operating boost converter the on-time D_1*Ts is almost fixed and can be rewritten as

$$D_1 T_s = \frac{i_{pk}\, L}{v_{in}} \tag{6}$$

The quadratic formula is now changing to

$$M^2 - M - \frac{D_1 i_{pk}}{V_{in}\, 2} = 0 \tag{7}$$

So we get finally the solution for the DC gain M of a boost converter power stage in DCM using a peak current limit.

$$M = \frac{1}{2} * \left(1 + \sqrt{1 + 4KD_1}\right)$$

$$and \quad K = \frac{i_{pk}\, R}{V_{in}\, 2} \tag{8}$$

This result shows that for reasonable duty cycle values the gain can be increased by choosing an appropriate peak-current limit. As a concrete example, Fig. 3 shows the comparison

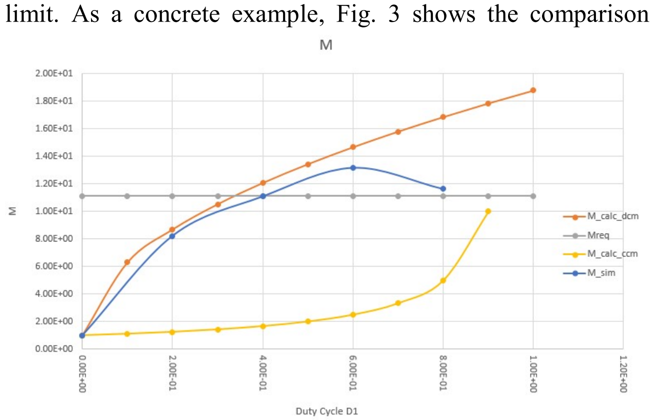

Fig. 3 Comparison between calculated and simulated open-loop DC gain (peak current limit set to 60 mA, R = 40 kOhm, Vin = 3.6V)

of the DC gain in CCM and DCM for a specific load resistance. It is remarkable that the DC gain with a single stage boost converter can be high enough for the required output voltage even at moderate duty cycles.

C. DESIGN

The system is shown in Fig. 1. The control scheme is based on a peak current control with adaptable off time. As soon as the output voltage drops and $V_{fb} < V_{ref}$ the comparator switches on the power FET. The current sense circuit finishes the on-time when it hits the current limit threshold and triggers the mono-flop for a predefined time TOFF. During this time the power FET is forced into the OFF state. In this 0.35um bulk high voltage CMOS technology the power FET and gate driver

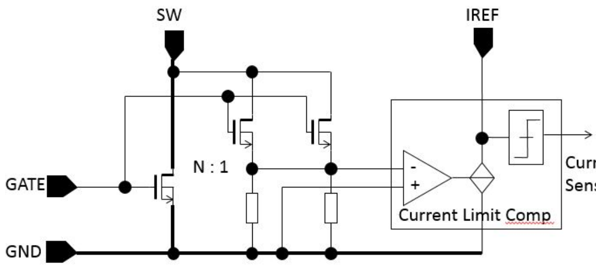

Fig. 4 Power FET, Sense FET and current limit amplifier

largely dominates the die size. As power FET device a 400V NMOS is selected with minimum drain-source breakdown voltage of 460V, which will enable the test of output voltages larger than 100V. The typical area specific on resistance $R_{dson,sp}$ is 5 Ohm-mm^2. The maximum current is set by the current limit which has to guarantee the DCM mode under all conditions. For the current limit setting and finally dimensioning the power FET size in this technology we get:

$$I_{limit} > \frac{2I_{load}}{(1-D)} \tag{9}$$

Operating conditions and a maximum load current of 0.5 mA require a current limit of approx. 100 mA so that R_{dson} has to be

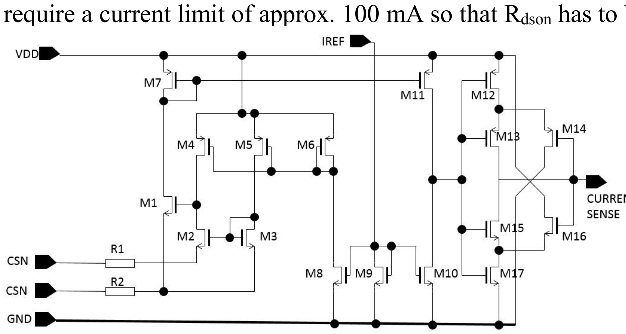

Fig. 5 Current sense amplifier, current comparator with hysteresis

lower than 1 Ohm to keep the power FET in the linear region. For the given technology parameter a W/L of 135kum/1.5um is chosen with a total area of 9 mm^2. The current sense is realized by a sense FET structure with a transformation ratio of 340 (Fig. 4) (Power FET size W/L = 135ku / 1.5u). The current sense amplifier is implemented by a 2-stage current-input amplifier where an output inverter with hysteresis is driving the following TOFF mono-flop circuit (Fig. 5).

III. EXPERIMENTAL RESULTS

The complete chip has been processed with XFAB XU035 technology and packaged within a QFN7x7 with 48 pins (Fig.7). This chip doesn't include only the boost converter but

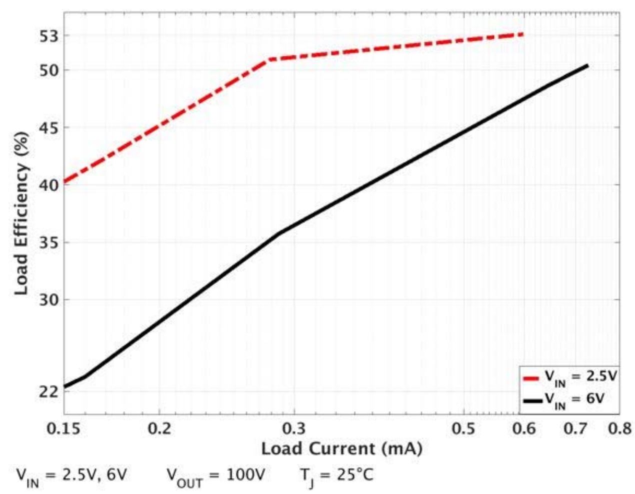

Fig. 6 Boost converter efficiency at Vout = 100V

also the negative power supply for the piezoelectric driven micropump and reference current generation. The package has been chosen for experimental purposes only. The efficiency measurements [Fig.5 and 6] demonstrates results for direct conversion from 2.5V to 100 V with a peak efficiency of 70%.

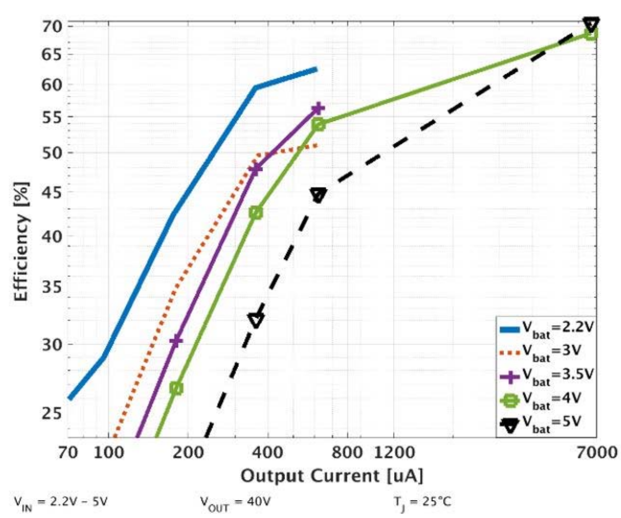

Fig. 7 Boost converter efficiency at Vout = 40V

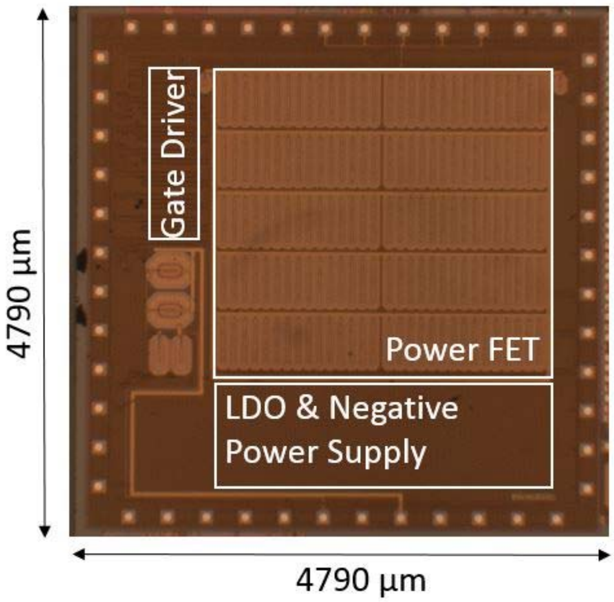

Fig. 8 Die photo

IV. CONCLUSIONS

A single inductor high voltage boost converter for portable applications has been presented. The work shows that DCDC boost converter operating in very high duty cycle conditions for applications with power consumptions in the range of mW's like micropumps with piezoelectric actuators can be realized without using any transformers and by applying modern high voltage bulk CMOS processes. Further optimization of the light load efficiency will be done by reducing the quiescent current and optimizing the power FET design for the target application.

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