A novel current-mode actuator driver for enhanced piezoelectric reliability

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***Abstract*—In this paper, we present a novel, piezoelectric actuator driver topology that combines high-voltage actuator driving in the range of -50 V- to +100 V with piezoelectric reliability. The output waveform is generated by a novel capacitor clamping circuit (patent# PCT/EP2016/066134) with programmable rise-and fall times implemented in a 0.35 um high-voltage bulk CMOS technology optimized for capacitive light-load (2 nF- to 8 nF) operation. The novel piezoelectric actuator driver consists of a negative voltage generator and a degradation regulator integrated onto a single chip. The smart driver electronics is optimized towards reliable piezoelectric operation by taking fatigue and electrical overstress into account. The novel piezoelectric actuator driver is the first step towards self-regulated electrical compensation of piezoelectric actuator degradation which promises increased actuator lifetime and reliable operation.**

Keywords— DC/DC Converter, Micropump Driver, Low-Power Loads, Piezoelectric Driver, Piezoelectric Reliability, High-Voltage Driver, DCM Operation

I. INTRODUCTION

With the ongoing miniaturization of Microelectromechanical Systems (MEMS), piezoelectric actuators (PA) are opening new application areas by converting an electrical signal into mechanical actuation or vice versa at minimum area requirements. Piezoelectric actuators promise high displacement accuracy, fast displacement speed and are able to generate high force at minimum area when properly driven. They are widely used in all fields of application, but especially when precise position control and high sensor performance is necessary, a high grade of strain stability and reliability are a prerequisite [1]. This work focuses on the implementation of a novel, miniaturized, fully integrated piezoelectric actuator driver topology that promises enhanced piezoelectric actuator reliability dominated by material degradation.

II. PIEZOELECTRIC ACTUATOR RELIABILITY

The main failure mechanisms of lead zirconate titanate piezo-ceramics (PZTs) are micro-cracking due to overstress and fatigue degradation in the resistive and capacitive load behavior. Increased temperature and increased driving amplitudes aggravate the ongoing ceramic degradation caused by an electrochemical reaction [2]. Fatigue degradation manifests itself as a decreasing electrical load impedance (resistive and capacitive) the piezoelectric actuator exerts on the driving circuit. Fatigue and overstress can be compensated/reduced through adaptive driving of the piezoelectric actuator. The first aim is to ensure driving conditions that reduce the effects of degradation and overstress. By setting the voltage peaks in the negative and positive domain (-50 V- to 100 V) instead of higher positive domain (0 V- to 150 V), the reliability can be improved while the relative displacement per energy remains the same. Optimized power efficiency of the driver electronics can lead to reduced heat dissipation from the electronics delivered to the actuator and low driving signal ripple (<2 %) reduces the displacement jitter. Equation 1 expresses the relationship between equivalent electrical capacitance C, electric field E, and mechanical strain S of PZT PAs. In which V is the voltage drop between both PA contacts required to establish the electrical field, d and l are device parameters for piezoelectric charge constant and the actuator length. I·t is the applied current over time [3]. Fig.1 shows that the relative equivalent piezoelectric capacitor variation can be reasonable electrically compensated by driving current I_{drive} adjustments. The adaptive driving for piezo-electric compensation is achieved through active amplitude- and ramp-control (rise/fall times) implemented through programmable current-mode charging of the capacitive load. The mechanical strain S can be actively maintained to the grade of equivalent PZT PA capacitor

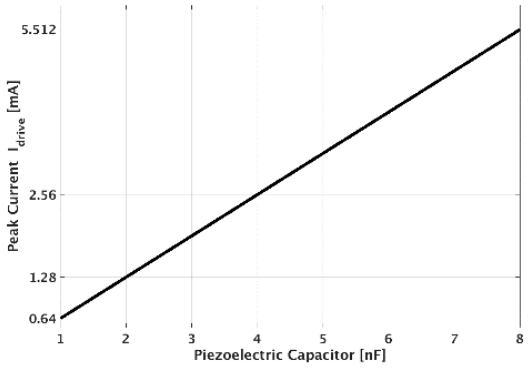

Fig.1. Required driving current for varying equivalent capacitor of the PA, based on equation 3.

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change by adjusting the driving current to equation (2) at fixed driving voltage amplitudes.

$$S = dE = d \cdot \frac{V}{l} = \frac{I \cdot t}{C} \cdot \frac{d}{l} \quad (1)$$

$$I_{drive} \rightarrow \alpha \cdot I_0 \quad (2)$$

$$\alpha = \frac{C_0 \pm C_{deg}}{C_0} \quad (3)$$

Where C_0 is the initial piezoelectric capacitance and I_0 is the resulting initial driving current calculated from (1). The parameter C_{deg} corresponds to the change of the piezoelectric capacitor. The presented actuator driver topology offers current-mode load charging with adjustable current sinks for degradation compensation based on the theory in equations (1)- to (3).

III. A NOVEL PIEZOELECTRIC ACTUATOR DRIVER TOPOLOGY

In this paper, we propose and validate a novel actuator driver topology that combines high-voltage actuator driving with piezoelectric reliability, illustrated in Fig.2. The proposed topology has been optimized for driving piezoelectric actuators in micro-pumps. These will be mainly used in battery driven applications and thus need to be optimized towards size and power consumption. In safety critical applications, like in the medical domain, it is mandatory to protect the user from any system malfunction, pump interaction and high-voltage contact.

State-of-the-art driver topologies, like the widely used full-bridge driver [4] circuit, are not appropriate for this field of application due to missing adaptability possibilities of amplitude and signal shape necessary for system reliability prescribed in Chapter II. The following chapter describes a novel driver topology consisting of high-voltage DC/DC Converter, Dual Polarity Clamp, Current-Mode Output Stage and Degradation Regulator forming the Actuator Driver optimized towards high-reliability.

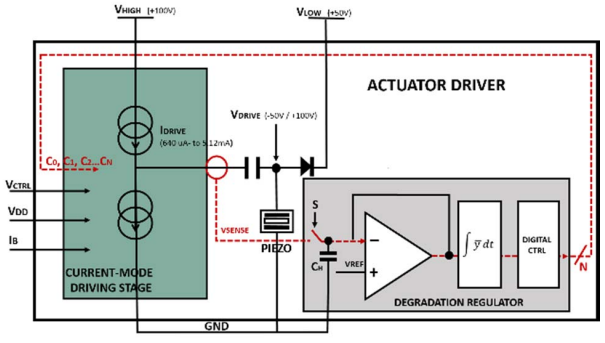

Fig.2. Actuator Driver including a Current-Mode Driving Stage and Degradation Regulator

The output waveform V_{drive} (-50V- to +100V) is generated by capacitive clamping (patent# PCT/EP2016/066134). Adaptive control over the driving current and resulting load charging rise/fall times calculated in (5) is achieved through Programmable Voltage Controlled Current Sinks that are controlled by Bits C_0-to C_2, forming the Current-Mode Output Stage

$$t_{rise/fall} \sim \frac{C_{pz} \cdot |V_{drive,hi} - V_{drive,lo}|}{I_{drive}} \quad (5)$$

Where C_{pz} is the present equivalent capacitance of the driven piezoelectric actuator, $V_{drive,hi}$ is the maximum positive polarity driving voltage amplitude, and $V_{drive,lo}$ is the maximum negative polarity driving voltage amplitude. In the Degradation Regulator, the driving voltage slope is sensed, sampled and compared to a reference signal. A following integrator generates an average slope error based on the individual slope errors during several switching periods. Finally the slope error is converted to a set of control Bits C_N that adapt the driving current to the grade of degradation. This technique promises high mechanical strain stability and overstress protection to the piezoelectric actuator. Figure 3 gives a more detailed view into the Current-Mode Output Stage that was fully integrated in a 0.35um Bulk CMOS Technology. It consists of a Current Programming Stage (CP-Stage) that sets the driving current by a certain Bit-Combination ($C_0C_1C_2$) controlled through the Degradation Regulator output. The CP-Stage can be flexibly extended to the required current resolution. Furthermore, the output stage includes a High-Voltage Current-Mode Output Stage (HVC-Stage) that sources/sinks the previously set driving current to the output node while switching the output between V_{high} and ground level. The HVC-Stage is biased by the Driver-Ctrl-Stage that decides about the direction of output current flowing (Sourcing or Sinking) depending on the polarity of the driving voltage amplitude. This work presents the first steps towards a fully integrated system aiming for piezoelectric degradation detection and resulting driving signal self-regulation. On the fabricated Testchip MAGNOLIAA0, illustrated as block level schematic in Fig.4, an Asynchronous Boost Converter that operates in discontinuous conduction mode (DCM) uses an integrated programmable inductor-current sense circuitry implemented by a SenseFET-

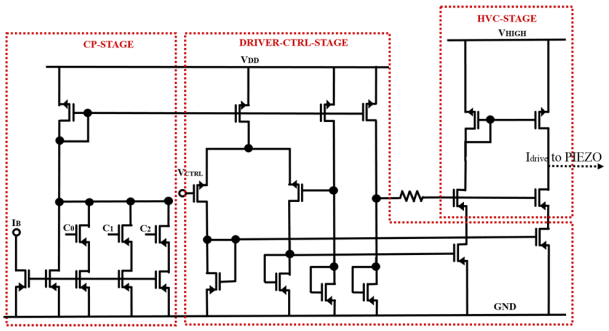

Fig.3. Programmable Current-Mode Driving Stage controlled by the Degradation Regulator

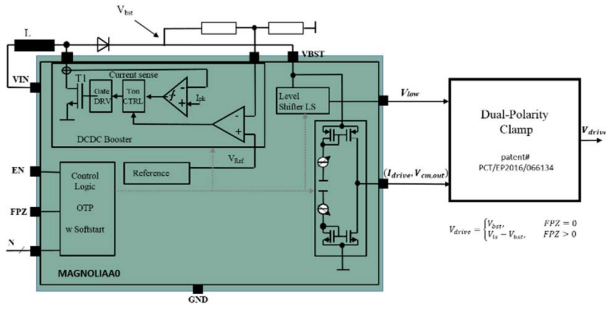

Fig. 4 MAGNOLIAA0 Block Level Schematic

technique. The high-voltage booster output voltage V_{bst} is used to supply the Programmable Current-mode Output Stage and the Level Shifter. This Level Shifter provides a second, lower level power supply V_{ls}. The Input Signal FPZ decides about the switching frequency of the driving voltage and therefore the displacement direction of the piezoelectric actuator. In the patented Dual-Polarity Clamp, the deviation between V_{bst} and V_{ls} defines the voltage levels generated to

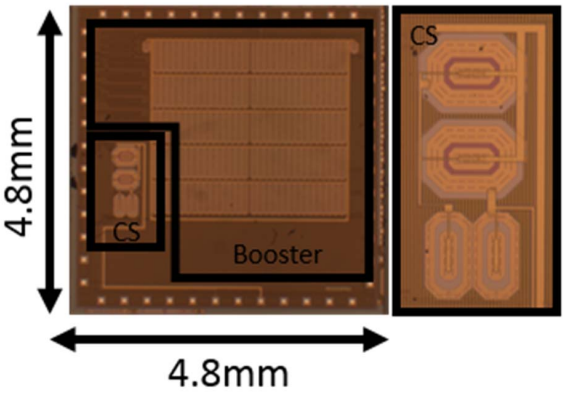

Fig. 5 MAGNOLIAA0 (left side) with detailed view to the fully integrated Programmable Current-Mode Output Stage (right side).

drive the piezoelectric actuator. as given in

$$V_{drive} = \begin{cases} V_{ls} - V_{bst} & FPZ > 0 \\ V_{bst} & FPZ = 0 \end{cases} \quad (4)$$

IV. Results

A Testbench for the MAGNOLIAA0 Testchip in Fig.5 was set up using a 5 V supply, 2 nF equivalent piezo-capacitor and a FPZ frequency of 100 Hz. The typical set of waveforms is shown in Fig.6 demonstrating the adaptable voltage amplitudes +/-10 %. The waveforms have been simulated in nominal case under room temperature conditions, for an equivalent 1.8 nF-to 2.2 nF piezoelectric capacitor and constant rise/fall times. The output amplitude reaches an accuracy of <2 % after a start-up settling time of around

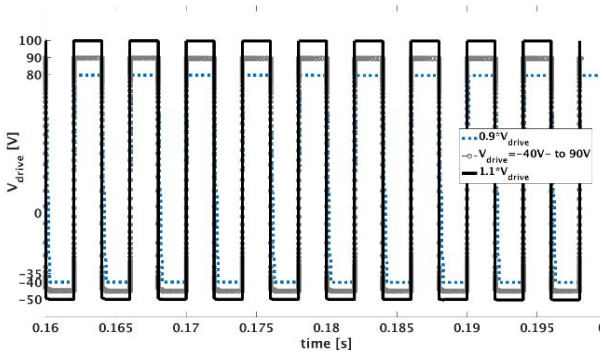

Fig.6 Adaptable driving voltage V_{pzt} with +/-10/ amplitude variation

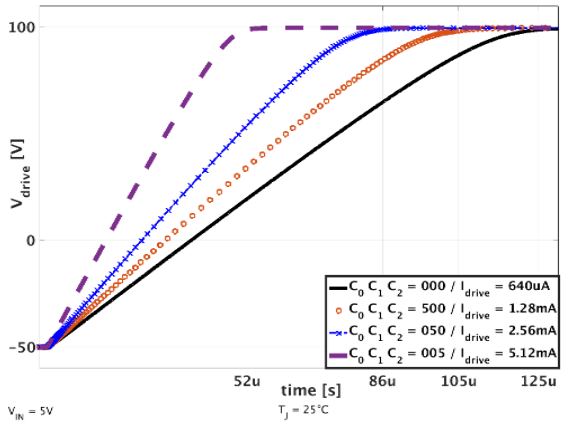

Fig. 7 Verified piezoelectric actuator charging through current mode output stage for different Programming bit combinations

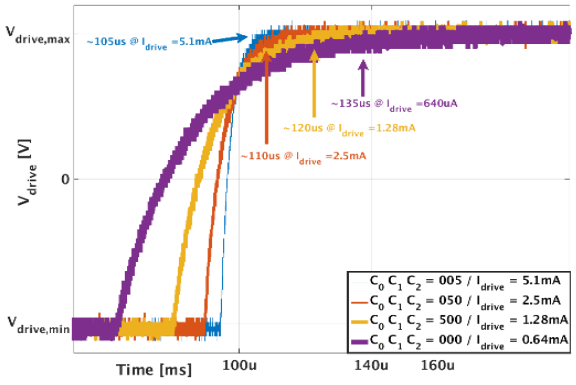

Fig. 8 Measured driving voltage through current charging for different Programming bit combinations

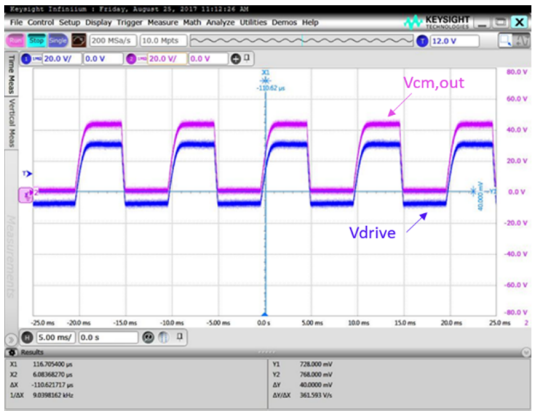

Fig. 9 Oscilloscope screenshot demonstrating the level shift between driving voltage (V_{drive}) generated from Current-Mode Output Stage and voltage applied to piezoelectric Actuator (V_{pzt}) generated through the Dual Polarity Clamp

50 ms. Fig. 7 and 8 illustrate the controllable rising slope of the driving voltage depending on the programmable driving current amplitude, verified by simulation (Fig.7) and proven by measurement (Fig.8). Simulation and Measurement have been performed under room temperature conditions. Fig.9 shows the level shifted voltage applied to the piezoelectric actuator (V_{drive}) compared to the voltage generated by the Current-Mode Output Stage ($V_{cm,out}$). Both the concepts of current-mode driving and capacitive dual-polarity voltage clamping have been proven by measurement. The circuit therefore allows a high grade of adaptability in terms of driving voltage (negative and positive amplitudes) and driving current setting.

V. Conclusion

A novel high-voltage actuator driver has been presented that offers the flexibility to drive a wide range of piezoelectric actuators (2nF- to 68nF) by adaptive (640uA- to 5.12mA), self-regulating current-mode driving for high-voltage waveforms (-50V- to +100V).

The actuator driver topology consists of a fully integrated Programmable Current Mode Output Stage in a 0.35um Technology followed by a Degradation Regulator that measures the grade of piezoelectric degradation and feds this information back to the output stage where it is reflected as a change in the driving current. The circuit is supplied through On-Chip Dual-Polarity High-Voltage Generation. The presented technique promises stable strain performance, protection from electrical overstress and extension of the piezoelectric actuator lifetime through early breakdown avoidance.

TABLE I: Performance summary and comparison

	[5]	This Work
Technology	0.18 um	0.35 um
Load Type	Haptic Actuator	Micro-pump
Capacitive Load	94 nF	≤10 nF
Package	QFN 4x4 mm	QFN 7x7mm
Input Voltage	3.6 V	2.5 V-to 6 V
Frequency	150 Hz	50 Hz-to 1 kHz
Output Voltage Vpp	100 V	150 V
Power	32.47 mW	64 mW@640 uA load current
Number of Core HV Power Devices	12	5

The next step concerning the driver development will be the full integration of the degradation regulation and long term reliability testing using the novel current-mode driving technique.

Acknowledgement

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