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# Impact of Height of Silicon Pillar on Vertical DG-MOSFET Device

**Authors :** Khairil Ezwan Kaharudin, Abdul Hamid Hamidon, Fauziyah Salehuddin

**Abstract :** Vertical Double Gate (DG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is believed to suppress various short channel effect problems. The gate to channel coupling in vertical DG-MOSFET are doubled, thus resulting in higher current density. By having two gates, both gates are able to control the channel from both sides and possess better electrostatic control over the channel. In order to ensure that the transistor possess a superb turn-off characteristic, the subs-threshold swing (SS) must be kept at minimum value (60-90mV/dec). By utilizing SILVACO TCAD software, an n-channel vertical DG-MOSFET was successfully designed while keeping the sub-threshold swing (SS) value as minimum as possible. From the observation made, the value of sub-threshold swing (SS) was able to be varied by adjusting the height of the silicon pillar. The minimum value of sub-threshold swing (SS) was found to be 64.7mV/dec with threshold voltage (VTH) of 0.895V. The ideal height of the vertical DG-MOSFET pillar was found to be at 0.265 µm.

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