PHOTONICS RESEARCH GROUP

TRANSFER PRINTING FOR HETEROGENEOUS SILICON PICs

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SILICON PHOTONICS FOR SMART MICROSYSTEMS

1. **photonic integration:** Build photonic systems on a chip
2. **silicon photonics :** Use the power of silicon CMOS-technology for integrated photonics
3. **heterogeneous integration :** Avoid the limitations of silicon through combination with other materials
4. **enable a variety of applications**
   - Core and access telecom networks
   - Optical interconnect and high performance computing
   - Sensors and biosensors
   - Biomedical instrumentation

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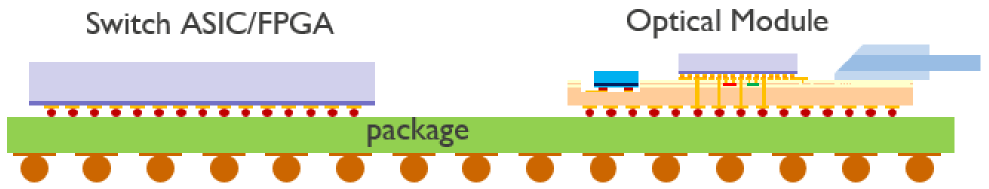
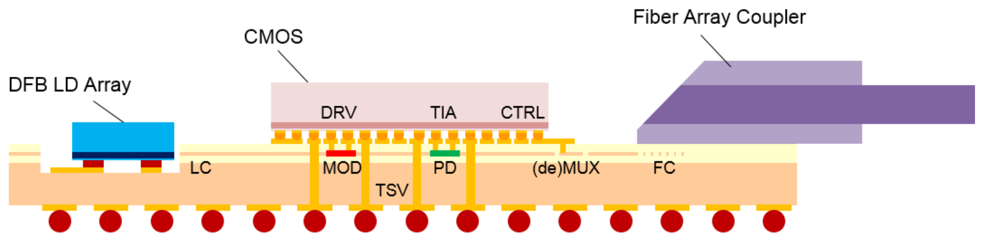
SILICON PHOTONICS FOR SMART MICROSYSTEMS – OPTICAL I/O

Cross-section



Optical Module



Light source

Modulator

Transport medium

Photodetector

DFB LD Array	Laser array
LC	Light coupler
MOD	Modulator
PD	Photodetector
(de)MUX	(de)Multiplexer
FC	Fiber coupler
TSV	Through Silicon Vias
DRV	Electrical driver
TIA	Transimpedance Amplifier
CTRL	Controller circuit

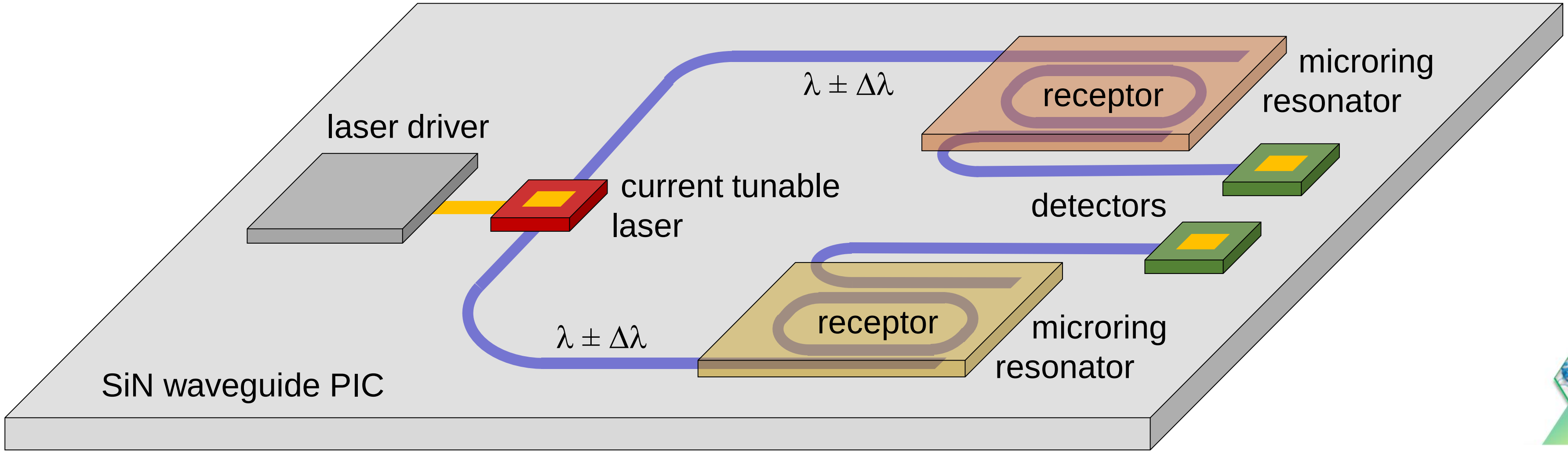
Michal Rakowski, Silicon Photonics Platform for 50G Optical Interconnects, In Photonics Summit and Workshop 2017.

SILICON PHOTONICS FOR SMART MICROSYSTEMS – SENSORS

The H2020 PIX4Life project:

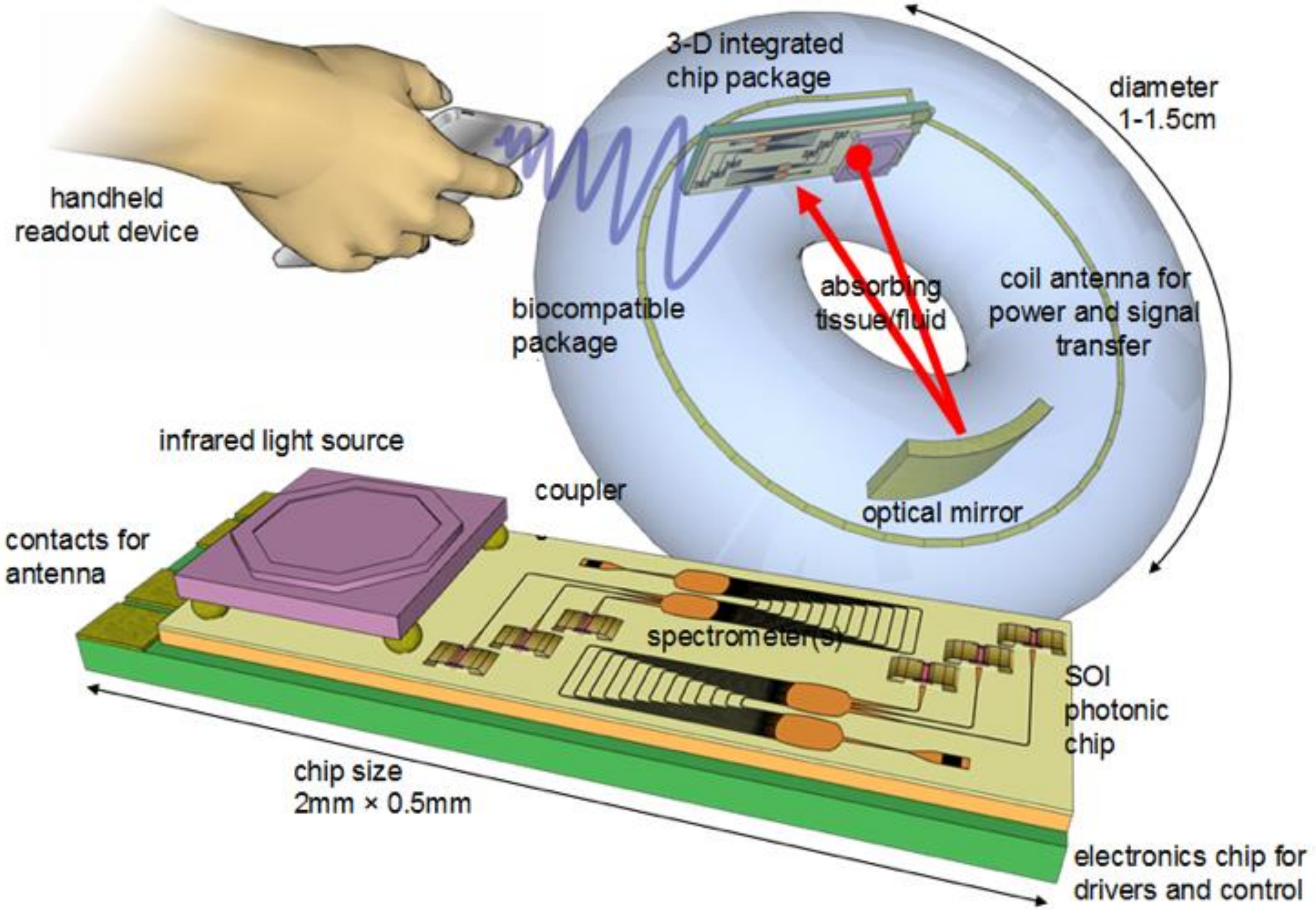
- Establishing a PIC pilot-line for life science applications in the VIS and VNIR (400 – 850 nm)
- Silicon photonics PICs with silicon nitride (SiN) WGs
- Light source integration

Multi-DoF (degree of freedom) sensor on chip

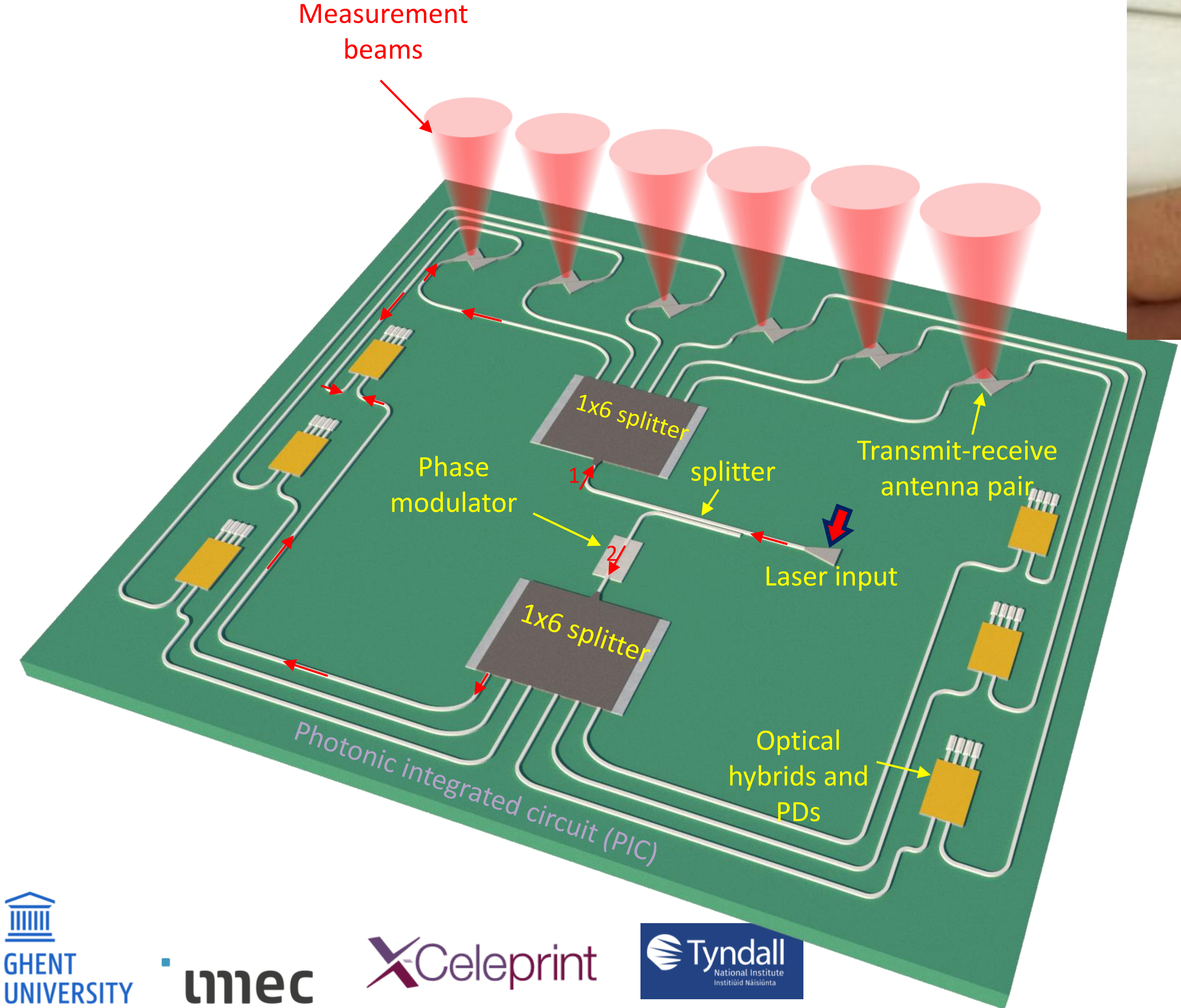


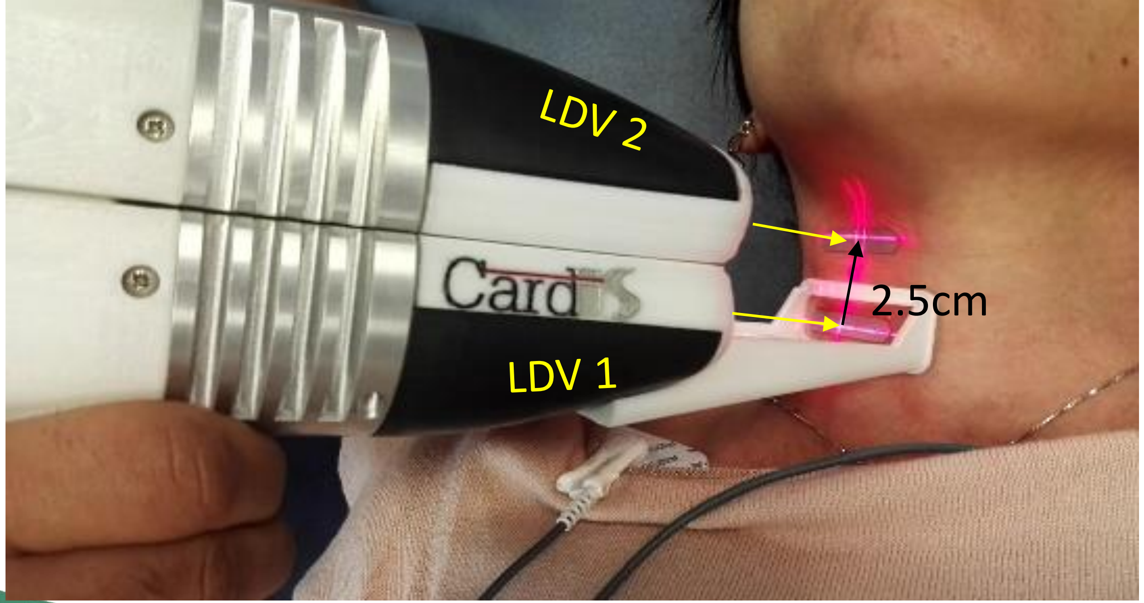
SILICON PHOTONICS FOR SMART MICROSYSTEMS – SENSORS

Implants for Continuous Glucose Monitoring



LASER DOPPLER VIBROMETER





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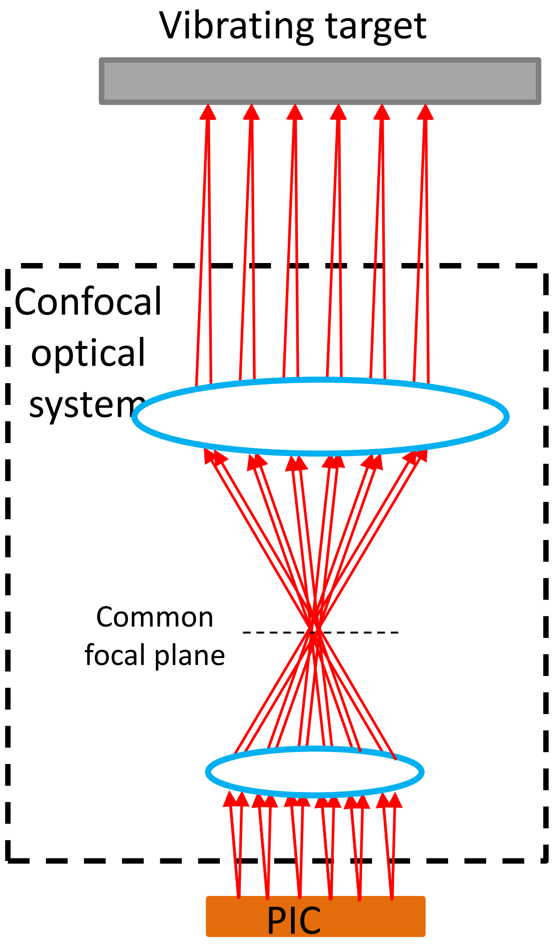
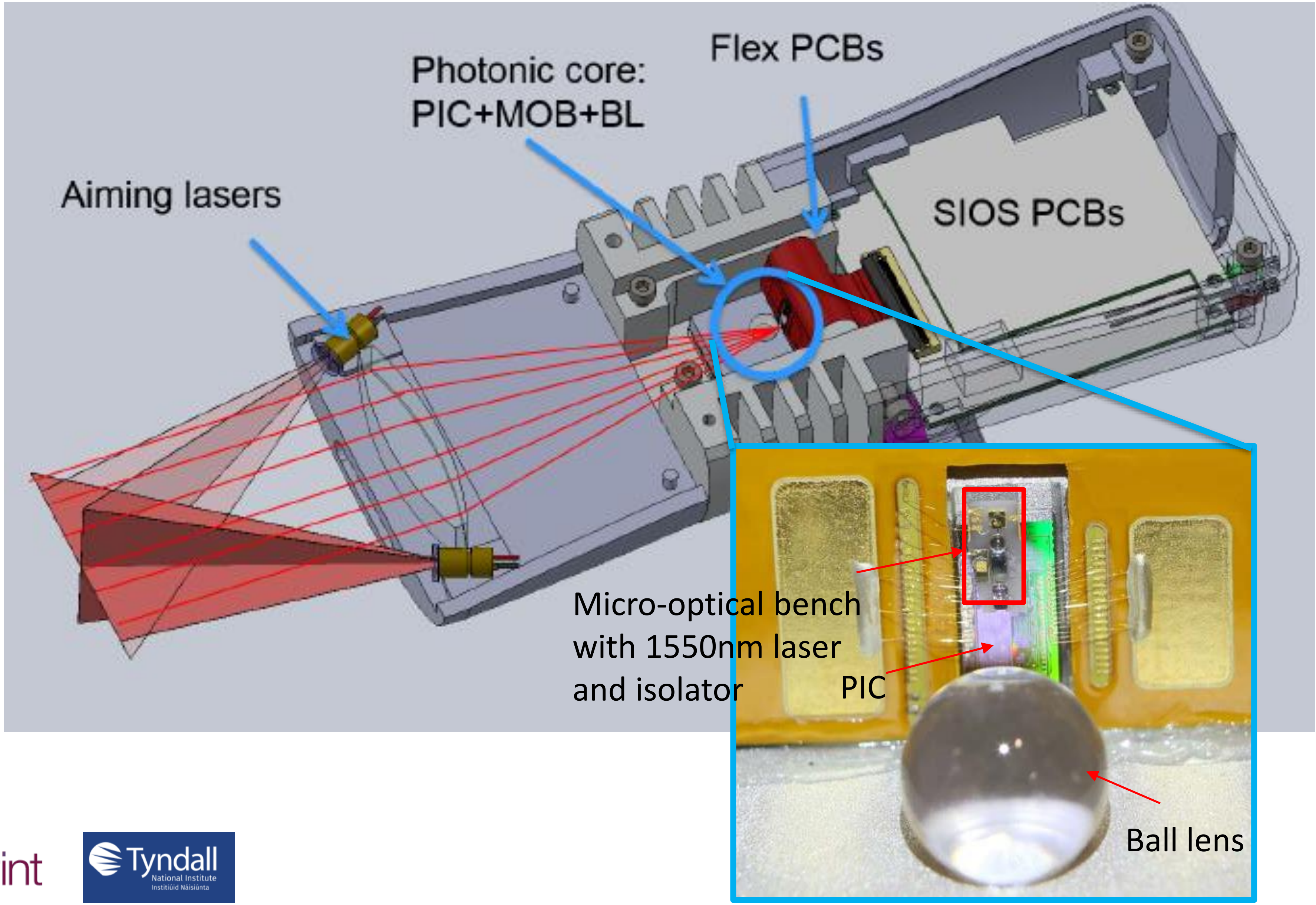
LDV-MEASUREMENT OF BLOOD PULSE VELOCITY



PIC and external optics



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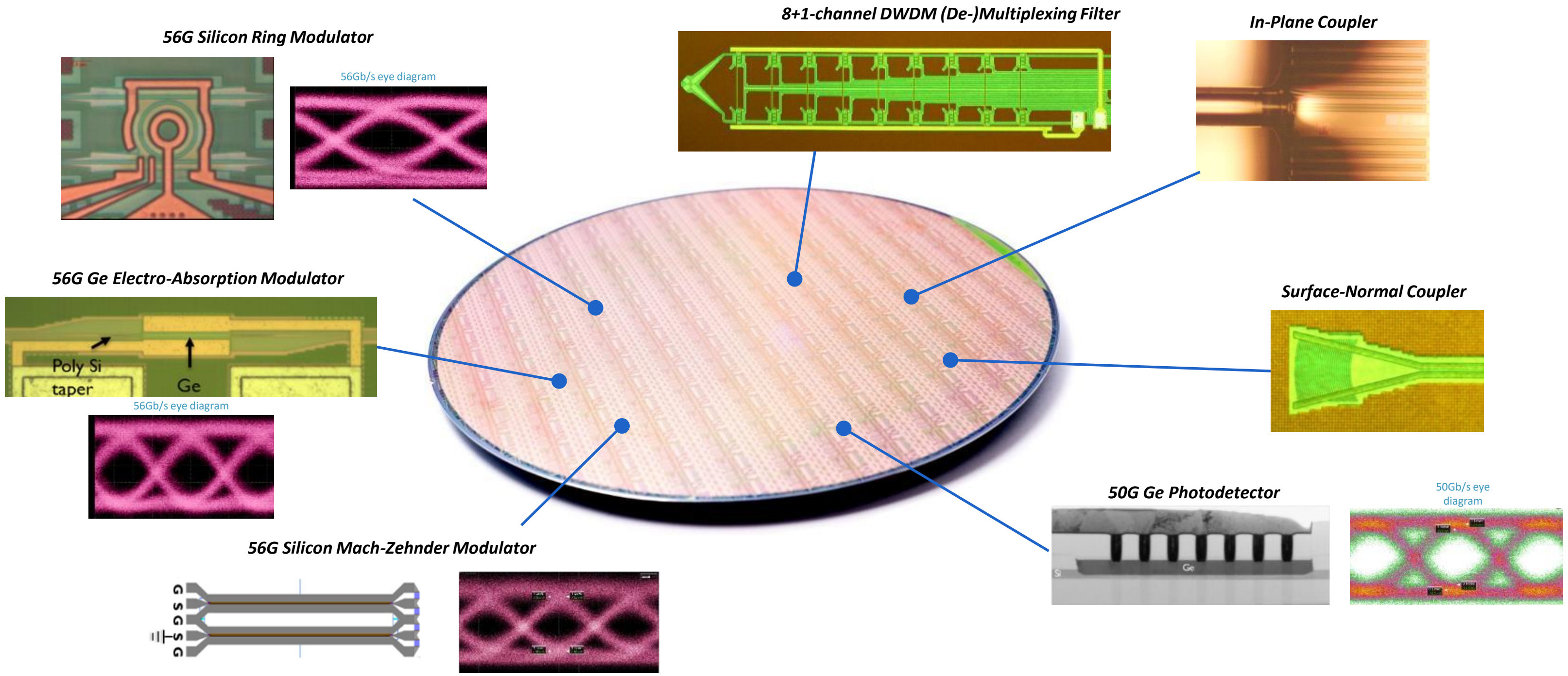
IMEC STATE-OF-THE-ART SILICON PHOTONICS PLATFORM

FULLY INTEGRATED SI PHOTONICS TECHNOLOGY



Co-integration of the various building blocks in a single platform

Today available on 200mm wafer size

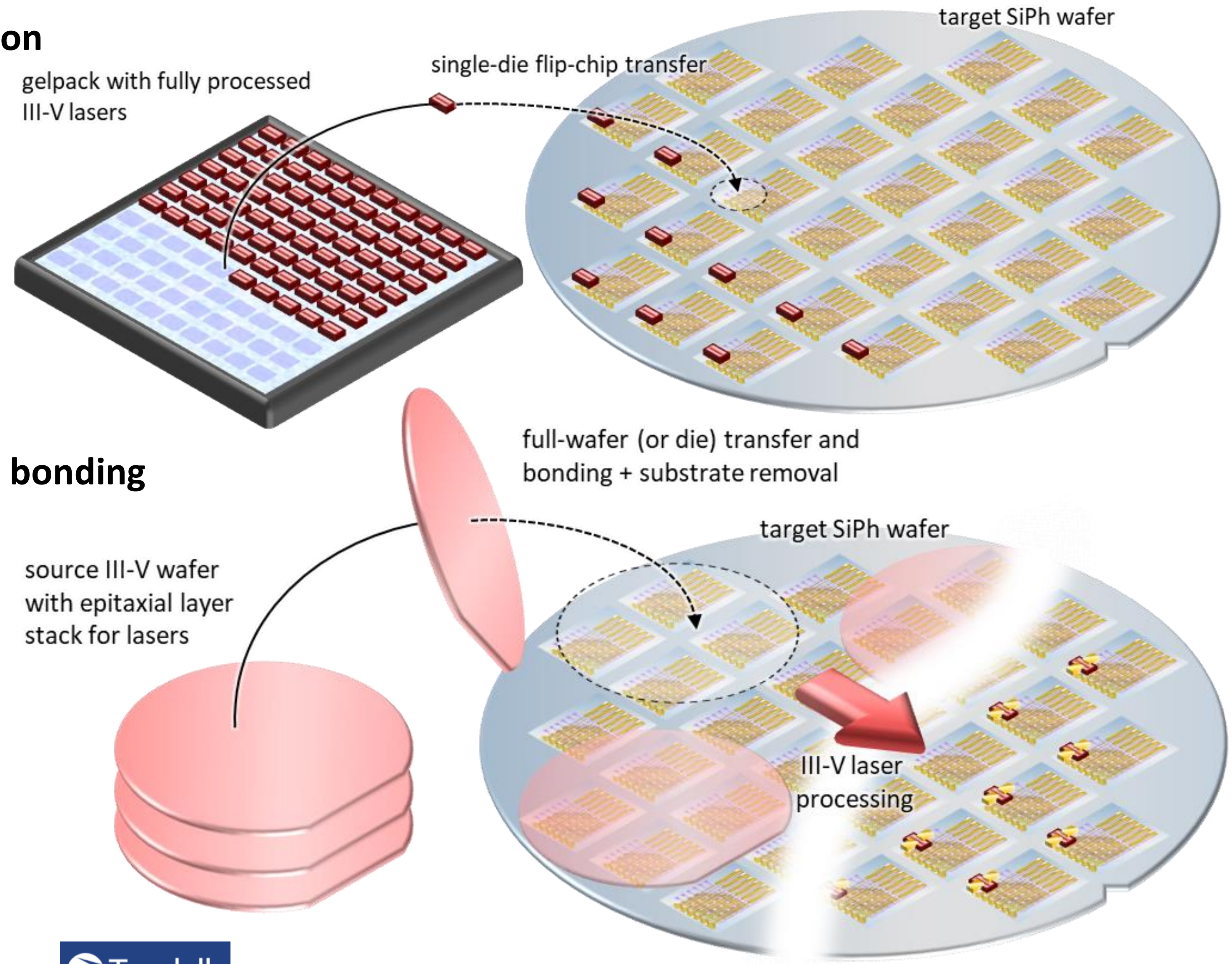
95% compatible with CMOS130 in commercial foundries

No integrated laser source => **need for a III-V/silicon photonic integration platform**

ESTABLISHED III-V-ON-SILICON TECHNOLOGIES

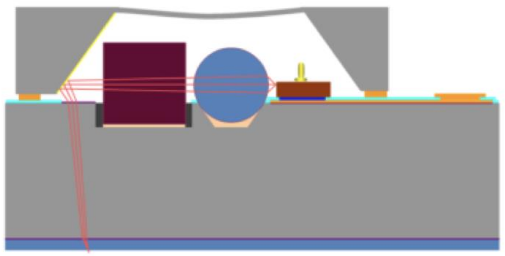
Flip-chip integration

III-V/silicon wafer bonding



ESTABLISHED III-V-ON-SILICON TECHNOLOGIES

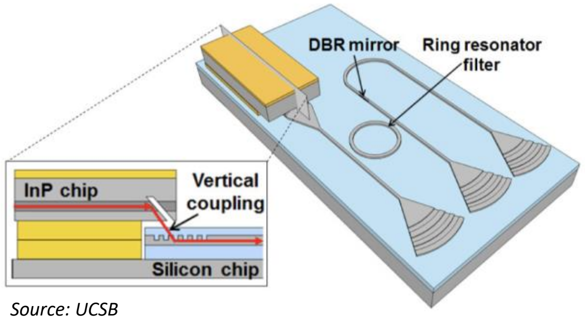
LaMP



Source: Luxtera

Use mature III-V technology
Fairly efficient optical coupling
No waveguide-in / waveguide-out devices
Wafer level assembly, packaging, test and burn-in
Sequential population of SiPh wafer
Currently only single wavelength lasers
Can be integrated on back-end stack

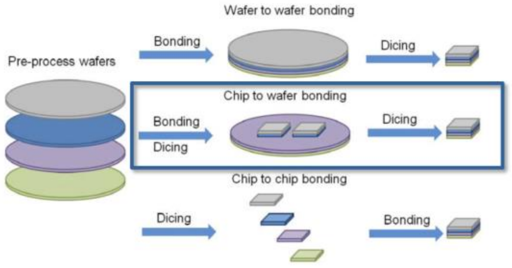
Flip-chip integration



Source: UCSB

Use mature III-V technology -> SSC
Fairly efficient optical coupling
Waveguide in-out devices possible (SOA)
Wafer-level test and burn-in on source
Sequential population of SiPh wafer
Advanced laser sources can be realized
Requires local back-end removal

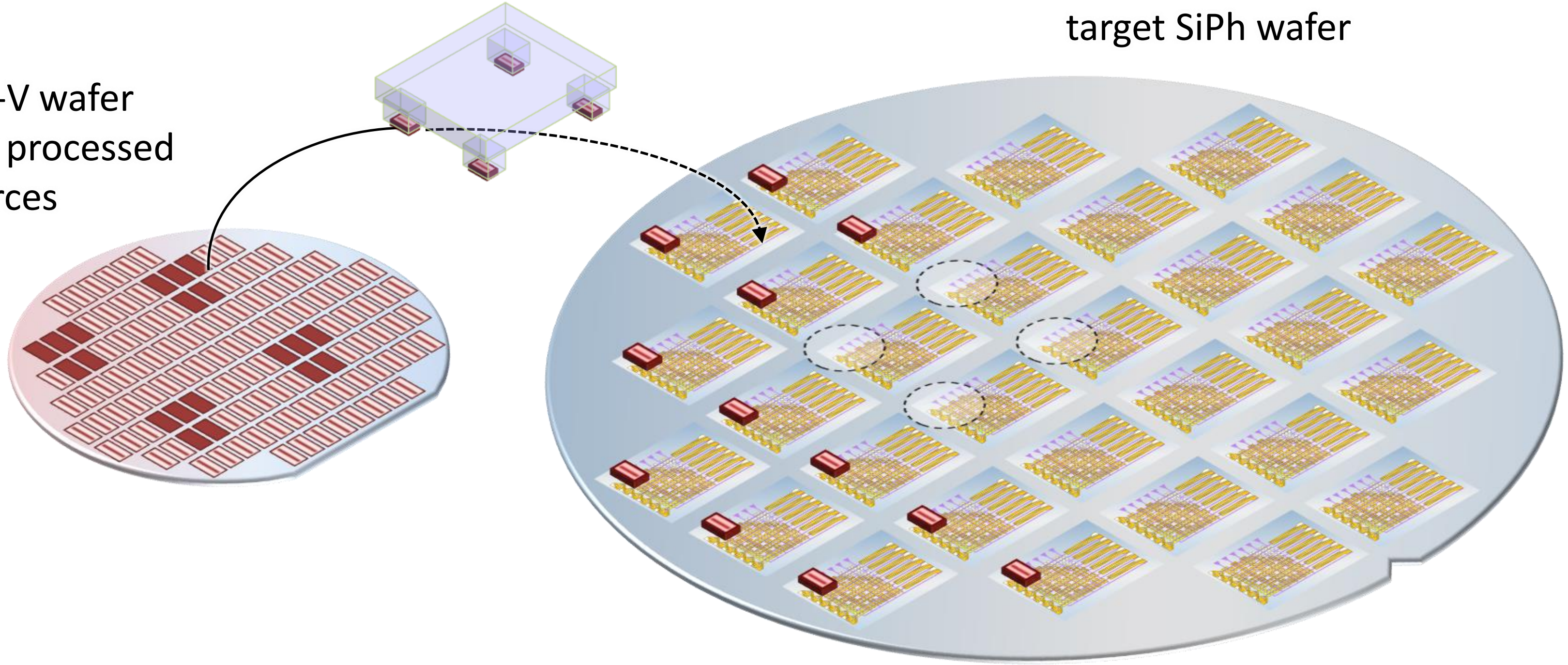
Die-to-wafer bonding



Source: Nanyang Technological University, Singapore

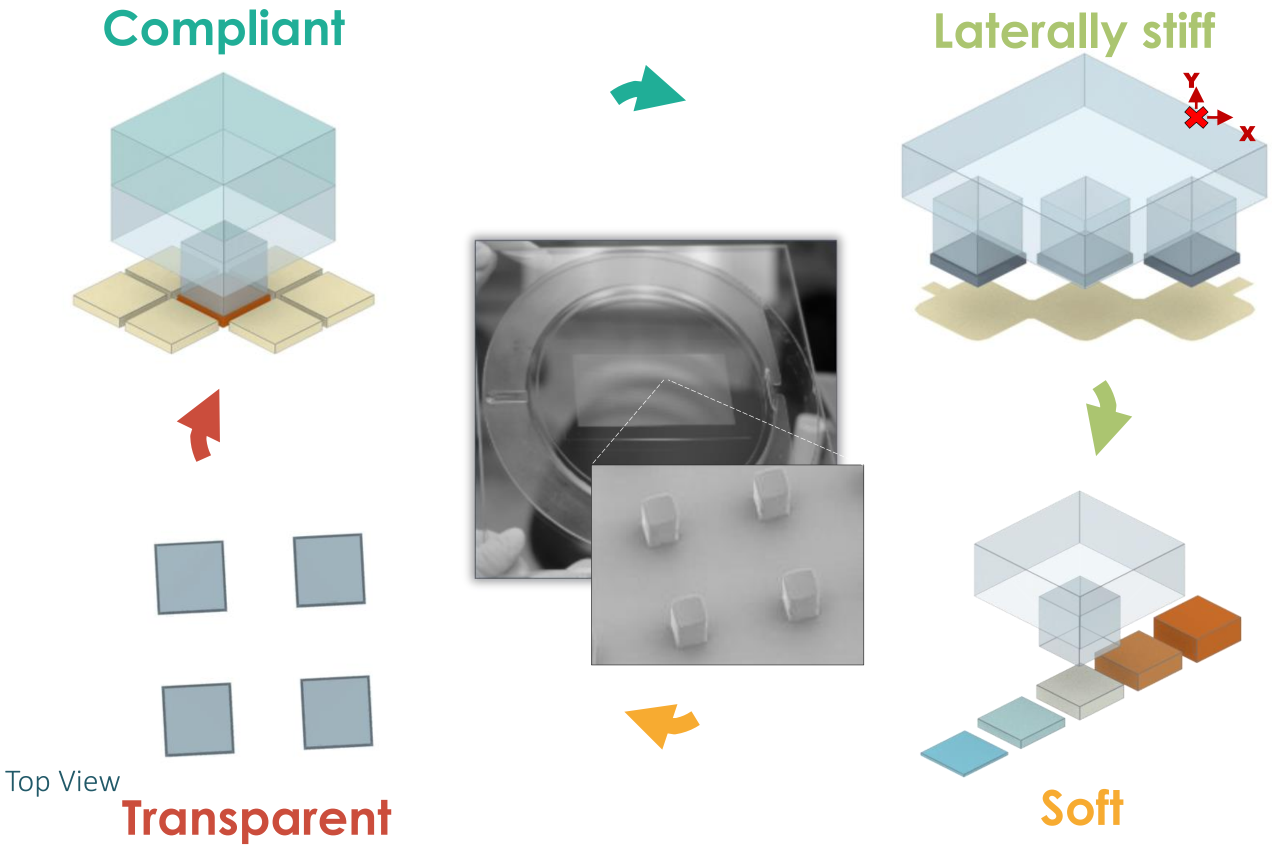
III-V processing on target wafer
Efficient optical coupling
Waveguide in-out devices (SOA)
Wafer-level test and burn-in on target wafer
Parallel processing of devices
Advanced laser sources
Requires large area back-end removal

MICRO-TRANSFER-PRINTING



µTP combines advantages of flip-chip and die-to-wafer bonding

MASS TRANSFER WITH ELASTOMER STAMPS



Compliant

Laterally stiff

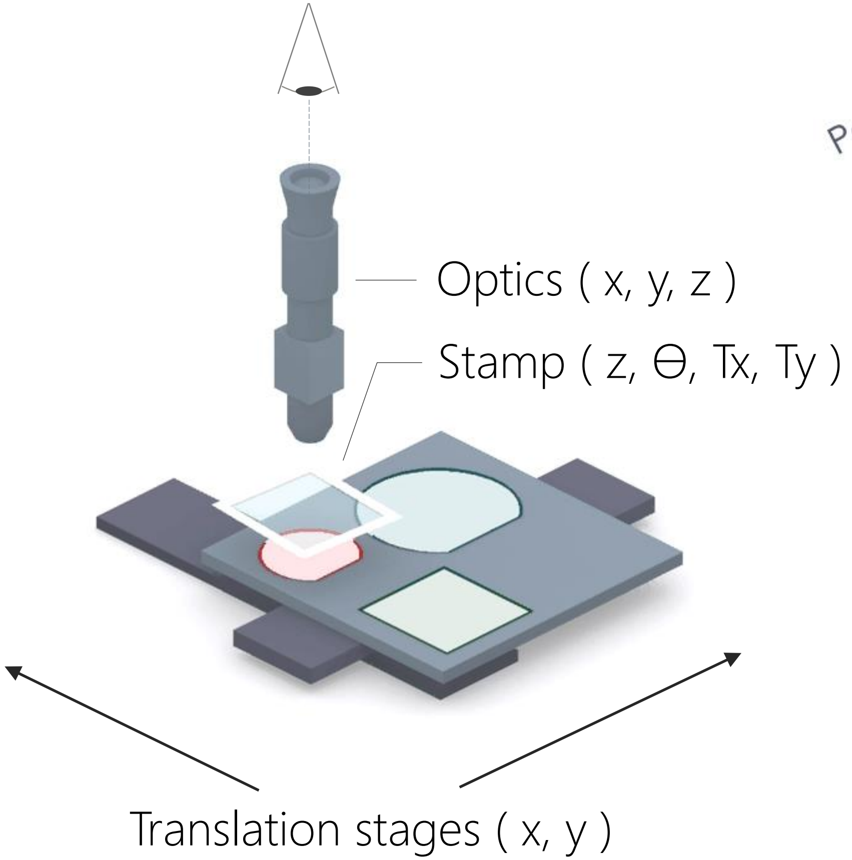
Soft

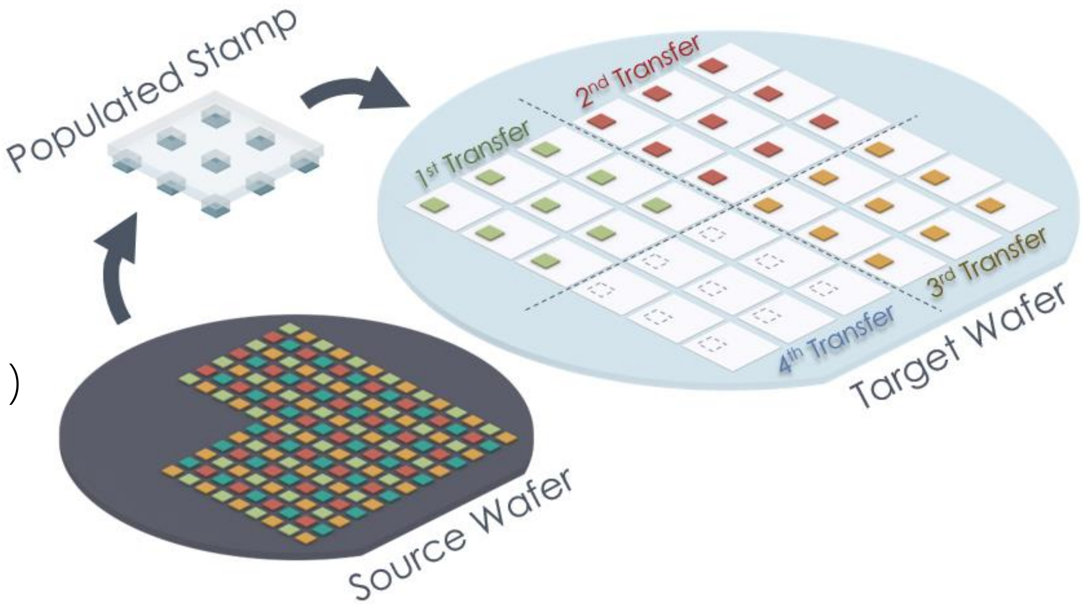
Transparent

Top View

MICRO-TRANSFER-PRINTING

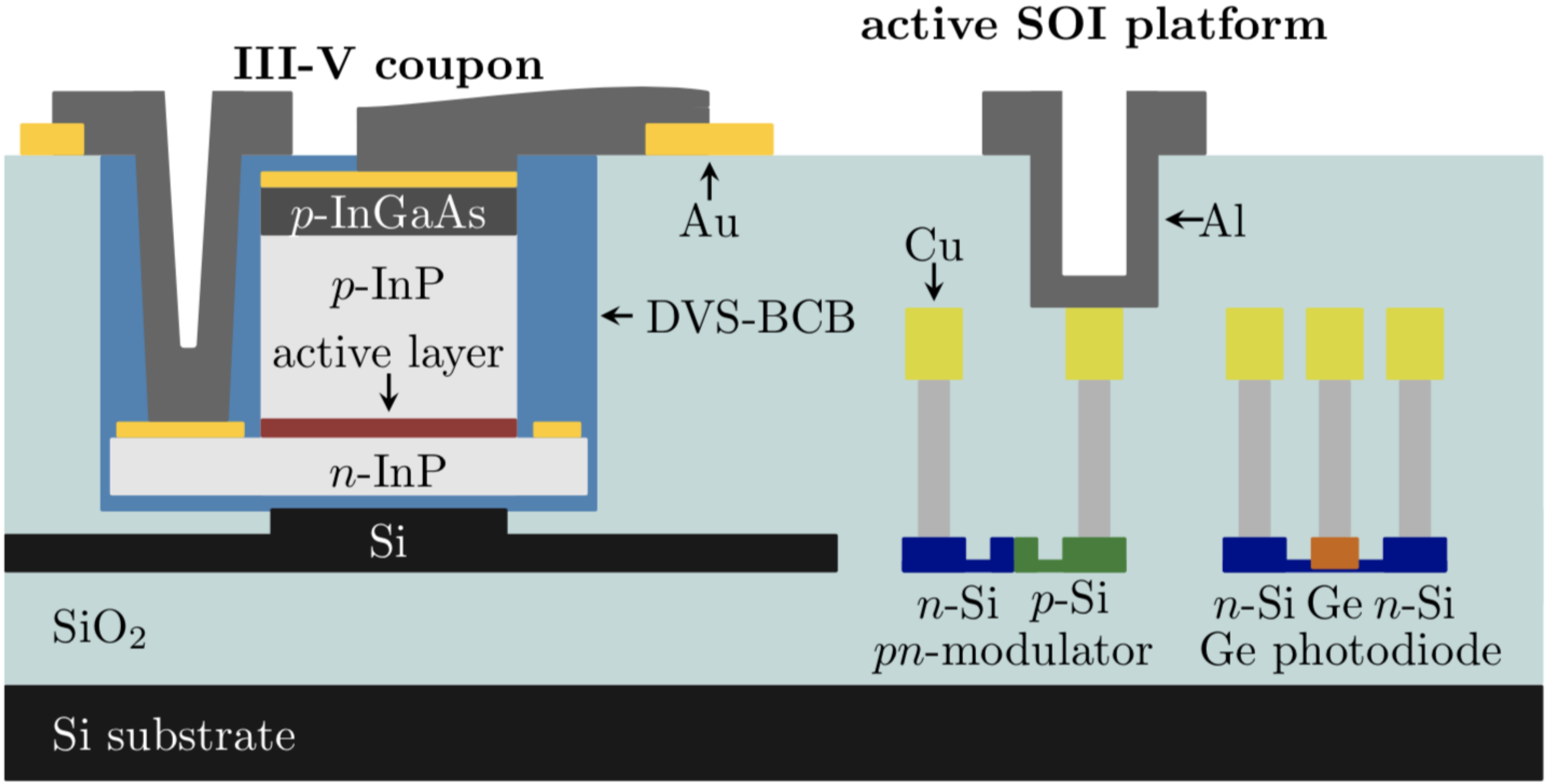
Stamp + Motion + Optics





Mature InP processing
Efficient optical coupling possible
Waveguide in-out devices (SOA)
Wafer-level test on source wafer
Parallel assembly of devices
Advanced laser sources
Requires local back-end removal

MICRO-TRANSFER-PRINTING



CHARACTERISTICS OF MICRO-TRANSFER PRINTING

Massively parallel

- >10,000 devices (LEDs) transferred per 45s cycle demonstrated
- *Flip chip transfers individual devices.*

Position tolerance of ±1.5μm at 3σ in large arrays

- ±0.5μm and better when printed in small arrays
- Pattern recognition based

The highest quality source materials used

- Can be pre-processed

Different types of devices or materials can be printed close to each other

Efficient use of expensive materials

- Width of devices << conventional for higher packing
- Substrate can potentially be recovered

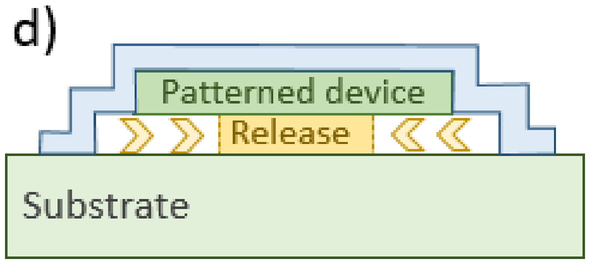
Independent of source substrate diameter

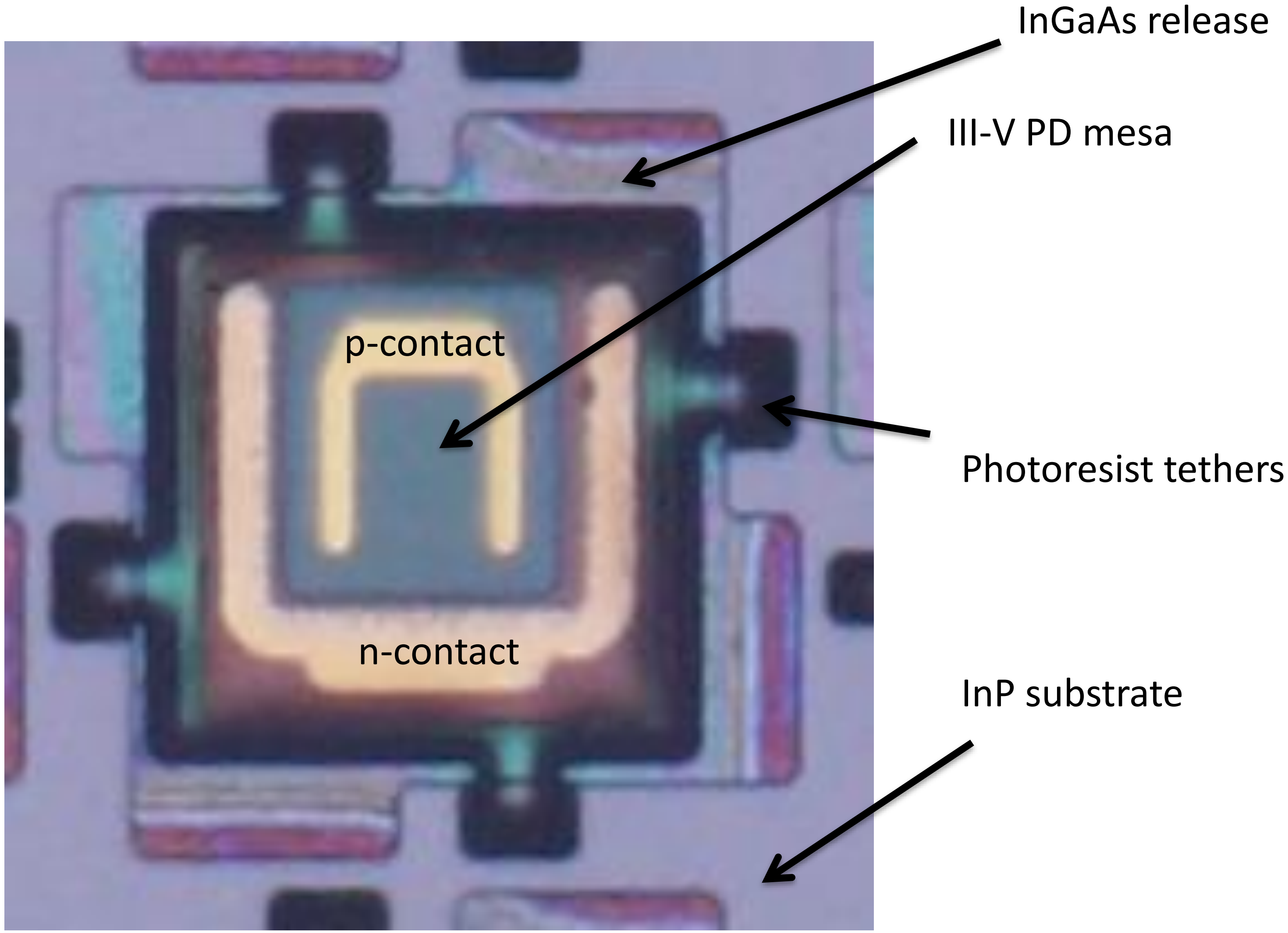
- InP wafers 50-100mm; Si wafers 200-300mm diameter

OUTLINE

- Introduction to micro-transfer-printing technology
- **Examples of III-V on Si micro-transfer-printing**
  - **Substrate-illuminated InP PDs on full platform SOI**
  - **InP widely tunable lasers on passive SOI**
- Examples of Si on Si micro-transfer-printing
- Outlook & conclusions

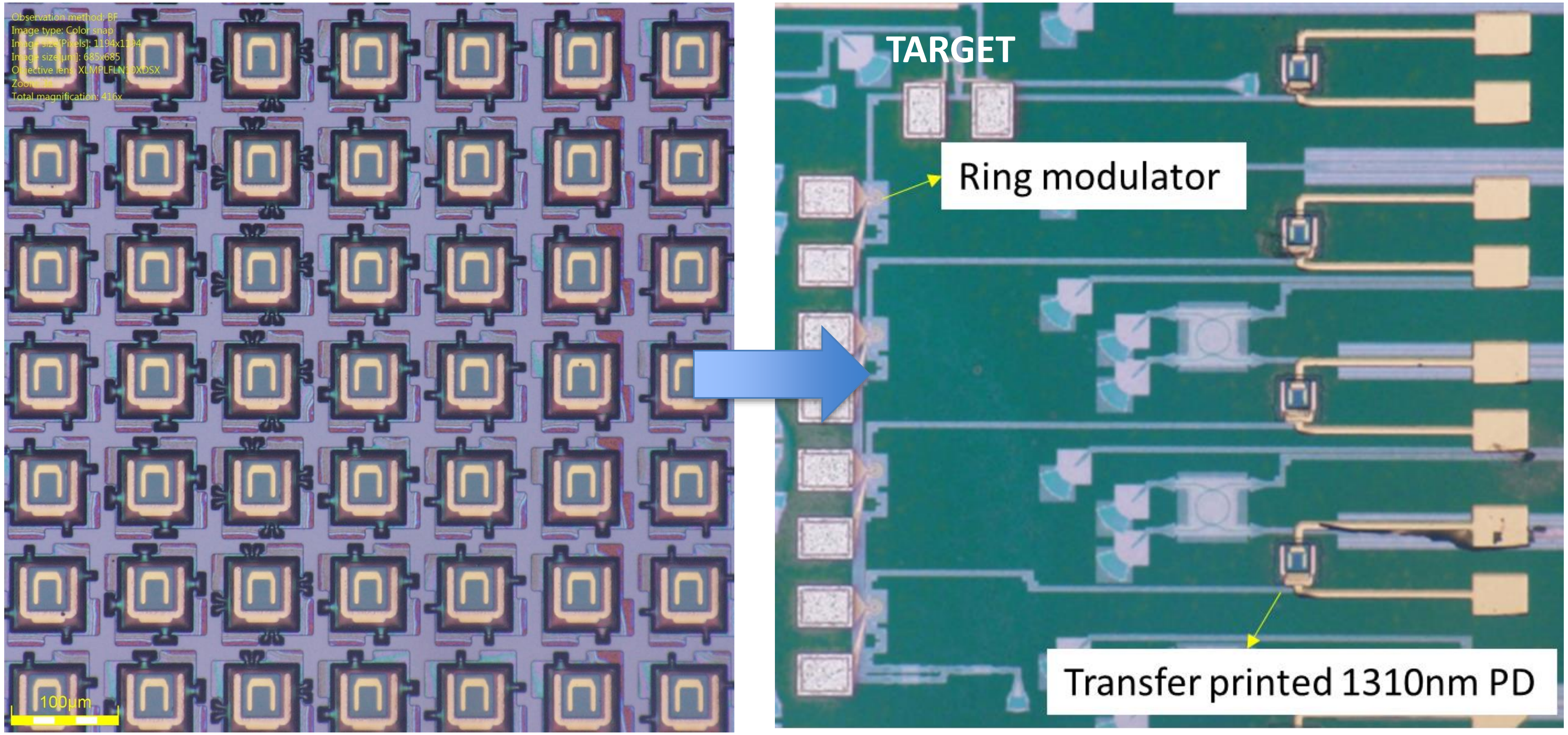
SUBSTRATE-ILLUMINATED INP PDS





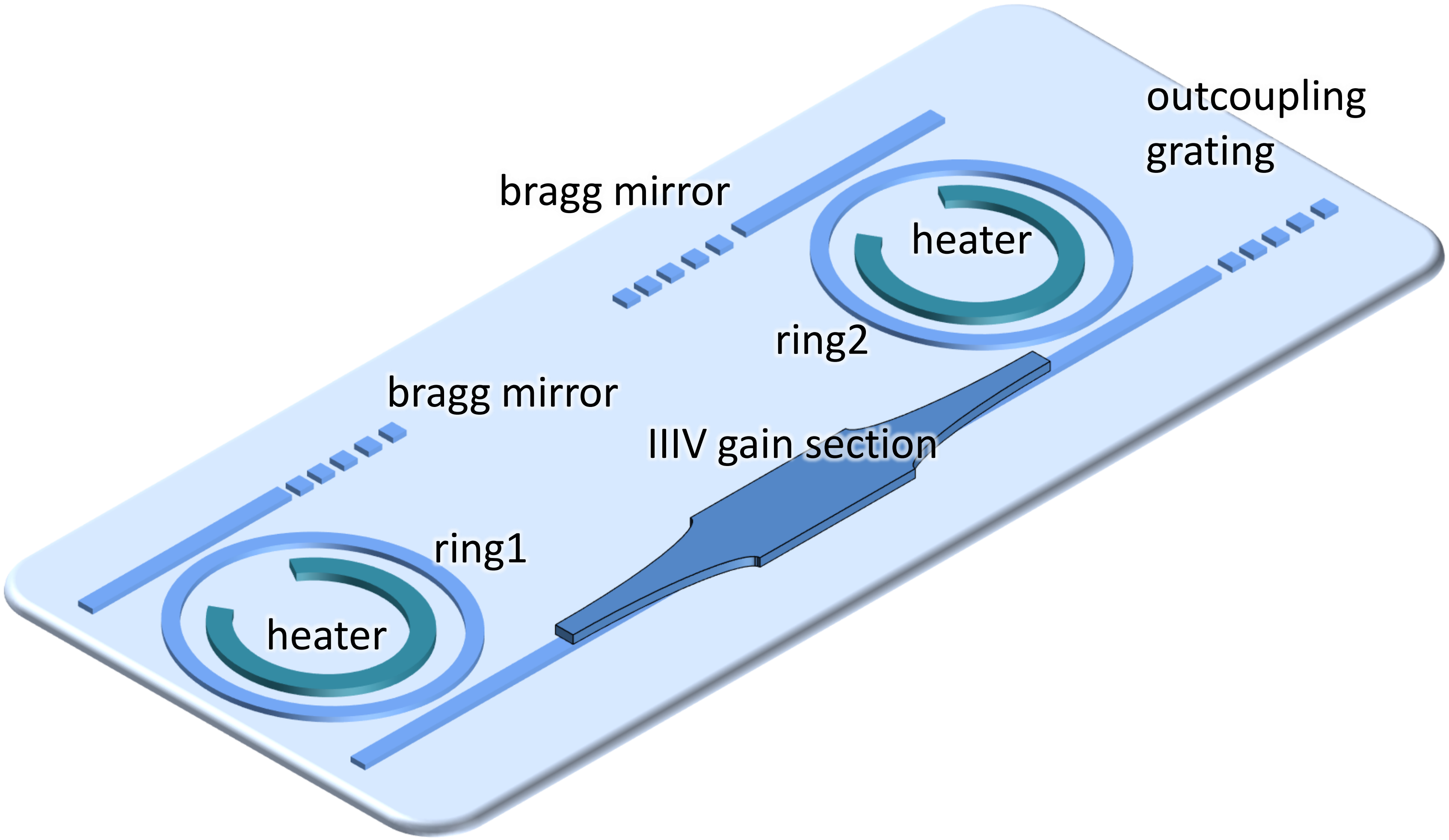
4x10Gbps III-V/Si TRANSCEIVER

III-V SOURCE WAFER **SiPh TARGET WAFER**



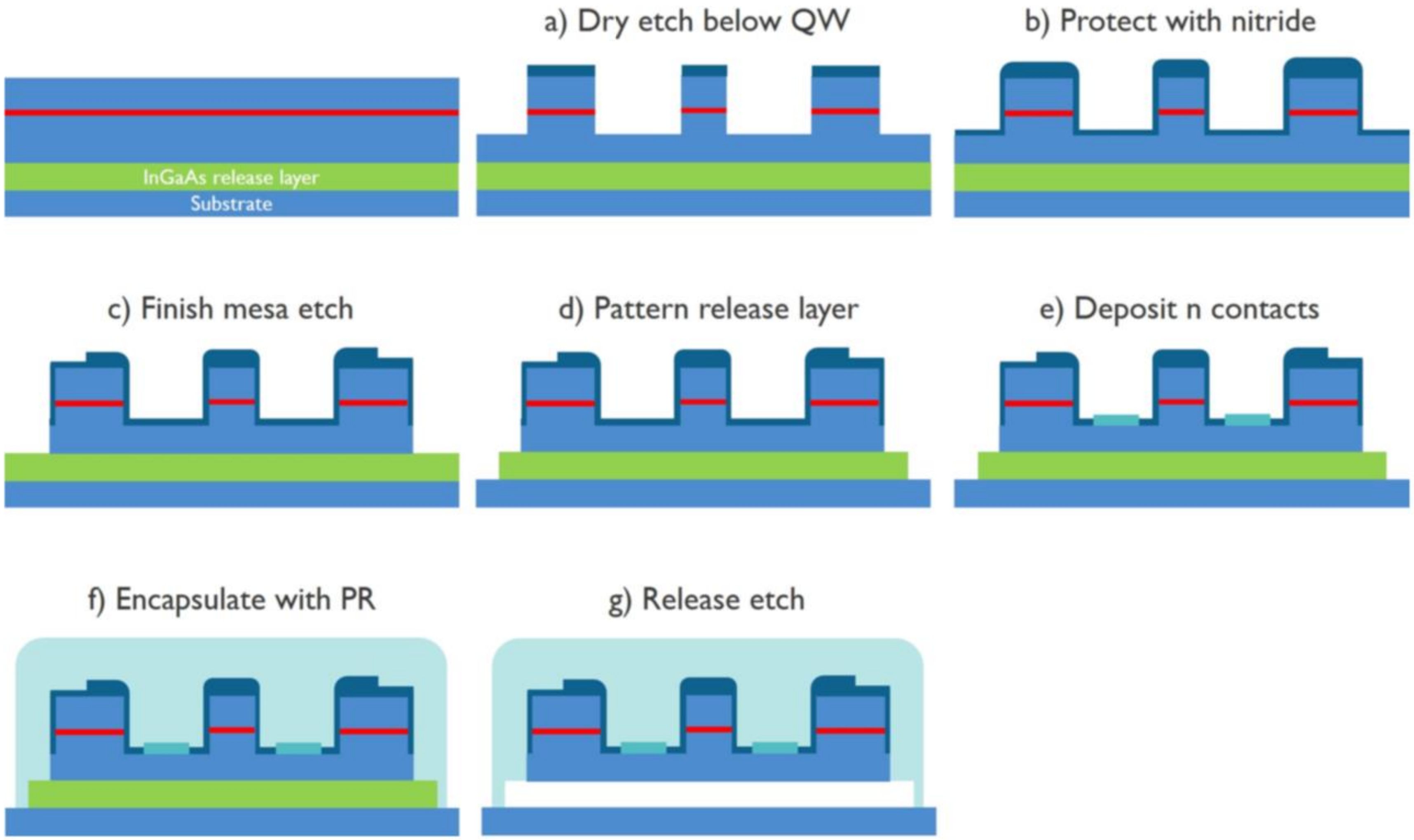
[J. Zhang et al., OE 2017]

HETEROGENEOUSLY INTEGRATED LASERS

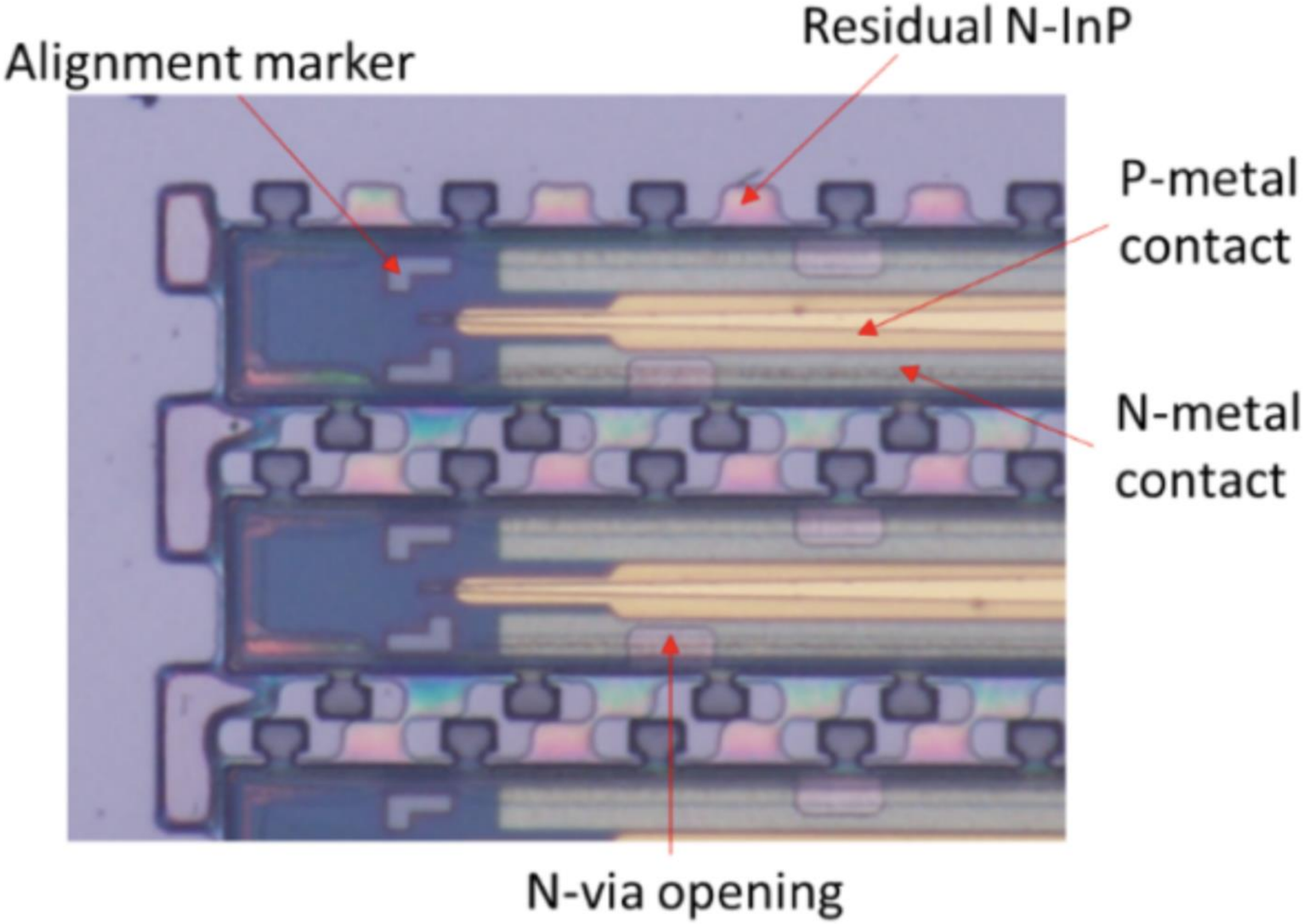


Can be realized both using wafer bonding and transfer printing

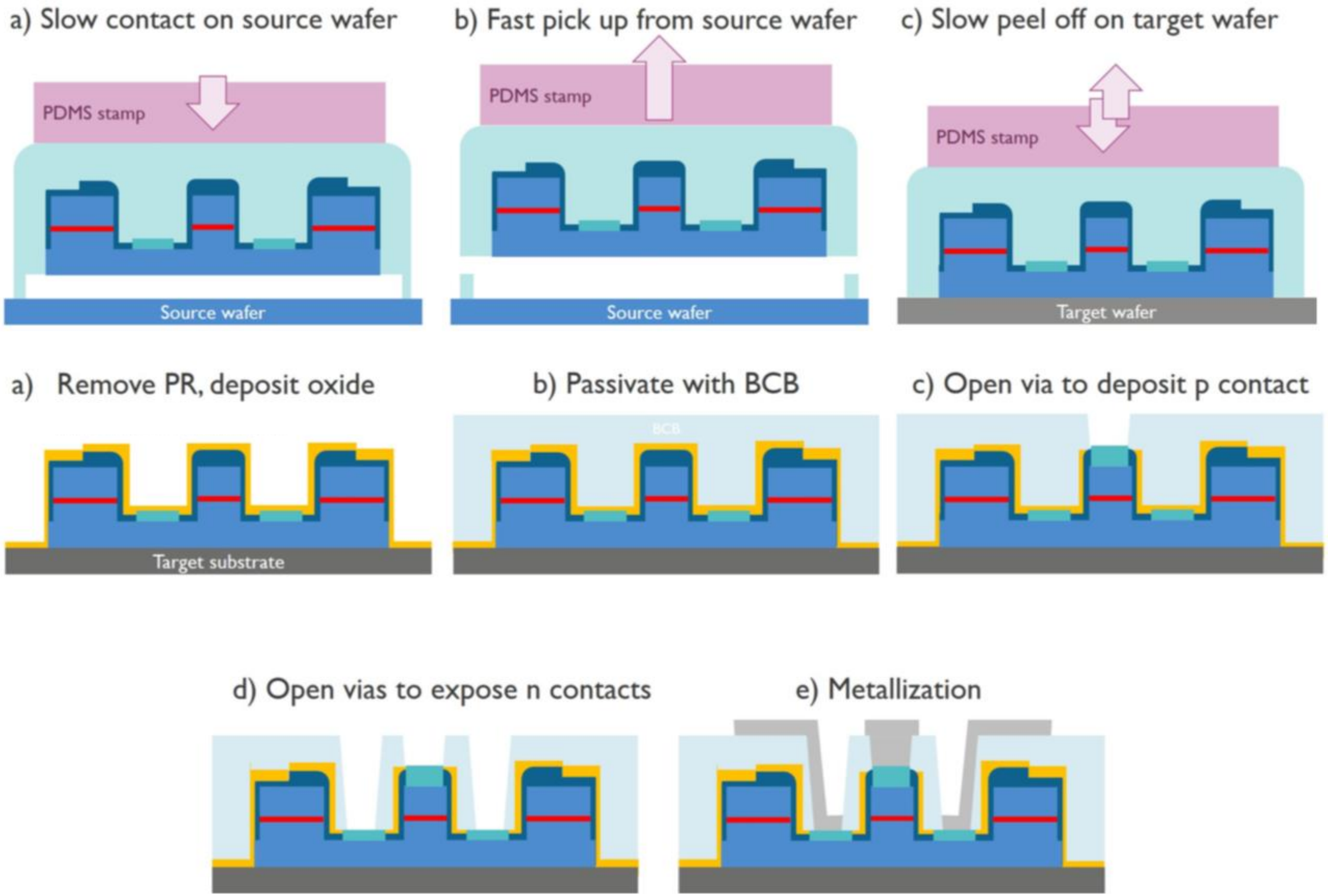
TRANSFER PRINTING OF ARRAYS OF LASERS



C-band SOAs on the III-V source wafer



TRANSFER PRINTING OF ARRAYS OF LASERS


a) Slow contact on source wafer

b) Fast pick up from source wafer

c) Slow peel off on target wafer

a) Remove PR, deposit oxide

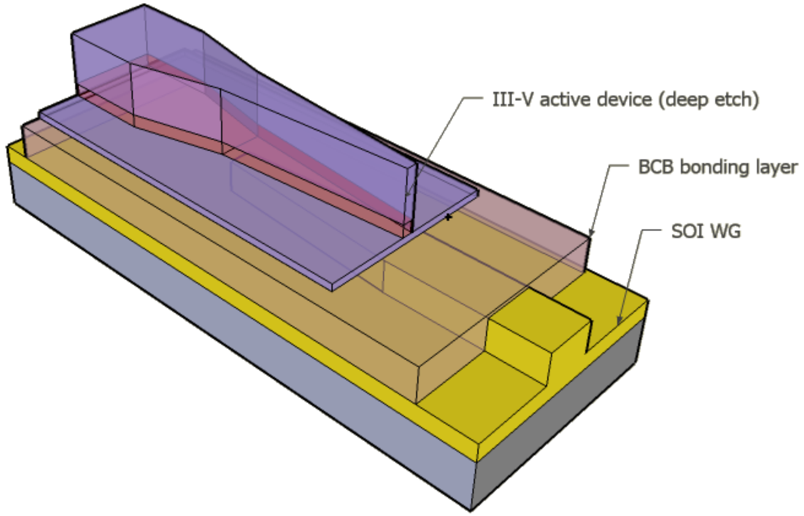
b) Passivate with BCB

c) Open via to deposit p contact

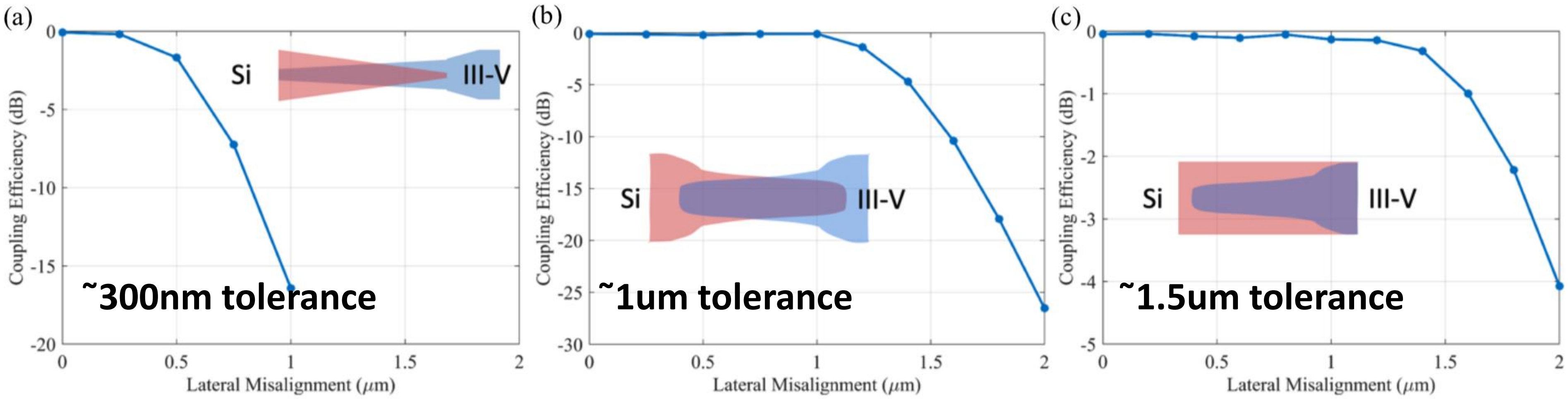
d) Open vias to expose n contacts

e) Metallization

ALIGNMENT TOLERANT OPTICAL INTERFACE



~250um taper length – transfer printing compatible

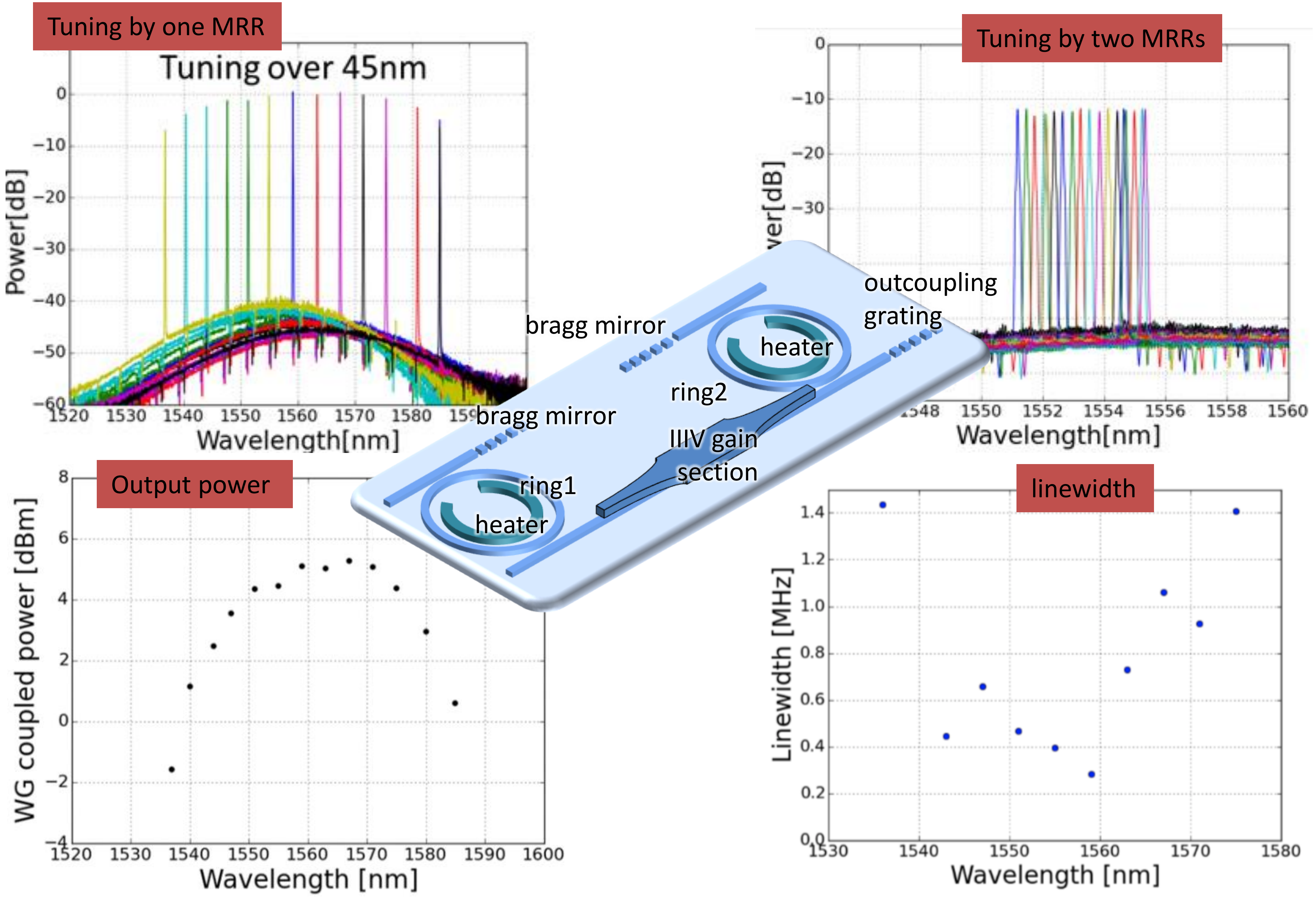


~300nm tolerance

~1um tolerance

~1.5um tolerance

WIDELY TUNABLE III-V-ON-SILICON LASER



Tuning by one MRR

Tuning by two MRRs

Output power

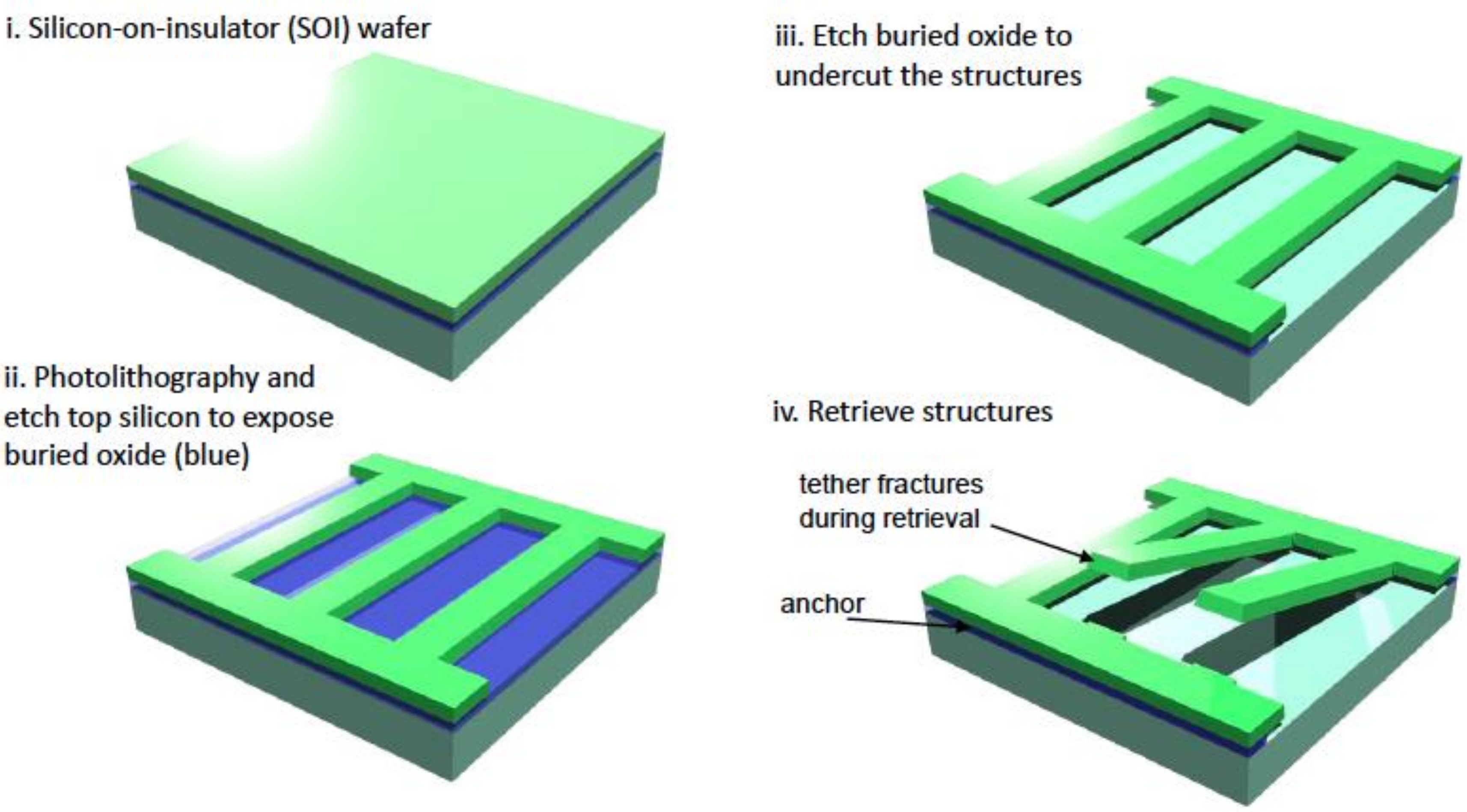
linewidth

OUTLINE

- Introduction to micro-transfer-printing technology
- Examples of III-V on Si micro-transfer-printing
- **Examples of Si on Si micro-transfer-printing**
  - **Ge photodiodes transfer printed on passive circuits**
  - **Si electronics transfer printing**
- Outlook & conclusions

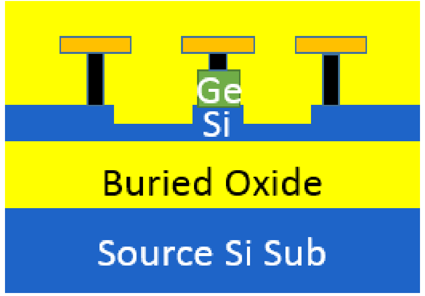
SI (OPTO-)ELECTRONIC DEVICE INTEGRATION

SOI (photonics / electronics) is very well suited for TP

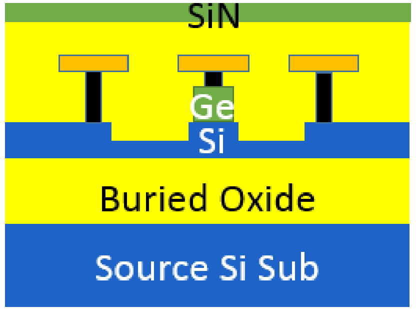


GePD Release process flow

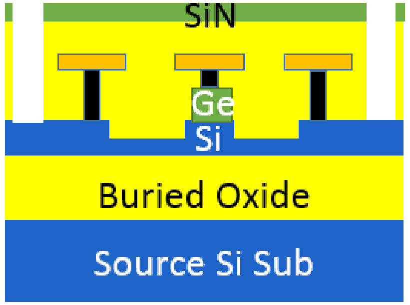
iSIPP25G chip



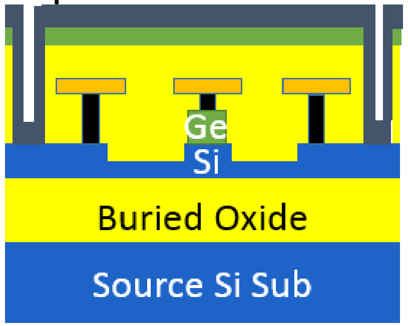
70 nm SiNx deposition



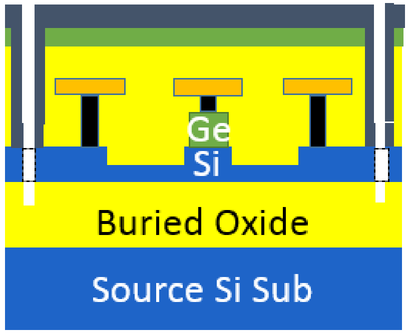
Litho I – coupon mesa



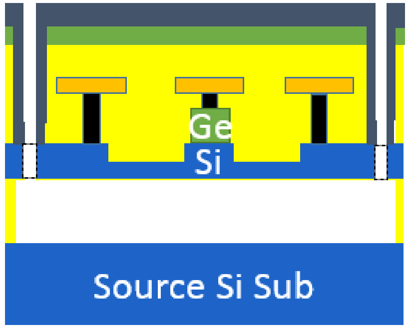
A-Si protection layer deposition



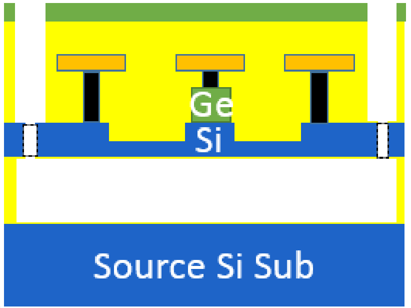
Litho II – Box exposure, Tether formation



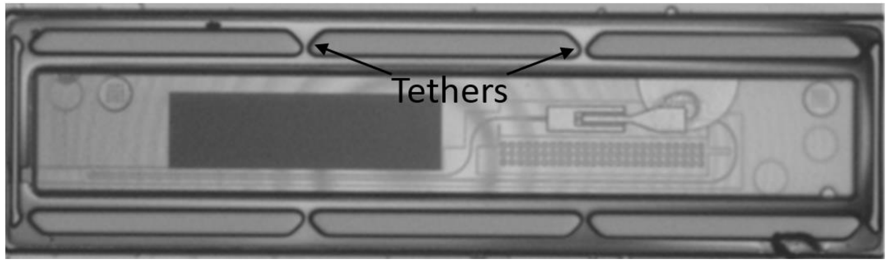
~13 min 40% HF release



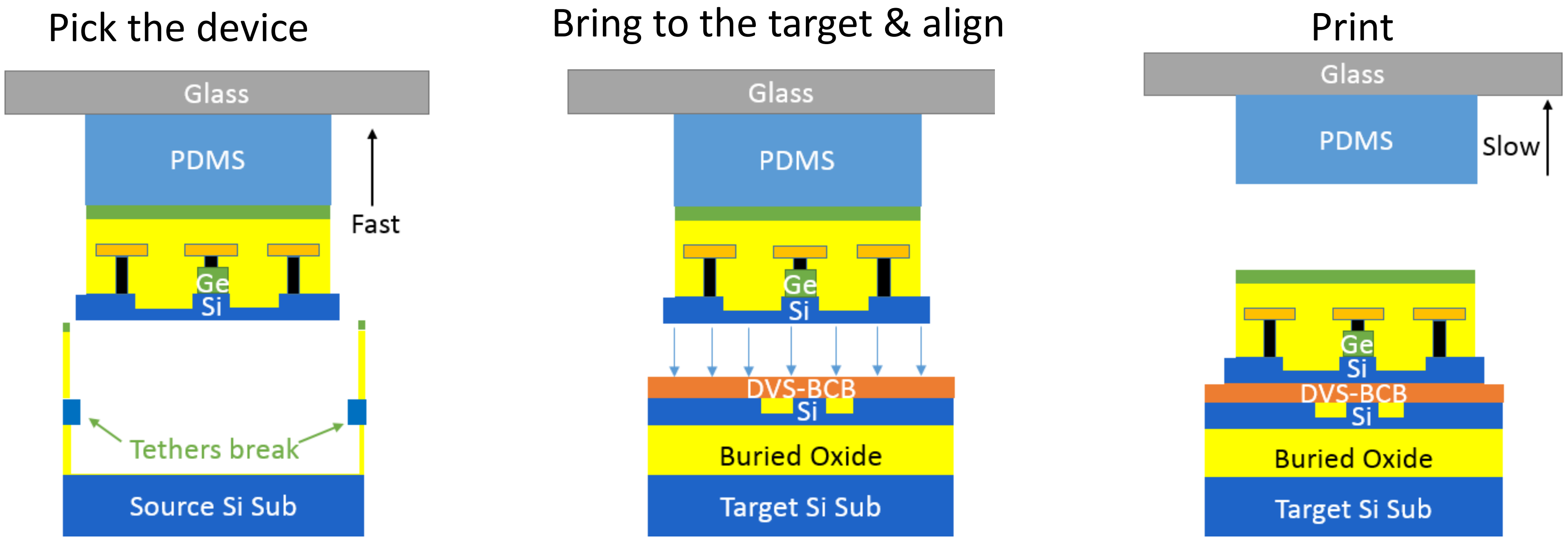
A-Si removal



Top view: device attached to the Si barrier using ~1.2 µm wide tethers



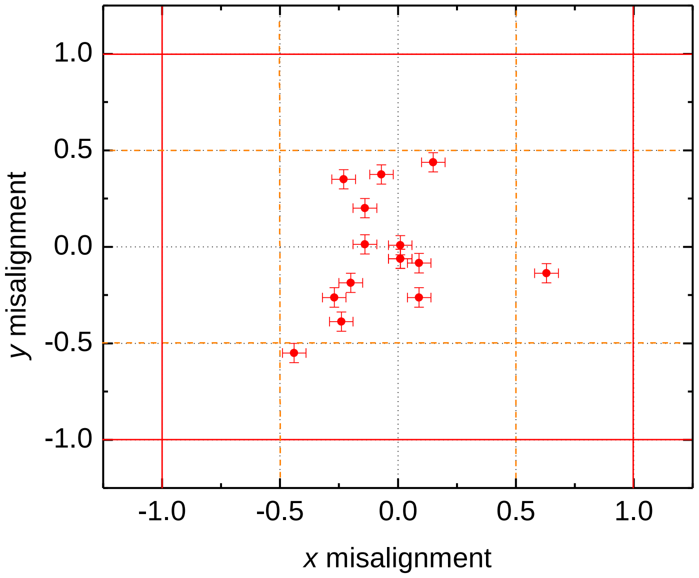
GED TRANSFER PRINTING PROCESS FLOW


Pick the device

Bring to the target & align

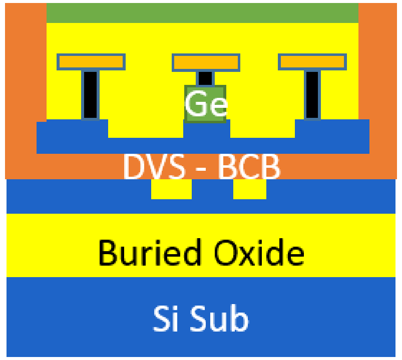
Print

+/- 0.5um printing alignment accuracy for printing of individual coupons

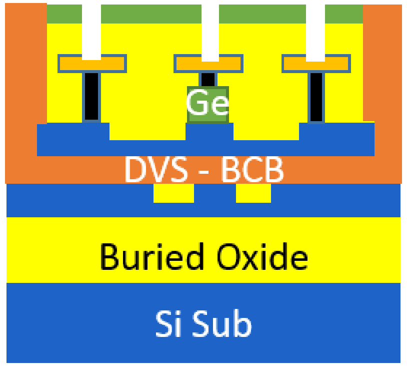


GE PD POST-PROCESSING

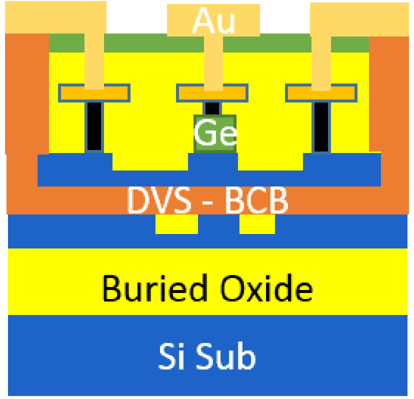
BCB spin-coated,
cured (280°C), planarized

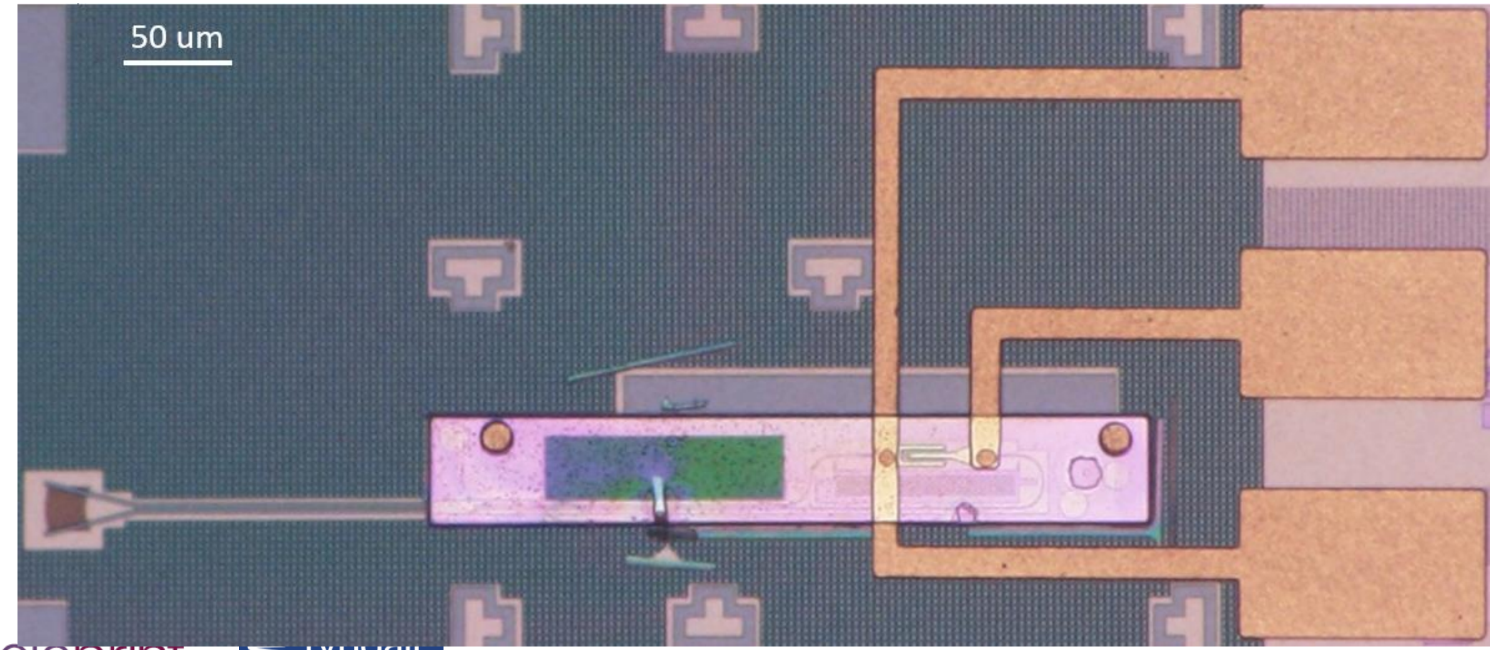


M1 window opened



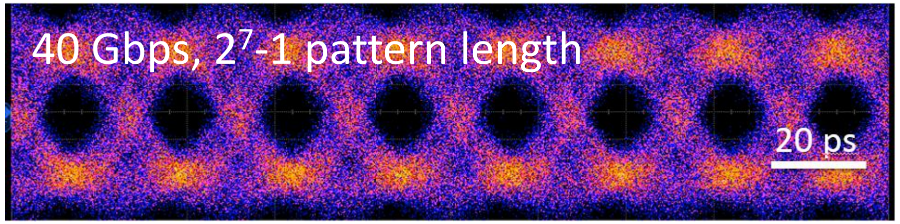
1.2 um Au contact deposited

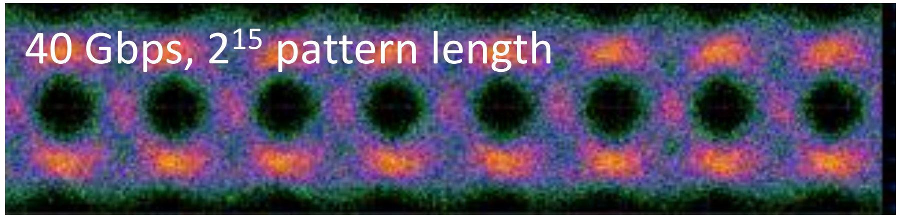


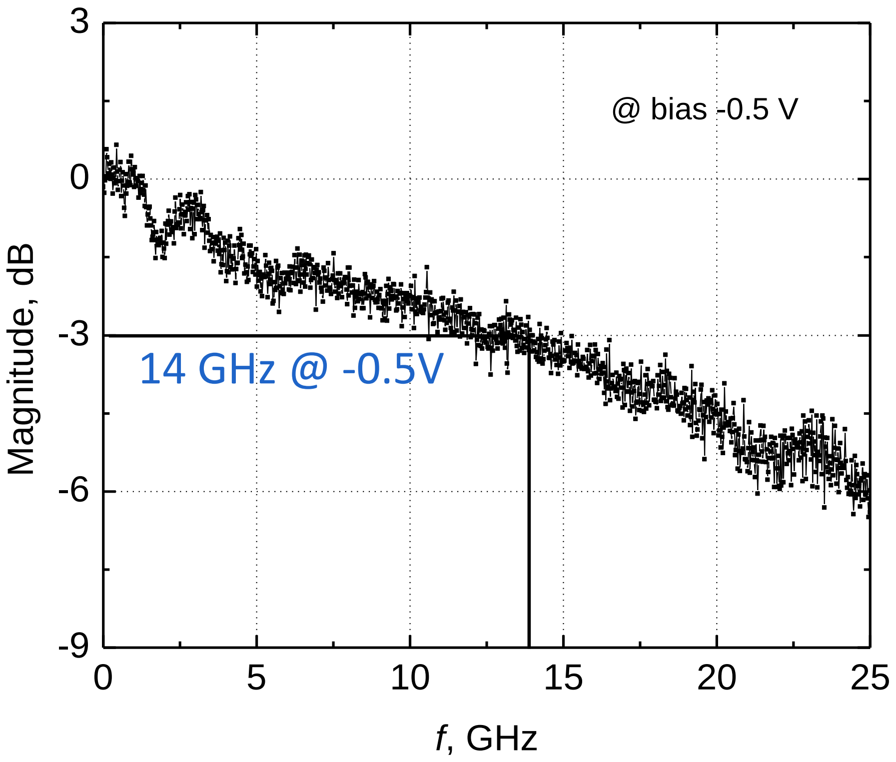


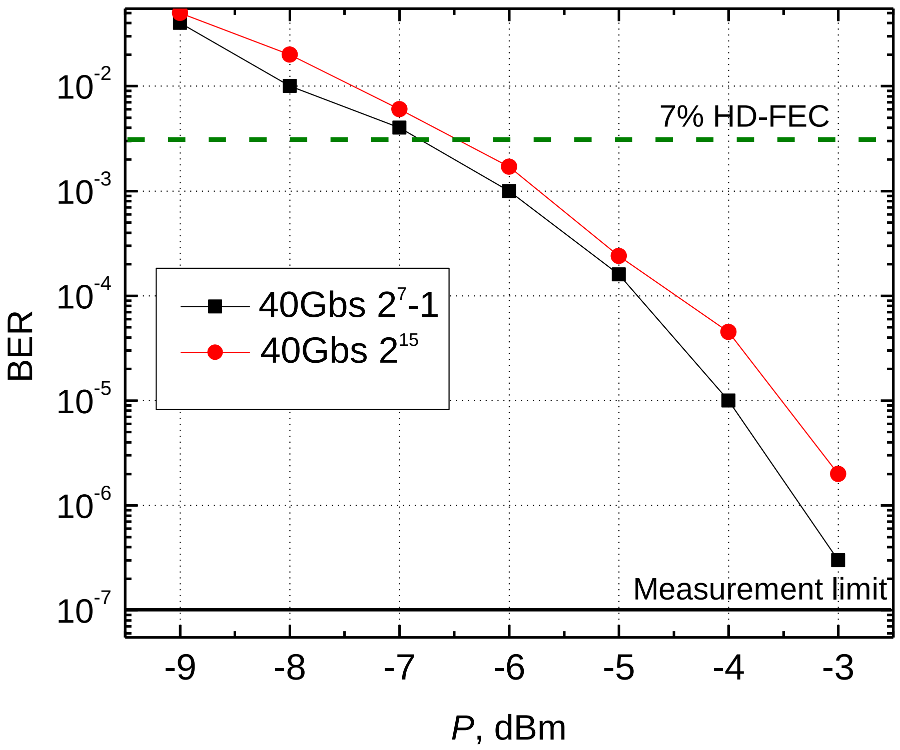
PRINTED GEPD CHARACTERISTICS

I_{dark} = 12 nA
R_{ser} = 29.6 Ohm
Responsivity > 0.6 A/W over C-band







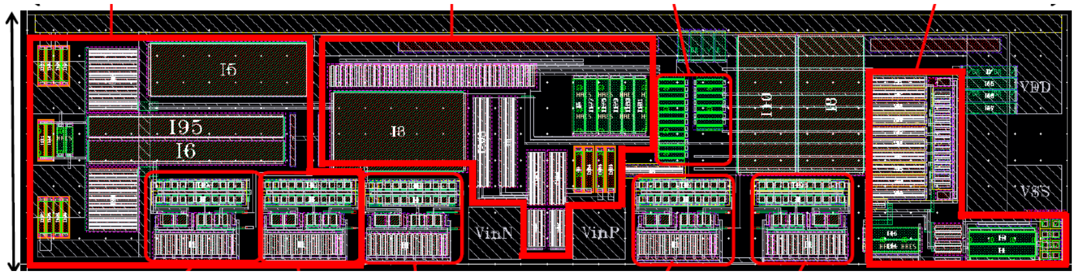


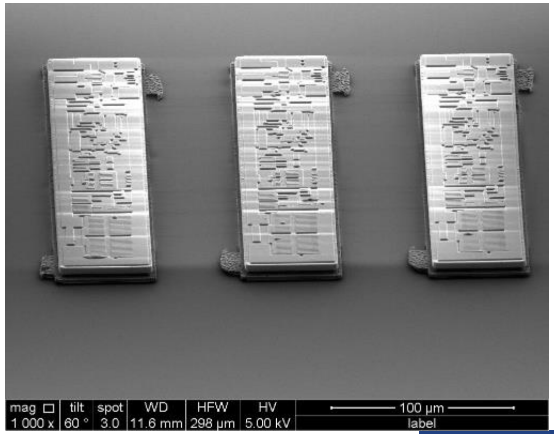
TRANSFER PRINTED ELECTRONICS

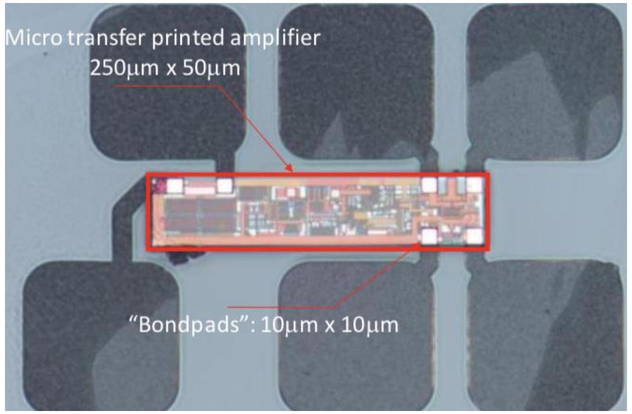
Design: P. Ossieur

Releasable silicon amplifier circuits realized

- XFAB 180nm SOI CMOS process
- 200μm x 50μm x 7μm device size
- Bond pads 10μm x 10μm

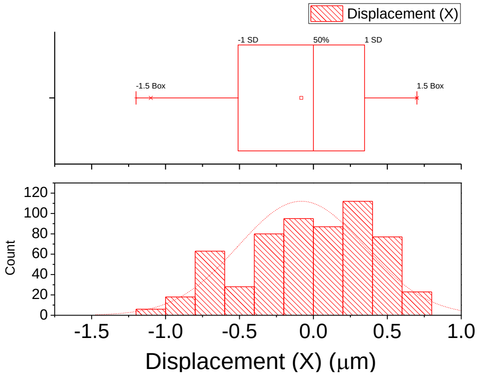


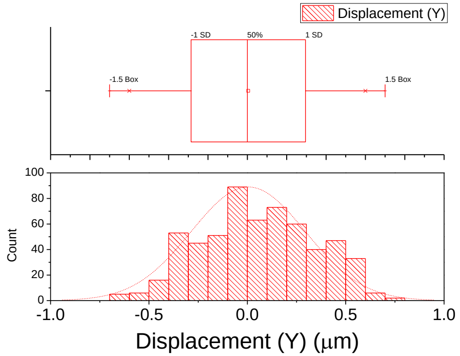



Micro transfer printed amplifier
250μm x 50μm

“Bondpads”: 10μm x 10μm

Positional accuracy better than ±1um in x and y





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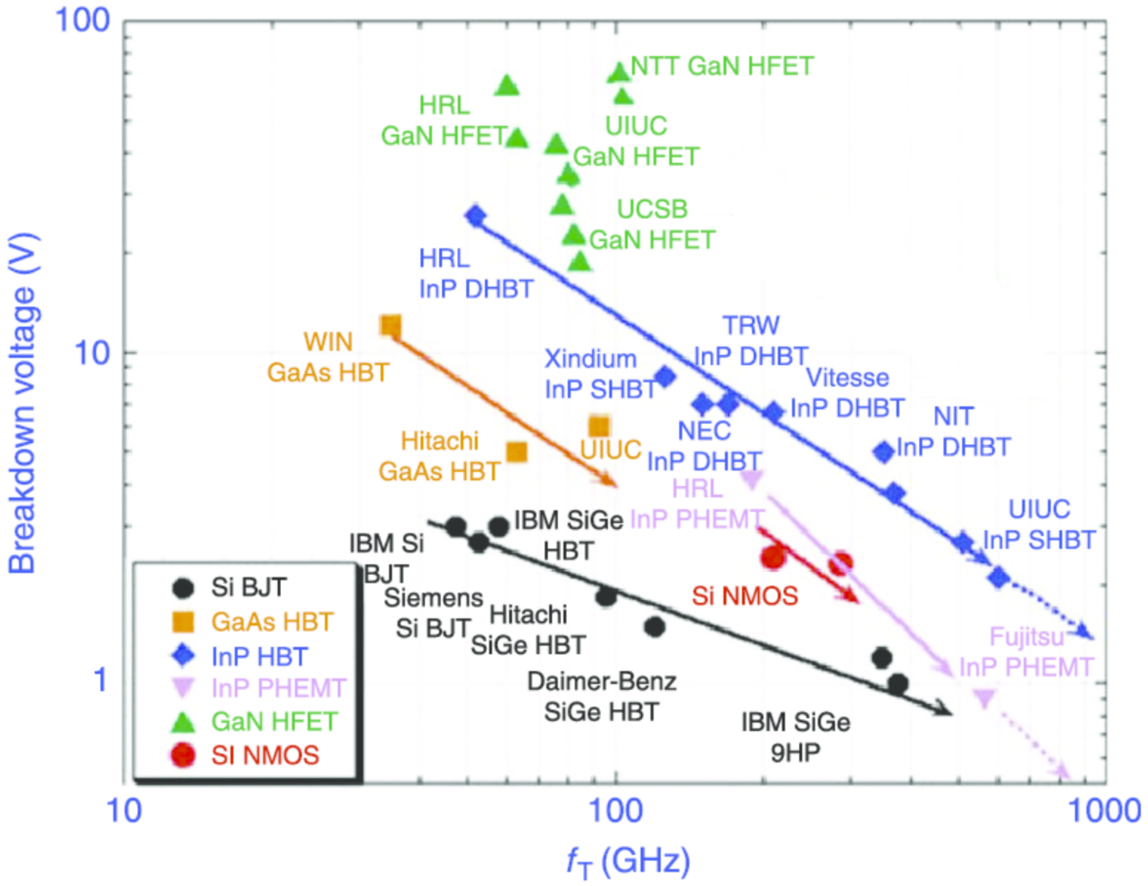
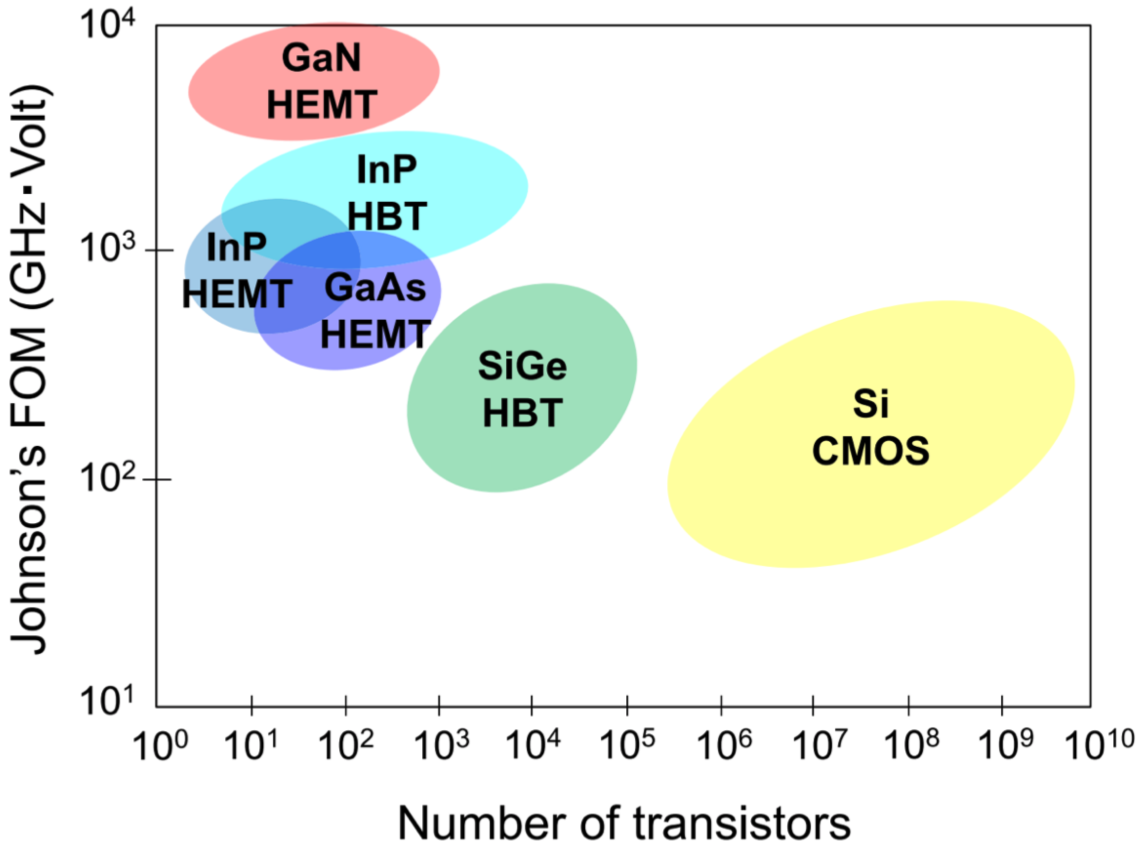
TRANSFER PRINTED ELECTRONICS – III-V ELECTRONICS





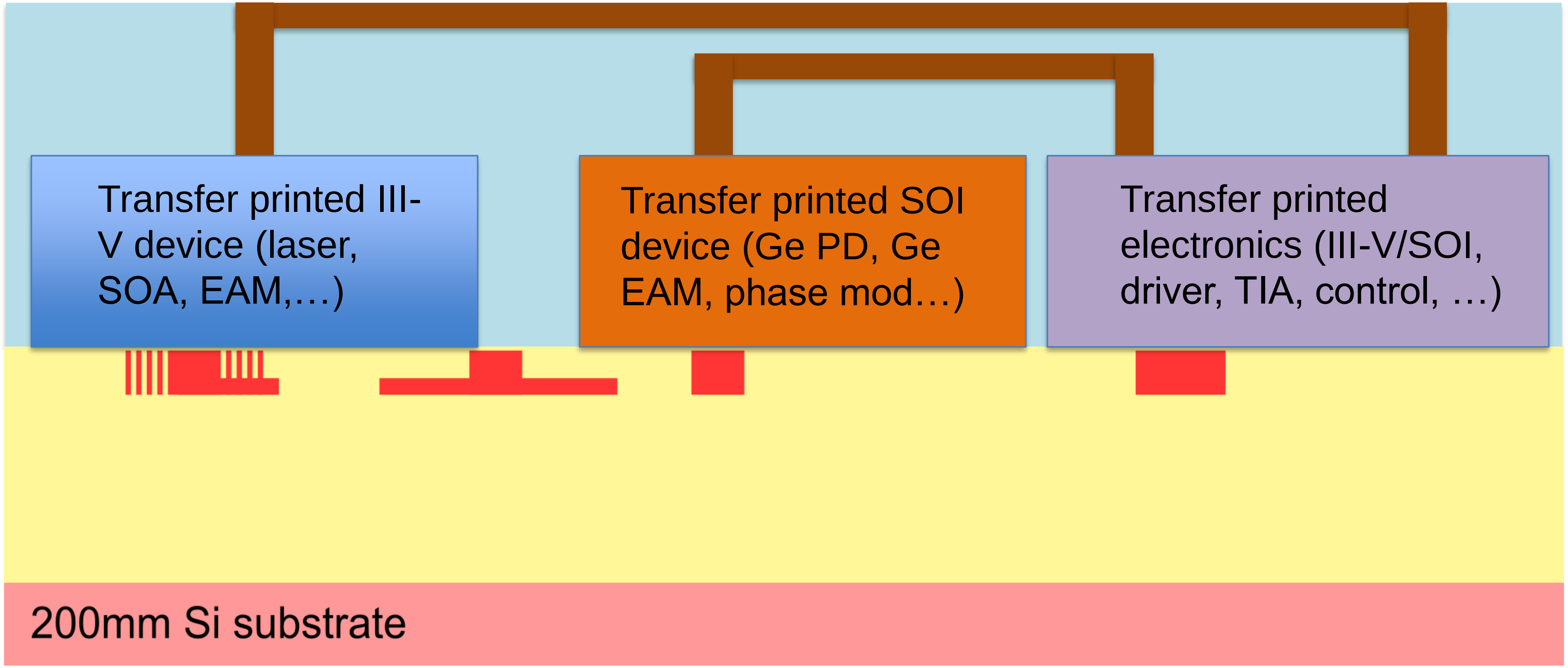
OUTLINE

- Introduction to micro-transfer-printing technology
- Examples of III-V on Si micro-transfer-printing
- Examples of Si on Si micro-transfer-printing
  - Ge photodiodes transfer printed on passive circuits
  - Si electronics transfer printing
- **Outlook & conclusions**

OUTLOOK: TRANSFER PRINTING IN A FOUNDRY

- The demonstrations presented in this work were realized on a lab printer
- Transfer the µTP-technology to an industrial environment (XFAB)
  - Bridging the "Valley-of-Death" to industrialization
- µTP pilot line in manufacturing environment for open access
  - Development of design rules (DR) and its implementation in Process-Design-Kits (PDK)
- Development of processes for heterogeneous system integration for (Bi)CMOS, MEMS and photonics wafers
  - Realization of processes for source wafer preparation, transfer printing and post-processing on 200mm silicon wafers
- Basically any material that can be released from its substrate can be transfer printed

HETEROGENEOUSLY INTEGRATED PICS



Transfer printed III-V device (laser, SOA, EAM,…)

Transfer printed SOI device (Ge PD, Ge EAM, phase mod…)

Transfer printed electronics (III-V/SOI, driver, TIA, control, …)

200mm Si substrate

CONCLUSIONS

- Micro-transfer-printing is an enabling technology for heterogeneous integration, combining advantages of flip-chip integration and wafer bonding
- Basically any material that can be released from its substrate can be transfer printed
- III-V integration and Si device integration on SiPh demonstrated
- Current demonstrations are lab-scale, but establishing an open access pilot line for the technology is work in progress

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