Micro-Transfer-Printing and Potential Process Optimizations by FEA

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Abstract

Micro-Transfer-Printing (µTP) as an alternative micro-assembly technology opens up new possibilities in the integration and packaging of smart devices like processed III/V devices, optical filters and special sensors on CMOS and MEMS on wafer-level. The technology uses an elastomer stamp to manipulate multiple printable components at the same time that are difficult to handle because of their size or fragility. Nevertheless, the industrial application of this technology as well as the transfer and upscaling from laboratory scale is still challenging. In order to realize a reliable printing process with sufficient yield, the interaction of the components to be printed, their fixation by tether structures to the source wafer and the adhesion of the transfer stamp must be well adapted. Therefore, the presented work will deal with results of mechanical experiments and FEA-modelling in order to get a deeper understanding of the µTP-process and will allow a defined tether layout and optimization of the processed source wafers.

1 Introduction

Looking on the current research of digital technologies, there are mainly two developments which are expected to have a major influence on today's society and are therefore of outstanding interest, namely the Internet of Things (IoT) and Artificial Intelligence (AI). Both of these technologies will further increase the already strong demand for highly-integrated CMOS and MEMS sensors with superior performance. Consequently, not only sophisticated MEMS / CMOS processing but also advanced packaging technologies will be required for satisfying the expected requirements on future sensor performance. Different technologies have been developed in microelectronic and also MEMS industry and are described in the literature [1,2].

In addition to the established approaches of e.g. through silicon via (TSV) integration and wafer level bonding, the new concept of micro-transfer-printing (µTP) [3] offers a promising technology for massively parallel heterogeneous integration of non-native components on wafer level.

µTP represents a versatile technology for micro-assembly which has been developed mainly in laboratory for more than 10 years and which is currently in the status of being transferred to an industrial environment. The technological principle is based on a parallel transfer of an array of identical devices onto a non-native target wafer. This transfer is implemented by a pick-and-place procedure typically provided by a polydimethylsiloxane (PDMS) stamp and its capabilities have been demonstrated for several applications like magnetic data storage, concentrator photovoltaics, µLED display technologies and different sensors [3].

Thereby, the lateral dimensions of the printed functional components can range from a few microns to a few hundreds of microns while the thickness remains usually around a few micrometers only. Furthermore, the technology offers a large potential of different native substrate materials ranging from 3, 4 & 6-inch III/V-semiconductor-based wafers over silicon wafers with optical or epitaxial layers up to 8 inch MEMS and 12 inch CMOS wafers.

The principal of the printing procedure is shown in Figure 1 and can be summarized to the following process steps:

1. Contact of the PDMS-transfer stamp to the native substrate with printable devices → a defined adhesive contact by Van der Waals forces of the stamp and device has to be ensured without damage of the devices
2. Pick up of the devices by the stamp → the separation of the printable devices from the native substrate has to be realized (e.g. by tether structures)
3. Transfer and deposition of the devices to non-native target wafers
4. Removing of the PDMS-stamp from the devices for reuse and further post processing of the devices → a reliable fixture of the devices to the target substrate is needed (e.g. by adhesive bonding)

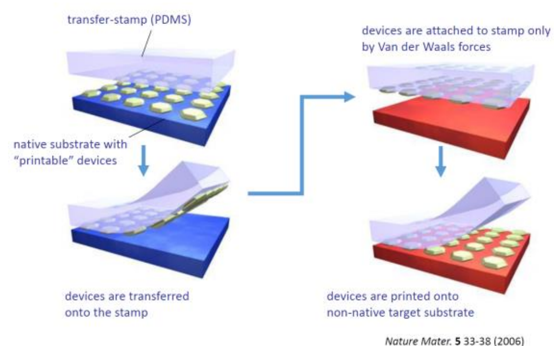


Figure 1: Principal of the µTP [4]

As shown at the sketch, an essential prerequisite of the µTP is a defined rate dependent adhesion behavior of the PDMS stamp material to the chip surface [4,5,6]. Here a higher printing velocity leads to an increasing adhesive force to the device and this behavior has to be aligned to the release properties at the source wafer in order to result in a high yield of the printing process. A common way to realize this release step is the use of Si_3N_4 tether structures which can be manufactured using etching techniques at the source wafer. An example of a possible chip/tether layout is shown in Figure 2a). By use of a patterned stamp array as show in Figure 2b), these structures can be mechanically separated during the printing process.

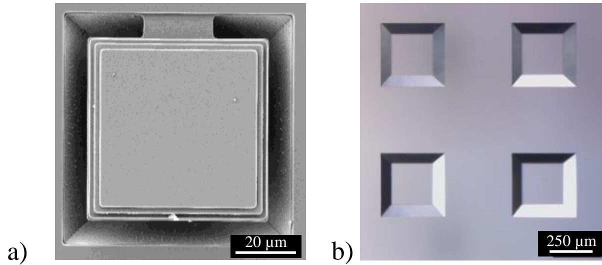


Figure 2: a) Printable device fixed by tether structures to the source wafer, b) Top view of a structured PDMS-stamp showing four single PDMS-posts

In order to get a deeper understanding of the stamp, chip and tether interaction the presented work will deal with FEA-modelling and mechanical experiments of the µTP pick up process step.

The generated model should allow a defined tether layout and design optimization of the processed source wafers. Therefore, important data defined by the velocity rate dependent adhesion of the PDMS-stamp material and its viscoelastic behavior as well as the mechanical load at the tether structures will be analyzed. The achieved measurement results were transferred into 3D models using a Prony series for the stamp material and adhesion properties for cohesive zone modeling (CZM) at the interface. As a result, the FEA-model should be capable to predict the stamp displacement vs. tether stress behavior at the pick-up stage of different tether designs.

2 Results

2.1 PDMS-Stamp Array Characterization

During the pick-up stage of the µTP-process the reaction forces at the tether structures are mainly influenced by the stiffness properties of the elastomer stamp material. Especially polydimethylsiloxane (PDMS) material is well known to show a highly nonlinear behavior and can be characterized using viscoelastic [7,8] or creeping models [9]. Nevertheless the specific material properties are dependent from the manufacturing conditions influencing the resulting polymer network and values of 1.32–2.97 MPa for Young's modulus can be found at the mentioned literature. Also the applied load condition (e.g. tensile- / compression- or indentation testing) during this parameter estimation can lead to significant variations of the models. Using literature data, first preliminary examinations of the µTP-process show, that these properties cannot fit the performed experiments with sufficient accuracy (see section 2.2.1) und further measurements at application related conditions are needed.

2.1.1 Measurement of Viscoelastic PDMS Properties

For characterization of the stamp material dynamic sweep measurements were performed using a DMA TA Q800 on a cylindrical PDMS specimen of 13 mm diameter and 3.1 mm height. The tests were performed in compression mode. Assuming the principle of time temperature superposition the measurements were done at a temperature range of -50…150°C and a frequency range of 1...55 Hz in order to predict a wide range of velocity and relaxation times.

Figure 3 shows the resulting frequency dependent behavior of the storage (E') and loss modulus (E”) measured at the experiment. For parameter identification a fit-function of the storage modulus following the Generalized Maxwell model was generated using equation (1) with a sum of z=25 terms. In this equation ω describes the radial frequency, E_i the stiffness constant i and τ_i the time constant i [10].

$$E' = \sum_{i=1}^{z} \frac{E_i \omega^2 \tau_i^2}{1 + \omega^2 \tau_i^2} \quad (1)$$

$$E'' = \sum_{i=1}^{z} \frac{E_i \omega \tau_i}{1 + \omega^2 \tau_i^2} \quad (2)$$

As shown at the graph the resulting fit-function matches the experimental data of E' very well, while a deviation of E'' occurs (estimated by equation (2)). Here the approximation of the material simplification by a viscoelastic model is limited for E''.

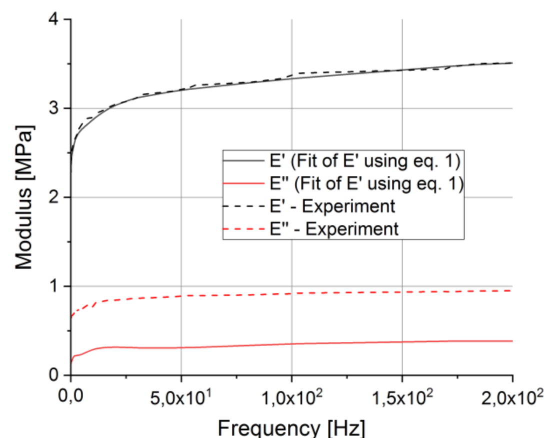


Figure 3: Measured frequency dependent storage and loss modulus of the PDMS stamp material by DMA

$$2G(t)(1+v)=\sum_{i=1}^{Z}E_i e^{-t/\tau_i} \quad (3)$$

From the data of *E'* the time dependent shear relaxation modulus *G(t)* was determined by equation (3) and is show in Figure 4. In comparison to literature [7] an increased stiffness of the characterized material under the assumed compression loading is obvious. Afterwards the gained data was used to fit the shear- and bulk-relaxation moduli inside ANSYS v.19.2 assuming a constant Poisson's ratio of ν=0.49. A validation of the resulting material behavior using a pattered PDMS post structure for printing is shown in section 2.2.1.

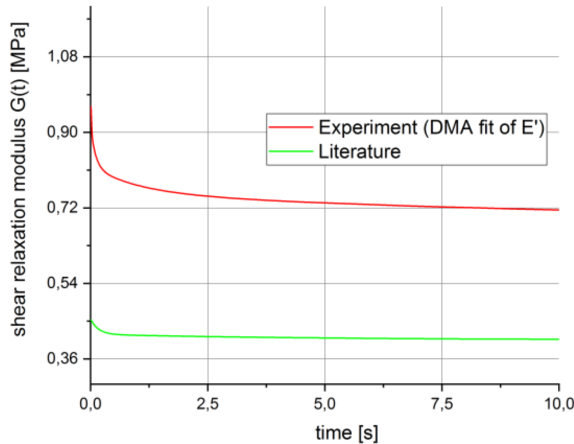


Figure 4: Measured time dependent shear relaxation modulus *G(t)* in comparison to literature data [7]

2.1.2 Rate Dependent Adhesion Measurements

The second important parameter to model the µTP-process by FEA is given by the description of the adhesion behavior between the PDMS stamp and the chip surface which is based on Van der Waals forces.

Therefore fracture mechanical data can be found in literature [5,6] where the temperature and rate dependent energy release rate of a kinetically controlled transfer printing process was measured. Nevertheless, the transfer to available modelling approaches like CZM can be quite complex and further parameter alignment is needed. In order to realize a more application oriented approach, all necessary CZM-parameters were estimated from a velocity dependent tension test of a single PDMS-post attached to a Si_3N_4 surface.

The measurement was performed using a dynamic uniaxial test device with a variable pick-up velocity of 1...132 mm/s. Figure 5 shows the test setup where a Si_3N_4-surface (top) is pushed to the PDMS-post (bottom) with 0.35 MPa initial load and v=0.1 mm/s (overdrive). After 1s dwelling time the structure is pulled off considering different velocities.

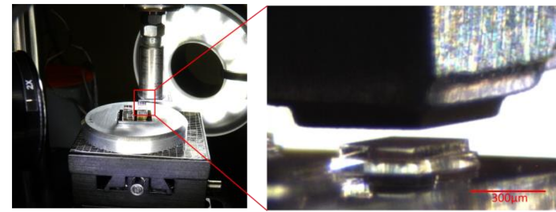


Figure 5: Used test setup to measure the rate dependent adhesion force of a Si_3N_4 / PDMS-post interface

The resulting force vs. displacement behavior of the experiment is schematically shown in Figure 6. It can be clearly shown that the adhesive force increases with higher velocity and also the stiffness of the stamp during unloading increases for higher strain rates caused by viscoelastic effects.

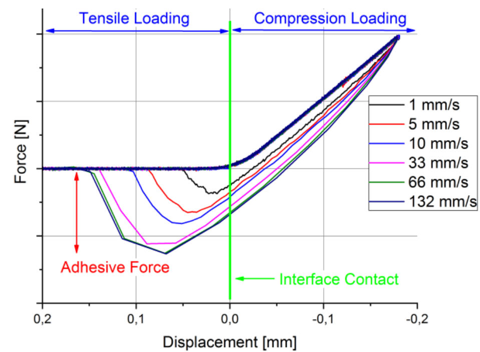


Figure 6: Schematic of the adhesive force measurement

The maximum stress values of the experiment of five different sample structures (100x single measurements for each structure and each velocity) are shown in Figure 7. It can be shown, that a maximum adhesion stress of 0.4 MPa to 0.45 MPa can be reached using this type of PDMS material. Also observed standard deviation between 100 cycles (touch down and lift off of one structure) is rather small and the total reproducibility between different test structures of one test array is good. In addition, a saturation of the maximum adhesion stress can be found at velocities higher ~30 mm/s. For parameter identification this measurement data was used to fit the parameter of a mode I dominated bilinear CZM in section 2.2.1.

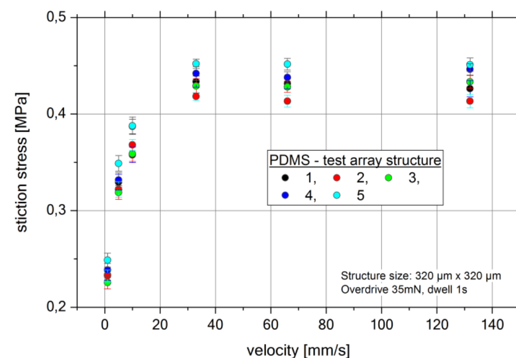


Figure 7: Measured adhesion stress at the PDMS / Si_3N_4 interface of the five different test structures

2.2 FEA-Modeling of the µTP Process

2.2.1 Numerical Calibration of the PDMS-stamp behavior

i. Validation of the Viscoelastic Material Assumption

For validation of the material data presented in section 2.1.1 and its application inside FEA a compression test of a single stamp was simulated. Therefore, the setup of Figure 5 and the compression load regime of Figure 6 was used to compare the viscoelastic behavior of the PDMS-stamp in compression mode.

For modeling the Si_3N_4 surface was assumed to be rigid, which seems to be sufficient, comparing the Young's moduli of PDMS (E_0 = 1.1 MPa) and Si_3N_4 (E = 166 GPa). The top side of the PDMS stamp was pushed onto a flat Si_3N_4 surface with velocities of 0.01, 0.1, 1 and 5 mm/s. A sketch of the model including the boundary conditions is shown in Figure 8.

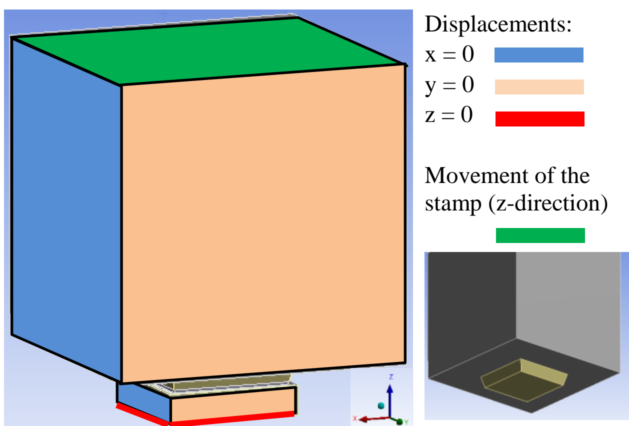


Figure 8: Sketch of the FE-model for validation of the viscoelastic stamp behavior showing the boundary conditions and the geometry of the stamp

A comparison of the resulting force vs. displacement curves of the experiment and simulation including literature data of [7] are shown in Figure 9.

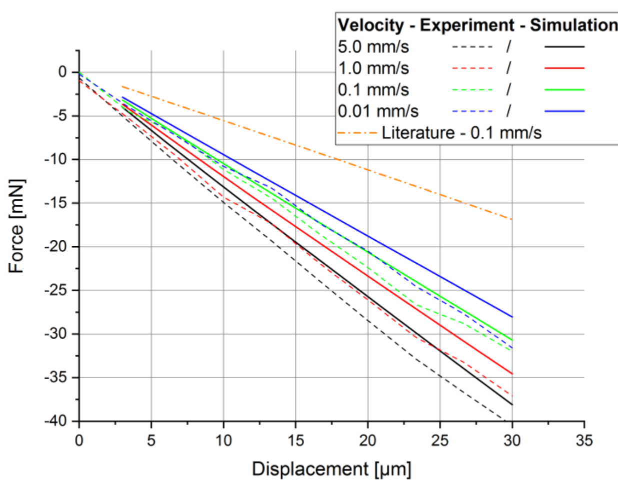


Figure 9: Force vs. displacement of the performed compression tests to validate the determined material properties in comparison to the experiment and literature

The modelling of the viscoelastic PDMS material seems to fit the real behavior quite well which can be seen in the change of stiffness using different velocities. The absolute stiffness is not perfectly met. This might be caused by a not exactly remodeling of the sample geometry. Therefore, further investigation of the accurate geometry has to be done.

ii. Calibration and Validation of the Adhesion Model

For modelling of the adhesive contact between stamp and Si_3N_4 surface, CZM was used. CZM is a part of interface models being used to describe crack growth or delamination of adhesives like epoxy, polyurethane or silicone [11]. Therefore, CZM can be used to describe the following modes of separation:

- Mode I: contact surfaces are separating normally to each other
- Mode II: contact surfaces are separating tangentially to each other or
- Mode III: represents a combination of Mode I and II

In comparison to the µTP process steps mentioned in Figure 1, a mode I dominant separation for the pick-up process from the source wafer and a mode III process for stamp release after printing becomes relevant. Because the current FEA-work is focused on the interaction of the stamp and tether design during pick-up, only a mode I separation is considered by a bilinear CZM approach at the current state.

To do so, three parameters are needed. An artificial damping coefficient η which is set to be $5 \cdot 10^{-7}$ s for all simulations, the maximum normal contact stress σ_{max} and the contact gap at the completion of debonding u_{sep} were determined by the adhesion measurements describe in section 2.1.2. Figure 10 shows exemplarily how this parameter alignment has been done for one pickup speed using the force vs. displacement curve. The maximum normal force ($F_{z,max}$) needs to be converted into a stress depending on the used stamps geometry.

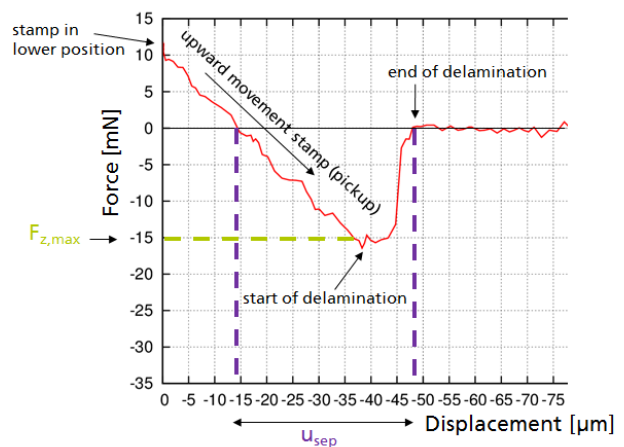


Figure 10: Rate dependent CZM-parameters used for the simulations

Afterwards validation of the determined CZM-parameters was done by using the above mentioned experimental setup and stamp geometry (see Figure 8) adding a upward movement after pushing the stamp onto the substrate. The velocity at compression was constant 0.1 mm/s. Pick-up speeds of 5, 10, 33 and 66 mm/s were tested. The resulting force vs. displacement curve of the experiment and simulation is shown in Figure 11. The CZM-model assumptions are in good agreement with the experimental data. The model can represent the entire pickup process of the stamp on a substrate starting at the compression of the stamp up to the complete debonding.

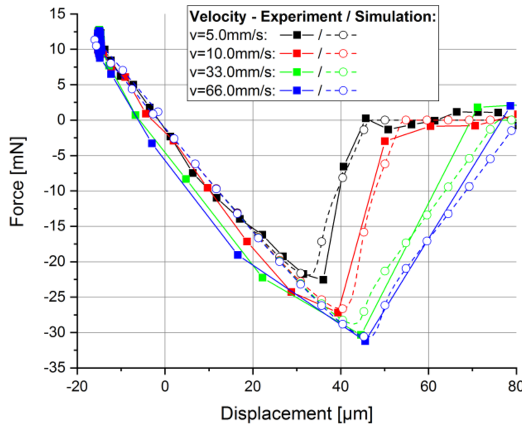


Figure 11: Force vs. displacement of the stamp during compression and pick-up, up to the debond at the interface at different pickup velocities

2.2.2 µTP-Process Modeling

For modelling the µTP-process, the same stamp geometry like shown in Figure 8 was used. A quadratic Si_3N_4 chiplet was modeled being attached to a {100} Si-wafer by two different tether designs (see Figure 13a - single side fixed and symmetrically fixed version). Caused by the Si-lattice, the cavity below the chip has an angle of 54.74° also defining a notch to the Si_3N_4-tether. An adhesive contact between the top side of the chip and the stamp using CZM is defined. In order to consider possible contact of the chip and the cavity side wall during downward movement, also a frictionless contact between the bottom side of the chip and this wall has been modeled (see Figure 12). The material properties and boundary conditions of the model are the same as described in the previous chapter.

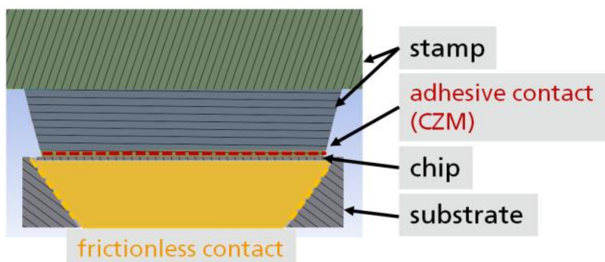
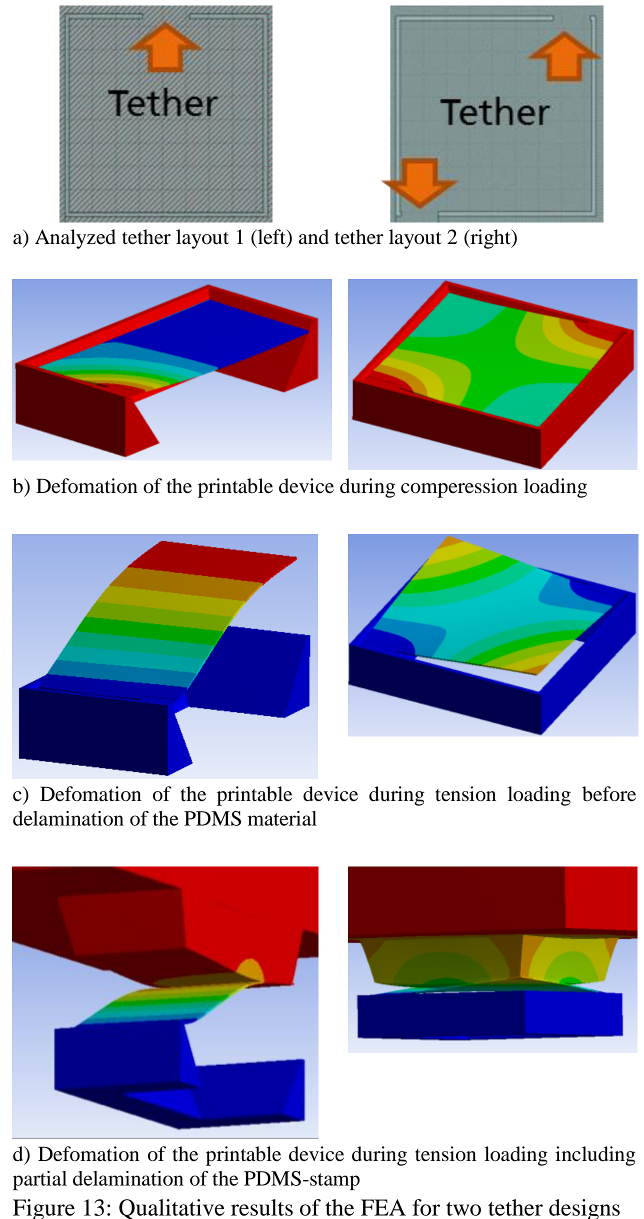


Figure 12: Schematic of the FEA-model for µTP-modeling

2.2.3 Results of the FEA Modeling

Figure 13b) shows the deformation of the printable device, when the stamp is in the lower position (compression loading). At a certain stamp displacement, design 1 shows a contact of the chip edge to the cavity side wall. In contrast design 2 shows a maximum deflection of the corners where no tethers are attached. In Figure 13c) the deformation of the designs during upward stamp movement (tension loading) is presented. Because at the current model no breaking mechanism of the tether has been included yet, the stamp will start to debond from the chiplet if the contact normal stress exceeds σ_{max} in order of the stamp displacement as shown in Figure 13d).



a) Analyzed tether layout 1 (left) and tether layout 2 (right)

b) Defomation of the printable device during comperession loading

c) Defomation of the printable device during tension loading before delamination of the PDMS material

d) Defomation of the printable device during tension loading including partial delamination of the PDMS-stamp

Figure 13: Qualitative results of the FEA for two tether designs

The resulting calculated kinematic behavior of the printing stamp together with the resulting maximum stress at the tether (1st principal - S_{11}) are shown in Figure 14.

From this graph the following regimes can be defined:

I. Initial contact of the stamp to the devices surface
II. Compression loading of the stamp; the released chip reaches the remaining material of the source wafer below; this state defines the max tether stress during downward movement
III. Starting delamination of the PDMS stamp from the chip surface; the separation from the native substrate must have occurred up to this position.

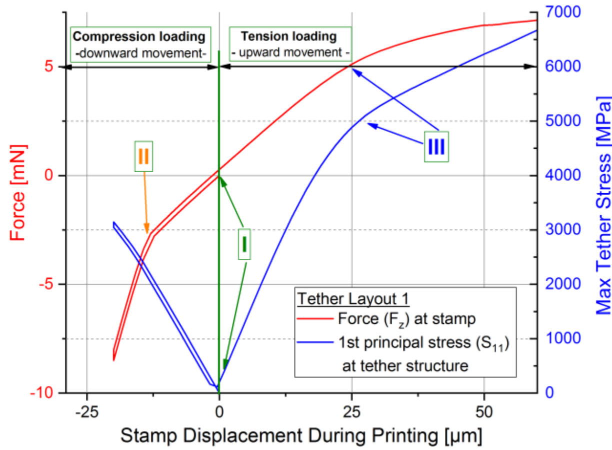


Figure 14: Force / stress vs. displacement of tether design 1 during µTP-printing (*stress values assuming a sharp notch at the tether / cavity interface leading to significant overestimation of the real stress (stress singularity))

In order to define a failure mode of the tethers, critical fracture stress values for Si_3N_4 of 400-500 MPa can be found in literature [12,13]. Hence, for layout 1, fracture of the tether structures would occur before reaching the maximum downward movement of the stamp (between point I & II). Nevertheless experimental validation of these values is needed and planned at a next step. In addition, the current model assumes a sharp notch between the tether and cavity interface. This can lead to significant overestimation of the model caused by local stress singularities of the real stress. For comparison of absolute stress values a detailed analysis of the notch radius and therefore an adapted FEA-mesh showing a sufficient element size convergence is needed.

Hence, at the current state only a qualitative comparison of different tether layouts is feasible, leading to deeper process understanding, but further validation is needed. A second and more quantitative approach to predict the tether release is given by fracture mechanical approaches using fracture toughness (K_{IC}) of Si_3N_4 [14]. This approach, together with experimental measurements of the tether strength using dummy chips, will be added at a next step of the project to align the calculated stiffness and stress behavior of the model.

In order to crosslink the simulation results to practical issues, two application oriented case studies (i) comparison of different layouts and (ii.) varying process parameters will be discussed:

I. Comparison of Different Tether Designs

Figure 15 shows the results of the two analyzed tether designs 1 and 2 of Figure 13a) in comparison. Considering the force vs. displacement plot, design 2 is significantly stiffer than design 1, leading to increased stresses at the tether regarding the same stamp displacement. Although design 2 is showing a contact of the chip onto the cavity side wall as well, which can hardly be seen on the graph, its tether is expected to break earlier. Due to the increased forces during upward movement, the delamination starts earlier, if no fracture of the tether occurs.

It can be assumed that both tethers of design 2 will not break at the same time which will have further influence to the kinematic behavior. This case should be part of further experimental and numerical investigations to be able to verify this mode of tether breakage.

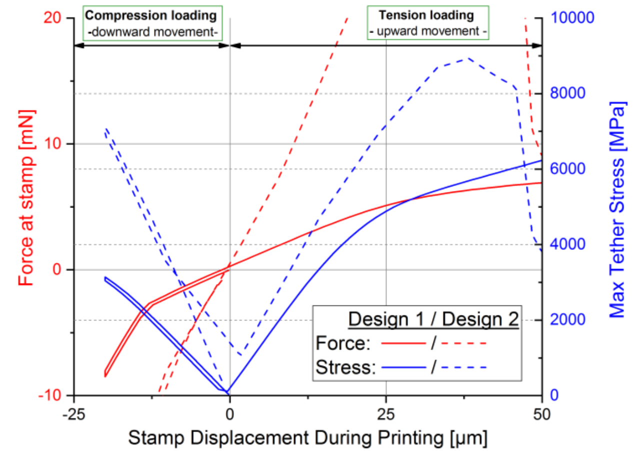


Figure 15: Force / stress vs. displacement of design 1 in comparison to design 2

II. Variation of Pickup Velocity and Adhesion Parameters

In Figure 16 a variation of the stamp's pick-up velocity (1 mm/s and 70 mm/s) with derived experimental CZM-parameters and a ten times reduced adhesive capability (70 mm/s - representing a PDMS surface contamination or degradation) using tether design 1 is plotted. Due to a constant compression speed, there is neither a difference during the downward stamp period in stiffness nor in tether stress.

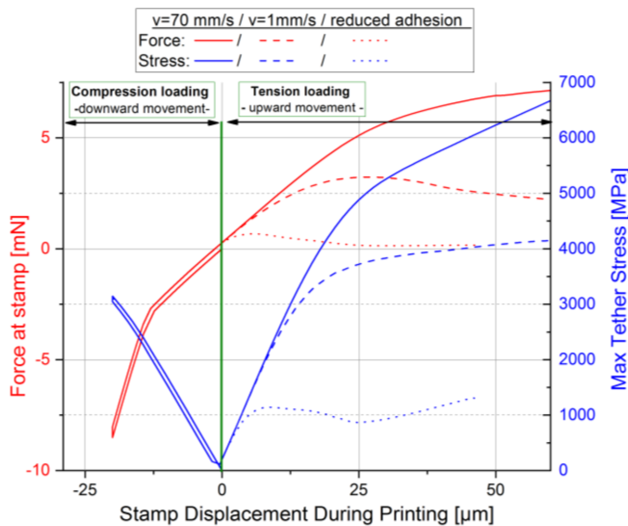


Figure 16: Force / stress vs. displacement at 70 mm/s and 1 mm/s as well as at 70 mm/s with a reduced adhesion of the stamp

As expected, a slower move up velocity of the stamp leads to an earlier debonding and lower maximum stresses at the tether during tension loading. This is caused in the viscoelasticity of the PDMS and the varying adhesive parameters at different velocities. Also the reduction of adhesive CZM-parameters of the stamp (representing contamination or wear) leads to a reduced stress at the tether structures avoiding fracture events at real printable devices.

3. Conclusion and Outlook

Micro-Transfer-Printing is an alternative micro-assembly technology which opens up new possibilities in the assembling and packaging of smart devices. In order to get a deeper understanding of the transfer printing process a mechanical and numerical workflow was generated to measure and to model the kinematic behavior during the pick-up process of a single printable device. The presented model can help to understand critical failure modes resulting from insufficient stamp adhesion or damage of the devices caused by contact to the remaining material after release etch of the source wafer. In addition, the current state allows the comparison of different tether layouts in order to get information about the qualitative local stress distribution at the tether structures. This information can help to optimize tether geometries for source wafer processing and can increases the printing yield during industrial application.

Nevertheless a qualitative evaluation of the stress values and model alignment is still needed. This evaluation is planned by nano-indentation experiments as far as test structures are available. After that alignment, the model can be used for the tether design of a wide range of lateral chip dimensions or further applications, reducing the number of empirical process designs.

Also model enhancements to fracture mechanical approaches for the tether breakage like stress intensity factors, CZM approaches or XFEM are planned as well as an evaluation of the influence of intrinsic stress of passivation layers. Finally the presented model can be extended to further µTP process steps like the placement of the devices to the target wafer followed by removing the stamp for reuse.

Acknowledgments

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