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A Very High Speed, High Resolution Current Comparator Design

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Abstract : This paper, presents an idea for analog current comparison which compares input signal and reference currents with high speed and accuracy. Proposed circuit utilizes amplification properties of common gate configuration, where voltage variations of input current are amplified and a compared output voltage is developed. Cascaded inverter stages are used to generate final CMOS compatible output voltage. Power consumption of circuit can be controlled by the applied gate bias voltage. The comparator is designed and studied at 180nm CMOS process technology for a supply voltage of 3V.

Keywords : current mode, comparator, high speed, high resolution.
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