A Dual-Window DC Bus Interacting Method for DC Microgrids Hierarchical Control Scheme

Fulong Li, *Student Member, IEEE*, Zhengyu Lin, *Senior Member, IEEE*, Zhongnan Qian, Jiande Wu, *Member, IEEE*, and Wei Jiang, *Member, IEEE*

***Abstract*--Hierarchical control schemes have been commonly employed in DC microgrid controls, which combine local control, DC bus voltage coordination and communication links to guarantee smart operation of DC microgrids. Conventional DC bus voltage regulation cannot conduct signal exchange. Therefore, external communication links are usually needed for hierarchical control schemes. However, once the communication link fails, the hierarchical control system will lose its ability to coordinate the distributed power smartly. This paper proposed a dual-window DC bus interacting (DBI) method to exchange information between the distributed energy sources, for the situations where communication link fails or is not available. A small-scale DC microgrid experimental system was setup, and a simple Master-Slave control scheme is implemented without communication link to demonstrate the feasibility of the proposed DBI method for DC microgrid controls. The expandability and immunity of the proposed DBI method were also evaluated.**

***Index Terms*-- DC microgrids, DC bus interacting, droop control, decentralized control.**

I. Introduction

With technology advancement of power electronics, more and more distributed energy sources (DESs) have been connected to the power grid, such as wind turbines, photovoltaics (PV) and energy storages. Conventionally, these energy sources are connected to the AC utility grid via grid-connected inverters. With the increasing number of DC renewable generation, energy storage and electronics loads, DC power systems have gained an increasing interest in the last several years. A DC microgrid [1] is a controllable subsystem with a cluster of DESs connected via a common DC bus, and can provide power to local loads. Compared with conventional AC systems, integrating DESs with a common DC bus has advantages of more flexibility, efficiency and reliability [2]. Besides, the nature of DC means that it does not have reactive power and synchronization issues, so the system design is simpler than an AC system.

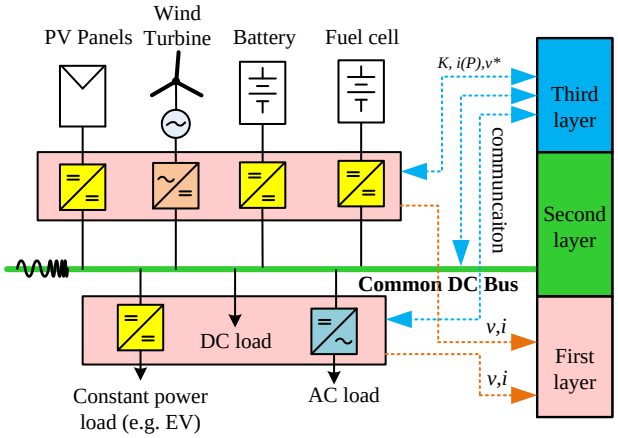

Fig. 1. A typical DC microgrid structure.

Paralleling DESs via a single common DC bus, as is shown in Fig.1, is one of the mostly used structure for DC microgrids [3]. Coordination and control of each distributed source are important for the system to operate efficiently. Different types of hierarchical control schemes [4][5][6][7] have been investigated for DC microgrid controls. In general, local controls [6] (such as voltage/current control and droop control) are embedded in the first layer to respond to the fast dynamics of power converters. The second layer control is to deal with power flow between DESs. The third layer is used for high level power management through communication links, changing or modifying the parameters in lower layers according to the weather, cost, user demands and so on.

On the first layer, droop control is embedded with voltage/current control in DC microgrids. Adding droop loop in voltage-controlled sources is necessary because it can not only reduce the circulating current between DESs, but also implement current sharing [8][9][10][11] by setting different droop coefficients. Besides, droop control has advantages in regulating energy storage systems, such as batteries and supercapacitors. For example, the state of charge (SoC) of batteries can be utilized to modify the droop coefficient to get a better performance in power sharing between the energy storages. SoC based adaptive droop control methods were presented in coordinating multiple battery banks [12][13][14], multiple supercapacitors [15][16], and hybrid energy storage [17][18]. Droop control can also combine with communication links to realize power regulation directly. However, once the communication link fails, it lacks the ability to regulate and manage the power distribution.

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F. Li and Z. Lin are with the School of Engineering and Applied Science, Aston University, Birmingham, B4 7ET, U.K. (e-mail: lif12@aston.ac.uk and z.lin@ieee.org).

Z. Qian and J. Wu are with the College of Electrical Engineering, Zhejiang University, Hangzhou, 310027, China (e-mail: zhongnanqian_ee@zju.edu.cn and eewjd@zju.edu.cn).

W. Jiang is with the School of Energy and Power Engineering, Yangzhou University, Yangzhou, 225127, China (e-mail: weijiang@ieee.org).

On the second layer, the common DC bus voltage can be used to regulate the power distribution among DESs. Typical methods are voltage level signaling (VLS) and DC bus signaling (DBS) [19][20]. Conventional VLS methods sectionalize the working voltage windows for dedicated DESs. This method utilizes the inner current loop saturation to realize the voltage drop. When the load increases, DESs will step into current limitation mode, so the DC bus voltage decreases as the load increases until it reaches the next working voltage window to wake up another DES to supply the load. DBS method is developed from VLS methods, which adds a droop loop in each working voltage window, and adjusts the load sharing automatically. However, DBS method has limited number of the working voltage windows that can be applied in a DC system. Based on DBS control method, many mode-adaptive decentralized control methods are proposed [21][22][23]. These methods use DC bus voltage as indicator to adjust the DESs according to the load condition. However, DESs state information exchange cannot be achieved. The work presented in [24] uses various DC bus voltage levels as signaling to regulate energy storage devices. Active DC bus signaling only can be achieved by the master module, but not slave modules. Besides, there are many DC bus signaling voltage levels involved in this method, which introduces large voltage gap and lower DC bus voltage quality.

Adding communication links on the third layer is a proficient way to manage DESs in a DC microgrid, so that the control system can modify the parameters or switch ON/OFF the interface converters for different scenarios. However, the failure of communication links is a major concern in many reported literatures [3][6]. Implementing communication functions without external communication links has been studies in many reported literatures. Conventional power line communication (PLC) [25] needs additional circuits to modulate signals to the power line, and additional circuits to demodulate signals. Power/signal transfer methods proposed in [26][27] are similar to PLC method. The common DC bus is used as the communication link, with the novelty of integrating the signal modulation into the power electronics converters. The disadvantages are signal demodulation circuit is still needed, and advanced microprocessor is needed to do digital signal processing, such as DFT (Discrete Fourier transform).

In this paper, a dual-window DC bus interacting (DBI) method is proposed for DC microgrid control in case of communication links failure or unavailability. This method is applied in a master-slave (M-S) control scheme for DC microgrids. The master module acts as a voltage source converter, and all slave modules act as current source converters to participate in the power regulations within the DC microgrid. The common DC bus voltage can be interactively regulated by the master or slave modules in a designed manner, so signaling over the interaction period can be achieved. Via information exchange, the master module is able to know the availability of slave modules, and sends command signals to control slave modules. In addition, slave modules can also inform their unavailability to the master module, such as low power supply ability or being plugged out. Therefore, a two-way signaling can be achieved. Only two voltage windows are involved in the proposed DBI method, so large voltage gaps in conventional DBS methods are avoided.

Compared with the power/signal transfer method proposed in [26-27], the proposed DBI method is a different way to implement communication between power converters through common DC bus. It is based on droop control and DC bus signaling. It uses sampled DC bus voltage and current to achieve active signaling, which are commonly measured for power converter's closed loop control. It has the advantages of no extra hardware cost, and no complicated digital signal processing, so low cost microprocessor can be used. The limitation is that the communication speed is slower, and the DC bus voltage is disturbed during the signaling period.

The rest of this paper is organized as follows. In section II, the working principle of the proposed dual-window DBI strategy is presented. Control blocks and algorithm state machine are discussed in section III. The experimental results are presented and discussed in section IV. Finally, the conclusions are given in section V.

II. Analysis of the DBI Working Principle

The proposed DBI method modifies conventional DBS methods, and takes the advantage of droop control in plug-and-play performance. It can achieve two-way signaling between power converters through the common DC bus without any additional circuits.

A. Discussion of Droop Curves

In the proposed DBI method, only two DESs will be involved in information exchange at the same time. The equivalent two-node circuit is shown in Fig.2. Assuming there are two droop curves applied in this two-node DC system, the droop equations are shown as equation (1).

$$V_k' = V_k^* - I_{ok}R_{vk}, \quad k \in \{1,2\} \tag{1}$$

where the V_k' is the reference voltage for the voltage loop, V_k^* is the floating voltage, I_{ok} is the output current of interface converter and the R_{vk} is the droop coefficient (or virtual resistance).

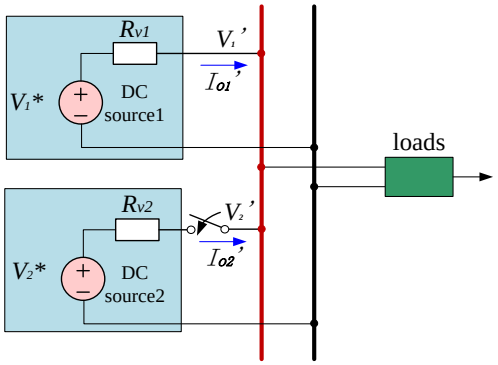

Fig.2. Two-node equivalent circuit.

When two converters are parallel-connected, which means $V_1' = V_2'$ (neglect the line impedance), therefore, equation (2) can be attained.

$$I_{o1} = \frac{V_1^* - V_2^*}{R_{v1}} + \frac{R_{v2}}{R_{v1}} I_{o2}, (R_{v1} \neq 0) \quad (2)$$

There are several possible droop curves for these two DC sources as shown in Fig.3-5.

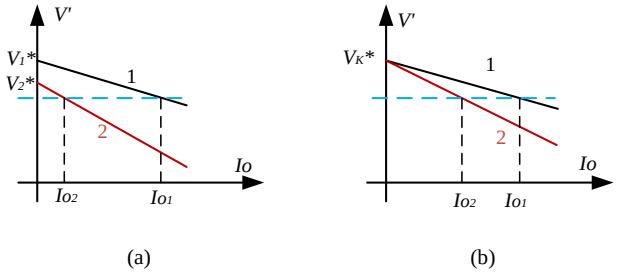

Fig.3. (a) droop curves with different floating voltages and droop coefficients; (b) droop curves with same floating voltage but different droop coefficients.

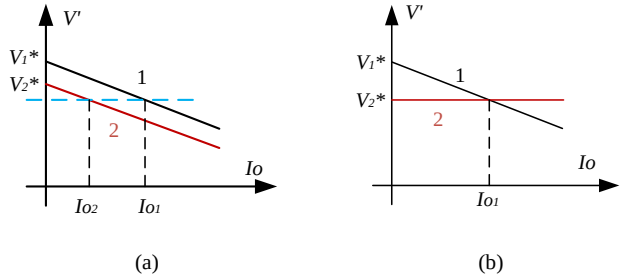

Fig.4. (a) droop curves with different floating voltages but same droop coefficient; (b) droop curves with zero droop coefficient and point of intersection at right side.

Fig.3 (a) shows the general droop curves of both sources. The current-voltage relationship is as shown in equation (2). There is no clear relationship between the DC bus voltage and currents of the DC source 1 (DS1) and the DC source 2 (DS2) when DS2 is connected or disconnected, so it is not applicable for the proposed dual-window DBI method.

Fig.3 (b) shows typical droop curves. In this figure, both DC sources have the same floating voltage, which is $V_1^* = V_2^*$, and the current sharing can be easily attained as equation (3) shows.

$$I_{o1} = \frac{R_{v2}}{R_{v1}} I_{o2} \quad (3)$$

Once DS2 is connected, the DC bus voltage will be slightly increased because the load current is shared by DS2. However, the new DC bus voltage level is uncertain. Different sources can lead to different voltage levels after being connected. Besides, the load change can also lead to a DC bus voltage change, which might result in the DC bus voltage misinterpretation. Therefore, this type of droop curves is not applicable for the proposed dual-window DBI method.

Similarly, the type of droop curves shown in Fig.4 (a) is not suitable for the proposed dual-window DBI method either, even though it has a relative constant relationship between current sharing as equation (4) shows.

$$I_{o1} = \frac{V_1^* - V_2^*}{R_{v1}} + I_{o2} \quad (4)$$

Fig.4 (b) shows a scenario when one of the droop coefficient is zero. Assuming that the master module is implemented with droop curve 1 at the initial state, when DS2 is connected, the DC bus voltage will be pull down at V_2^*, and the current in DS1 will be held at I_{o1}, while the current in DS2 will be adjusted by the load.

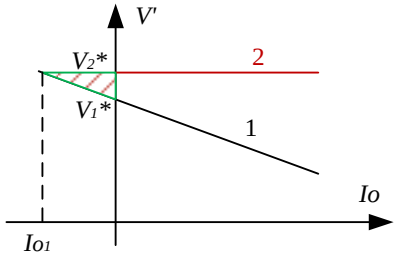

Fig.5. Droop curves with zero droop coefficient and point of intersection at left side.

Fig. 5 shows another scenario with a zero droop coefficient. Similarly, if droop curves shown in Fig.5 are applied, the DC bus voltage will be lifted to V_2^* when DS2 is connected.

Theoretically, both droop curves shown in Fig.4(b) and Fig.5 can be applied in the proposed DBI method. However, for Fig.4(b), when DS2 is connected, the DC bus voltage will be pulled down by DS2, and the current in DS2 is uncertain. If the load is light, the current in DS2 could be negative. It is not a problem if DS2 is a rechargeable battery, but it is unacceptable if DS2 is a renewable power source such as PV. As for Fig.5, the current in DS1 is always negative when DS2 is connected, so the current in DS2 is always positive, which is good for the DES that only can supply the power, such as PV. Therefore, droop curves shown in Fig.5 are more suitable for the proposed DBI method. The master module is a rechargeable energy storage, and PV, rechargeable battery, and supercapacitor can all be configured as the slave modules.

B. Working Principle of the Proposed DBI Method

Considering the droop curves shown in Fig.5, it is possible to implement dual-window DBI through a proper setting of the working voltage window and signaling voltage window. The working voltage window is designed for the normal working conditions while the signal voltage window is for information exchange between DESs.

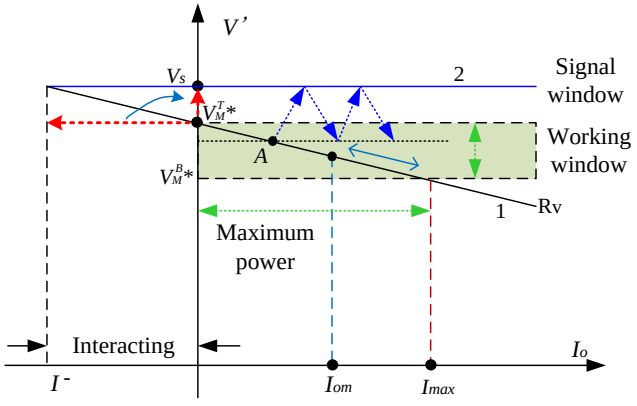

Fig.6. Droop curves for proposed DBI method.

The proposed DBI method is applied to M-S control for DC microgrids. During the normal operation, the master module is mainly under droop control within the predefined working voltage window, while slave modules work under constant power mode. During the signaling period, such as when a slave module is connected, the slave module will work under constant voltage mode, actively take over the DC bus voltage control and lift it at signal window with predesigned signal series for signaling. After information exchange completed, the slave module will step into power control mode. For example, for the PV generation, the final working mode is maximum power point tracking (MPPT), and for the batteries, the final working mode is SoC based current-control mode. Due to the mechanism of M-S control, if the master module is unavailable, the system will be deteriorated to an unmanaged droop control. Besides, the interacting period as is shown in Fig.6 will also reduce the DC bus voltage quality as a trade-off.

Fig.6 redraws the droop curves of the proposed DBI method. The master module works under the droop curve 1 with a non-zero droop coefficient (R_v) while the slave module works under droop curve 2 with a droop coefficient of zero. As for the master module, V_M^{T*} is set as the floating voltage reference. The working voltage window is set between V_M^{B*} and V_M^{T*}. V_s is set for the signaling voltage level window. For all slave modules, V_s is embedded for informing the master module their availability. Therefore, the voltage reference (V_M^{T*}) in the master module is as equation (5) shows.

$$V_M' = V_M^{T*} - I_{oM} R_v \tag{5}$$

Theoretically, once the slave module is plugged in, it will generate a negative interacting current (I^-) in the master module if without any processing as shown in the Fig.3. The interacting current can be written as equation (6).

$$I^- = \frac{V_M^{T*} - V_s}{R_v} < 0 \tag{6}$$

For the power balance consideration, the power capability in a slave module should satisfy the following equation (7).

$$P_s \geq V_s \cdot |I^-| + P_L \tag{7}$$

where the P_s is power capability of the slave module, and P_L is the load power.

In this period, the slave module needs to supply both interacting power and load power. Besides, for the real scenario, a negative current in the master module is not desirable, which can lead to unnecessary power exchange, especially for energy storage slave modules. Therefore, this negative current can be modified through setting the master module to work under current mode during the interacting period. As shown in the equation (6), the interacting current in the master module is negative. But if setting the master module to work under current control mode during the interacting period, the interacting current will be controllable. It is applicable as long as the master module detects the signal voltage level. The advantage by conducting this lies that the current reference in the master module can be set positive (or zero) during the interacting period, so that it helps the slave module to share load in case of the unavailability of the slave module. So the power balance in the slave module can be obtained in equation (8).

$$P_s^* = -V_s I_M + P_L \leq P_L, (I_M \geq 0) \tag{8}$$

where I_M is the reference current during the interacting period, P_s^* is the power output of the slave module. Therefore, the load requirement for the slave module can be relieved.

In order to avoid unnecessary power exchange of the master module providing power to the slave module, the current reference should satisfy the following equation (9).

$$I_M < \frac{P_L}{V_s} \tag{9}$$

In this research work, it is assumed that all the power generation modules used are able to supply power to the load during the interacting period ($P_L \leq P_s$). The impact of negative interacting current will be discussed in the section IV Part B.

C. Signal Series Configurations

The DC bus voltage is initially controlled by the master module, for example, the operation point *A* in Fig.6. When a slave module is plugged in, the DC bus voltage will be controlled by the slave module. The slave module will lift up the DC bus voltage at V_s to inform the master module its availability. The signal series (protocol) used in this research work are designed as shown in Fig. 7.

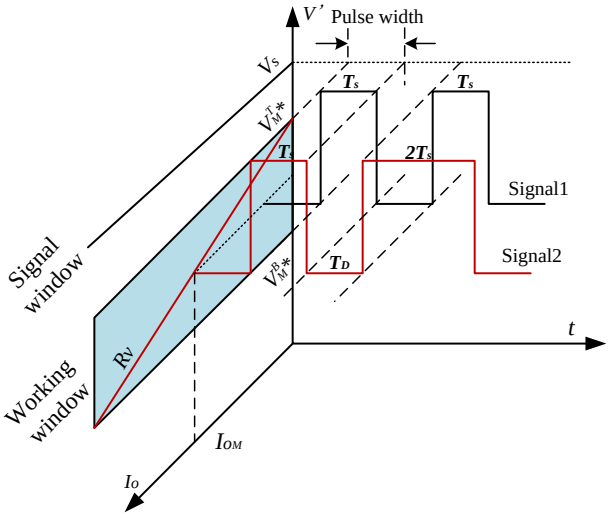

Fig. 7. Signal series arrangement for information exchange.

When the slave module is plugged in, the DC bus voltage will be controlled by the slave module at V_s for a period of T_s, after a delay period T_D, the DC bus voltage will be controlled by this slave module at V_s for a period of T_s again. During the delay T_D, the DC bus voltage is regulated by the master module.

In this signal series, the DC bus voltage is only pulled up by the slave module twice, which means two bits' information in total are used. The number of the pulse can be increased if dealing with more DESs or functions. This will be further discussed in the Part E of this section.

Signal 1 and 2 shown in Fig.7 can be generated by the slave

modules or the master module. If the signal 1 is generated by a slave module (assume it is labelled as S1), it means the slave module S1 is available, then this signal can be detected by the master module through the common DC bus, and the master module will know the availability of the slave module S1, and labels this slave module in its own control algorithm.

If the signal 1 is generated by the master module, it is to wake up the slave module S1. If the signal 2 is generated by the slave module S1, it means this slave module will be disconnected due to some reasons, such as low SoC for a battery module or being plugged out. If the signal 2 is generated by the master module, it indicates that the master module will actively switch off the slave module S1.

D. Discussing the selection of V_s and T_s

The proposed DBI method does not need any additional circuits to realize signaling, and only needs to regulate the DC bus voltage in a designed manner to operate the system. Key parameters in the proposed method are the signal pulse amplitude V_s and the signal pulse width T_s.

The signal pulse amplitude V_s can directly affect the DC bus voltage level, and has the potential risk to affect the system stability. Assuming the system parameters are in Per Unit (PU), such as V_{bus}^{PU} for the common DC bus voltage and V_s^{PU} for the signal voltage, then based on conventional DBS methods [18, 24], let arbitrarily

$$V_s^{PU} = 1.05V_{bus}^{PU} \tag{10}$$

The signal pulse amplitude lower than this value is acceptable as long as the noise from the DC bus voltage does not affect the signal and leads to the misinterpretation. While if the signal pulse amplitude is set too large, the stability issues need to be considered. The close loop compensator needs to be redesigned according to the signal pulse amplitude rather than the normal working voltage, because the phase margin may not be large enough to guarantee the stable operation over the signal interacting period.

The selection of T_s depends on the control compensator and soft start time. The step response time of an interface converter normally ranges from units *ms* to tens *ms*. For Boost-based power converters, the range of soft start time is quite dependent on applications; it thus makes T_s range from tens *ms* to hundreds *ms*. For Buck-based power converters where no soft start is needed, they can make the interacting period faster, and a higher data exchange rate can be achieved.

E. Discussion of Expandability

The proposed DBI method is expandable to a DC microgrid with more DESs, and can deliver more information with a more complicated communication protocol design.

There are two possible methods to expand signal series. Firstly, the number of pulses can be increased according to different situations. For example, if we use three pulses, it will have three states available to be defined by users. Generally, if we use n pluses, it will have $C_n^1 = n$ states available to be defined by users. However, more pulses will extend the period of signal exchange and limit its ability to regulate great amount interface converters. The other method is to use different pulse width T_s. Assuming there is a series of $T_{s1,}T_{s2,}\cdots T_{sn}$ functions as pulse signals, and two bits for example, it will have $C_2^1C_2^1 = 4$ states to use. Generally, for m bits, it will have n^m states, as equation (11) shows, for user to define

$$\underbrace{C_n^1C_n^1C_n^1\cdots C_n^1}_{m} = n^m \ \ (n \geq 2) \tag{11}$$

Compared to the first method, the number of available states is significantly increased with limited number of bits.

The expandability discussed above has been experimentally validated in this paper. Two bits and two pulses T_s are involved to combine interacting signals. The signal distribution is shown in Table I. Signal 1 and signal 2 are for the slave module S1, which are same as shown in Fig.7, and signal 3 and signal 4 are for the slave module S2, which share same function command as the slave module S1. Experimental results can be found in Section IV, Part C.

Protocol designs for more DESs with superiority control functions are feasible with the proposed dual-window DBS method, but it is out of the scope of this paper, which mainly focus on the feasibility study of the proposed DBI method.

TABLE I
SIGNAL SERIES FOR TWO SLAVE MODULES

Signal		Pluse1	Pluse2	Generated by slave	Generated by master
Slave module1	1	T_{s1}	T_{s1}	Loaded	Switch ON S1
	2	T_{s1}	T_{s2}	Low SoC/ self-OFF	Switch OFF S1
Slave module2	3	T_{s2}	T_{s2}	Loaded	Switch ON S2
	4	T_{s2}	T_{s1}	Low SoC/ self-OFF	Switch OFF S2

Note: S1 is slave module1, S2 is slave module2, $T_D = T_{s1}$.

III. CONTROL ALGORITHM

A. Analysis of Control Diagram

A DBI based system control diagram is shown in Fig.8. The master module is under droop control. The working voltage window is set between V_M^{T*} and V_M^{B*} with a droop resistance R_v. The inner loop compensator is shown in equation (12) and the outer loop compensator is shown in equation (13).

$$G_{ci} = G_i\frac{1+\frac{2\pi f_z}{s}}{1+\frac{2\pi f_p}{s}} \tag{12}$$

$$G_{cv} = G_v(1+\frac{2\pi f_{zv}}{s}) \tag{13}$$

All the parameters involved in Fig.8 are listed in Table II. The proposed control algorithm does not change the primary controller. Therefore, the stable operation is assured. This has been validated by immunity test in experiment part of this paper.

When the slave module S1 is plugged in, it will take over the DC bus voltage control. After sending an availability signal, it will go to the sleep mode, and wait for the master module to send a wake-up signal. After receiving a wake-up

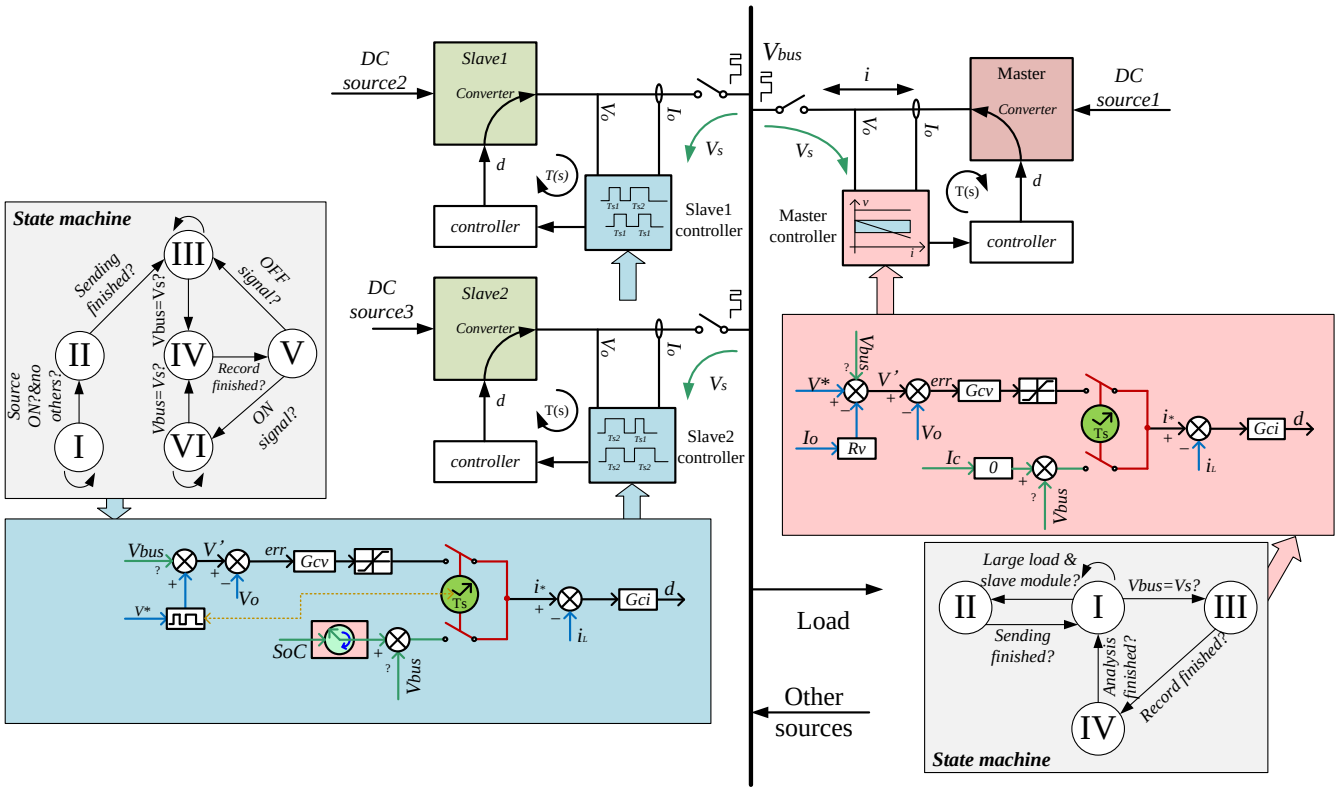

Fig. 8. Control blocks of whole system.

signal, it then goes to the SoC based current control loop. As discussed in section II, all the energy storage devices have the same control method and the only difference is the signal pulse width T_S. For example, if the slave module is a PV source, the SoC based current control need to be changed to MPPT control. Every slave module has a short delay for detecting the DC bus voltage before interacting the DC bus voltage control in case of interrupting with other slave modules.

TABLE II
PARAMETER VALUES IN CONTROL

PARAMETERS	VALUE	PARAMETERS	VALUE
L/ C/f_s	250UH/470UF/25KHZ	V_M^{T*}	48V
$G_i/f_z/f_p$	0.3/1KHZ/6.25KHZ	V_M^{B*}	46V
G_v/f_{zv}	49.2/83.3HZ	V_s	49V
T_{s1}/T_{s2}	400MS/800MS	R_v	1Ω

B. Explanation of State Machine

The proposed control method was implemented in a micro-processor TMS320F28335.

For the master module, there are four states involved to ensure a smooth operation, as shown in the right side of Fig. 8.

State I: the DC bus voltage is regulated by the droop controller of the master module. A slave module register is used to register

the available slave modules. When encountering a heavy load or light load, it will move to state II. When the DC bus voltage is the signal voltage level V_s, it will move the state III. Normally, the master module works under state I to supply the power to the load.

State II: the master module sends the signal to wake up the slave module when the load is heavy or shut off the slave module when the load is light. After sending the signal, it will move back to state I.

State III: the master module is recording the received signal. After the recording completed, it will move to state IV.

State IV: the master module will analyze the recorded signal. When it is completed, it will move to state I.

For the slave modules, there are six states involved, as shown in the left side of Fig. 8.

State I: The slave module is waiting for being plugged-in to the DC microgrid. Once plugged in and if the DC bus voltage is not regulated by other slave modules, it will move to state II. If the DC bus voltage is regulated by other slave module, this module will wait until this process finished. So that only one module is able to set signaling voltage at one time.

State II: the slave module will send signal by controlling the DC bus voltage at V_s. Once finished, it will move to state III.

State III: the slave module is under sleep mode, and detecting the DC bus voltage to see if any wake-up signals sent by the master module. If detected signal V_s, it will move to state IV.

State IV: the slave module is recording the received signal. After completed, it will move to state V.

State V: the slave module will analyze the received signal. If it is a wake-up signal, it will move to state VI. If it is a shut-off signal, it will move to state III.

State VI: the slave module will work under function mode as mentioned before. Meanwhile, it also detects the DC bus voltage to see if any shut-off signal from the master module.

IV. Experimental Validation

A small-scale DC microgrid experiment system was used to validate the proposed method, and its block diagram is shown in Fig.9. The experimental system contains three battery modules, a PV source and an electronic load.

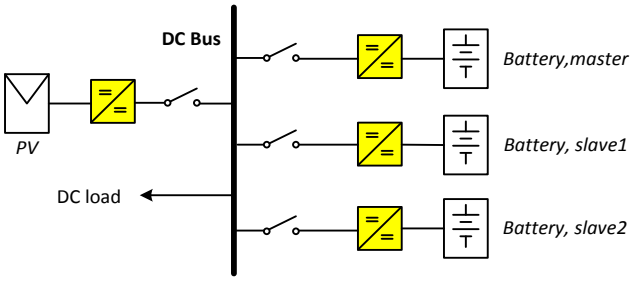

Fig. 9. Block diagram of experimental set-up.

The experimental test has three parts. The first part focuses on the validation of the proposed dual-window DBI method. In this part, the experimental system includes a master module and a slave module. The second part is to validate the immunity to time varying loads (TVL) and time varying sources (TVS). The third part is to validate the expandability, so the experimental system includes one master module and two slave modules.

For the illustration purpose and converter availability, the parameters involved the experiments are listed in Table III.

TABLE III
PARAMETER USED IN EXPERIMENT

Type	Value
Battery, master	24V
Battery, slave1	24V
Battery, slave2	24V
PV power	0~100W
DC electronic load	0~400W
Interface converter	Bidirectional boost converter /150W

A. Two-node Experimental Validation

Fig.10 shows the experimental result for the case of initial light load. Initially, the master module works under droop control mode. When a slave module is plugged in, it shows the DC bus voltage is regulated to 49V twice with a pulse width of 400ms by the slave module, which is detected by the master module. Because the load is light, so the master does not send signals to wake up the slave module. As the load increases, the output current of the master module increases as well. Once reaching the up-threshold, the master module sends a wake-up signal to the slave module. Once receiving the signal, the slave module will work based on its own SoC. In this case, it discharges 0.5A to supply the load.

Fig.11 shows the experimental result for the case of initial heavy load. After the slave module is plugged in (two 49V pulses with 400ms), a wake-up signal is sent back from the master module to the slave module after 1 second delay. When the slave module is at low SoC, which means that it cannot supply the load any more, it will send a log-off signal to the master module to inform it will be disconnected. A log-off signal is made up by two pulses with 400ms and 800ms pulse width at 49V, as shown in Fig.11. Therefore, the master module will supply the power to the load alone.

It can be seen from above experimental results that the proposed DBI method causes the DC bus voltage varies, which sacrifices the quality of the DC bus voltage.

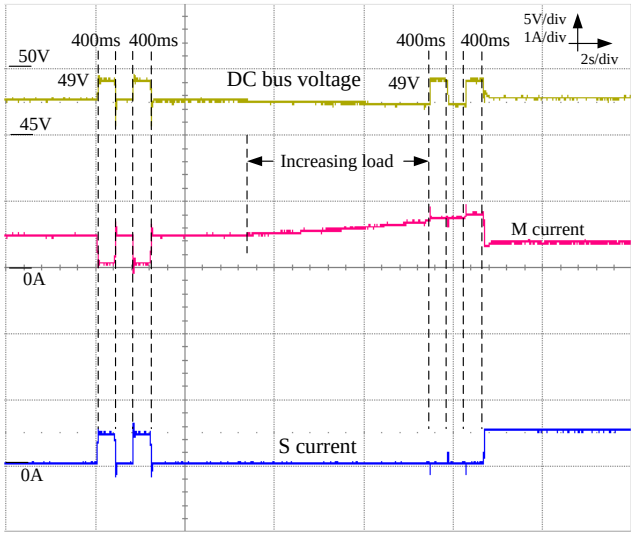

Fig. 10. Initial light load with a slave module plugged in. Increasing the load to wake up the slave module.

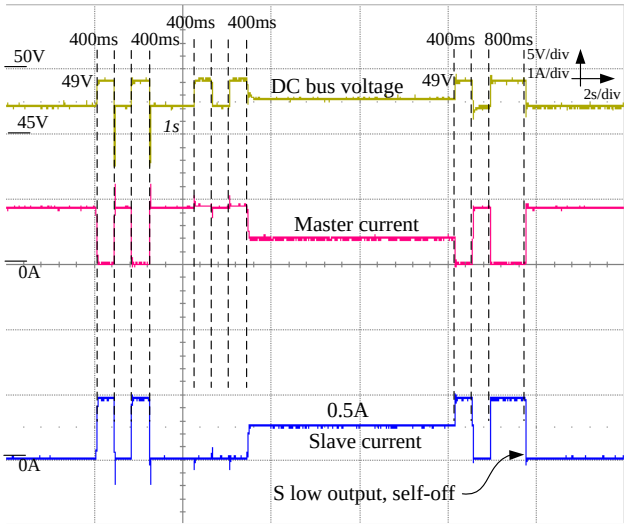

Fig. 11. Initial heavy load with a slave module plugged in and the slave module self-shut-down because of low SoC.

B. Immunity test of TVS and TVL

Fig.12 shows the time varying source experimental result. The maximum power point voltage of PV is 25V, and the maximum power is 100W. The solar irradiance varies from 100W/m^2 to 1000W/m^2. It can be seen that the signaling process can be conducted over the irradiance variation period.

Time varying load experimental result is shown in Fig.13, where the load changes between 30W and 100W. It can be shown that the signaling process can be completed no matter in MPPT period from PV source or load decrease period. The signal is configured to charge the slave battery at 1.2A according to the battery's current SoC.

The most severe situation is that the source and load change at the same moment. Fig.14 shows the experimental result with a mixed time varying source and load condition. It can be noticed that TVL and TVS do not have impact on the proposed DBI method, and signaling interacting period can be achieved as long as the converter feedback compensator is well designed.

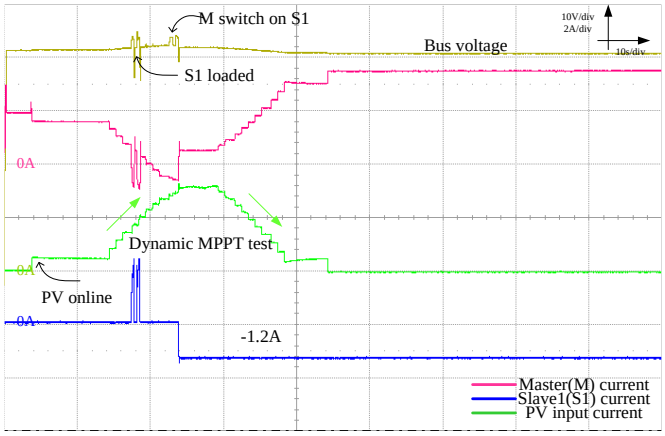

Fig. 12. Time varying source test result.

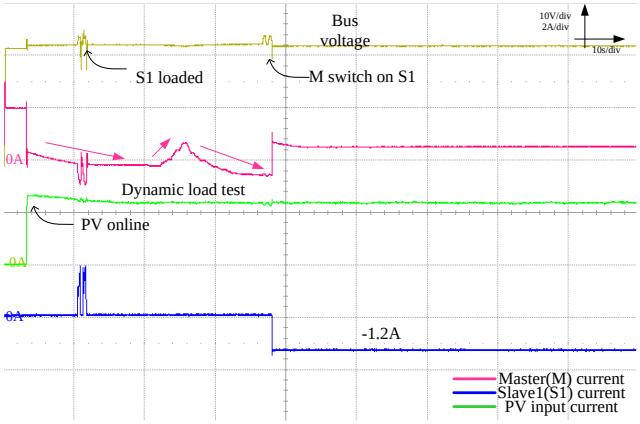

Fig. 13. Time varying load test result.

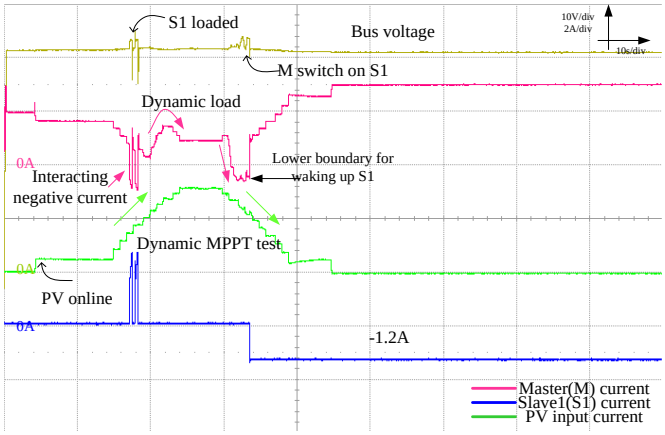

Fig. 14. Mixed dynamic source and load test.

In this case, the interacting negative current was not modified in the controller, it can be seen that the interacting current in the slave module needs to be large enough to compensate the negative current in the master module, which is not necessary. The following case C will show the experimental result with zero current in master module during the interacting period as mentioned in Section II, Part B.

C. Experimental Validation for Expanding to Three Nodes

Fig.15 shows experimental waveforms when the slave module S1 is plugged in and then the slave module S2 is plugged in. The master module did not wake up both slave modules due to the light load. If the load is heavy, once one of the slave module is plugged in, the master will wake it up to share the load, which is shown in Fig.16. Continuing to increase the load, the master module will wake up the slave module S2 if it is plugged in, as shown in Fig.17.

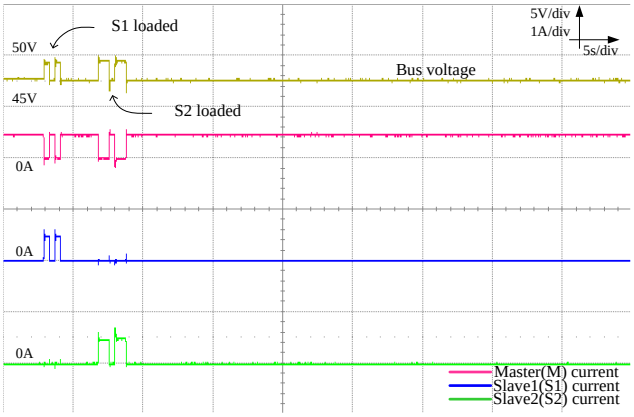

Fig. 15. Initial light load with two slave modules (S1, S2) plugged in.

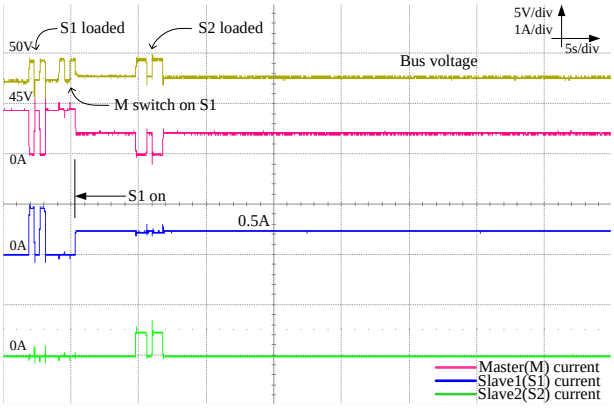

Fig. 16. Initial heavy load with S1 plugged in and the master wakes up S1, then S2 plugged in.

If the slave module S1 is at low SoC condition or going to be plugged out (a button on control board is needed), it will actively pull up the DC bus voltage to 49V for 400ms and 800ms to inform the master module that it will be disconnected, as shown in Fig.18. The slave module S1 pulls up the DC bus voltage at t1 with correspondent log-off signal. Meanwhile, the master module knows the slave module S2 is still available, so after the slave module 1 is disconnected, the master module pulls up the DC bus voltage level to wake up the slave module S2 to supply the power to the load.

Fig. 19 also shows that the master module can actively shut off slave modules. Firstly, the slave module S1 is plugged in and the master module wakes up the slave module S1 due to the heavy load. Then slave module S2 is plugged in at t1. The

increasing load makes the master module pull up the DC bus voltage and it wakes up the slave module S2. Decreasing the load at t2, the master module will pull up the DC bus voltage to send shut-off signal once the current in the master module reaches the lower threshold. Finally, the slave module S1 is switched off by the master module with higher priority.

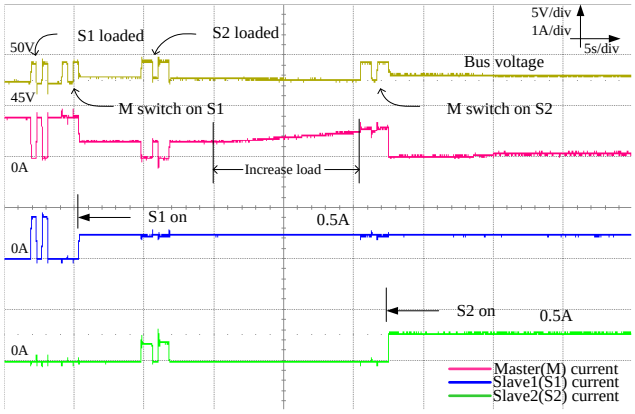

Fig. 17. Initial heavy load with S1 plugged in and the master wakes up S1, then S2 plugged in. increasing load to wake up S2.

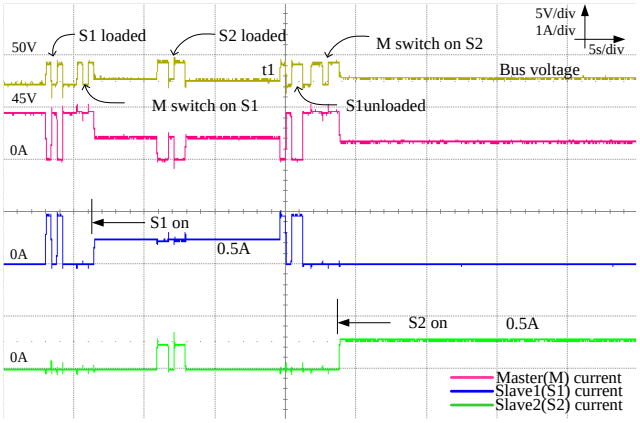

Fig. 18. Initial heavy load with S1 plugged in and the master wakes up S1, then S2 plugged in. when S1 is unloaded, self-shut-off then the master wakes up S2.

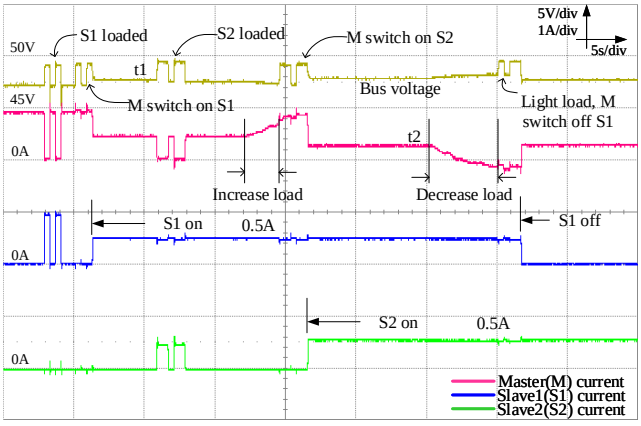

Fig. 19. Initial heavy load with S1 plugged in and the master wakes up S1, then S2 plugged in. Increasing load to wake up S2. When load decreases, the master switches off S1.

V. Conclusions

In this paper, a novel dual-window DC bus interacting (DBI) method was proposed for the applications of coordinating the distributed energy sources in a DC microgrid. It combines the concept of conventional non-communication based droop and DBS control methods. Compared with the previous works, a two way signaling between DESs can be achieved. Besides, the proposed method reduced voltage windows, and as a tradeoff, it involved a longer DC bus voltage interacting period. The working principle of the proposed DBI method was explained, the system control block diagram and the state machine of the control algorithm were illustrated. The immunity and expandability of the proposed method were validated experimentally. A simple Master-Slave DC microgrid control system without communication link was implemented to approve the feasibility of using the proposed DBI method for DC microgrid control.

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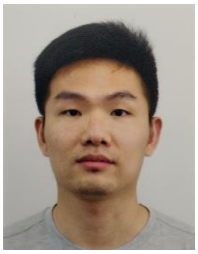
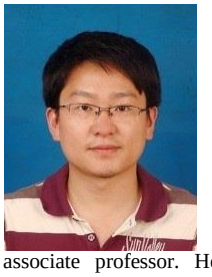


Fulong Li (S'16) received the B.S. degree in electrical engineering from Yangzhou University, Yangzhou, China, in 2015. He is currently working toward the Ph.D. degree in Electrical, Electronic and Power Engineering, Aston University, Birmingham, UK.
His current research interests include control methods and stability analysis of power electronics converters applied in DC microgrids and distributed power systems.

Zhengyu Lin (S'03–M'05–SM'10) received the B.Sc. and M.Sc. degrees from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1998 and 2001, respectively, and the Ph.D. degree from Heriot-Watt University, Edinburgh, U.K. in 2005. He is currently a Lecturer in Electrical, Electronic and Power Engineering with Aston University, Birmingham, U.K., and an EPSRC-UKRI Innovation Fellow.
His research interests include power electronics and its applications in renewable energy, energy storage, motor drives and microgrids.

Zhongnan Qian received the B.Sc. degree in electrical engineering in 2014 from Zhejiang University, Hangzhou, China, where he is currently working toward the Ph.D. degree in electrical engineering.
His research interests include wireless power transfer and communication techniques applied in power electronics.

Jiande Wu (M'11) was born in Zhejiang, China, in 1973. He received the B.Sc., M.SC and Ph.D. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1994, 1997 and 2012, respectively. Since 1997, he has been a faculty member at Zhejiang University, where he is currently an associate professor. From 2013 to 2014, he was an academic visitor at the University of Strathclyde, Glasgow, U.K.
His research interests include power electronics control, distributed power electronics system and fieldbus communication.



Wei Jiang (S'08–M'10) was born in Yangzhou, China. He received his B.S. degree from Southwest Jiaotong University, Chengdu, China, in 2003, and his M.Sc. and Ph.D. degrees in electrical engineering from the University of Texas at Arlington in Arlington, Texas, in 2006 and 2009, respectively. From 2007 to 2008, he worked at EF Technologies L.L.C. as a senior design engineer. In 2010, he joined Yangzhou University as a lecturer and founded the Smart Energy Laboratory, where he is currently an associate professor. He was on sabbatical leave in the University of Strathclyde, Glasgow, UK, as a visiting professor in 2015.
His current research interests include digitalized power conditioning to renewable energy and energy storage devices and microscopic analysis of electromechanical energy conversion.