NBTI and HCI models for circuit level aging simulations in different EDA environments

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Abstract

The significance of transistor degradation due to aging mechanisms such as BTI or HCI has increased significantly with the continuous scaling down of CMOS technologies and their presence in safety-critical systems. In order to deliver the reliable systems that the industry currently demands, it is necessary to apply aging simulations in IC design projects. However, the capabilities that are available strongly depend on the EDA environment and tools. In this paper we present the work done in a case study to characterize and model NBTI and HCI degradation for X-FAB's XU035 technology, and we discuss a methodology developed to implement and integrate user-defined aging models for circuit level simulation with consistent results across different design environments.

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1. INTRODUCTION

Technology scaling has continuously improved the performance and lowered the cost of integrated circuits (ICs), but increased reliability challenges since aging mechanisms, such as Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI), have a greater impact in submicron technologies [1], [2]. To ensure a proper IC functionality over its lifetime in the design phase already, it is important to perform aging simulations. These analyses require to have accurate transistor aging models integrated in the design environments.

In this paper, we present our work to create empirical models for HCI and Negative BTI (NBTI) degradation for X-FAB's XU035 technology, and their integration into different electronic design (EDA) environments.

2. THEORETICAL BACKGROUND

Circuit simulations (SPICE) are a standard verification method in IC design projects. Aging simulations extend them to investigate the circuit behavior after a pre-defined time of operation. They are available in different design environments and follow the following flow. (1) The performance of the fresh circuit is evaluated from a regular simulation. (2) From this simulation, the stress conditions (voltage and current waveforms) are extracted for each transistor in the circuit. (3) The degradation of each transistor is computed and the results are captured in a back-annotated netlist that represents the aged circuit. (4) A second simulation allows to evaluate the performance of the aged netlist.

The most important transistor degradation mechanisms are BTI and HCI. Defects in the gate dielectric or at the interface to the channel are the root cause of BTI. Driven by the gate to source voltage V_{gs} and temperature T, the defects are charged and discharged which mainly results in a shift of the device threshold voltage V_{TH} [3], [4]. NBTI is driven by negative V_{gs} and affects PFETs; Positive BTI (PBTI) is driven by positive V_{gs} and affects NFETs, especially at high-κ dielectric materials. Besides degradation, BTI shows a recovery effect after the stress is removed, leading to a partial restoration of the degraded characteristics.

Both NFET and PFET devices are affected by HCI. Carriers flowing through the transistor channel may gain sufficient kinetic energy to overcome the insulator-substrate interface potential barrier, creating interface states, oxide defects or get trapped, leading to a charge accumulation near the gate oxide. HCI degrades multiple transistor characteristics, for instance IDSAT, GMAX, VTH, and sub-threshold swing [5],[6]. HCI does not present a recovery effect and is worst at low temperatures.

Transistor aging models make information on BTI and HCI available for aging simulations. However, standards have not been established yet. In general, empirical models are one approach. They mimic the electrical behavior observed in measurements and can be set up relatively efficiently at the cost of accuracy. Physical models provide another approach that is based on the microscopic effects and therefore more complex and accurate at the cost of effort. For example, the microscopic explanation for NBTI is a recent research topic. Diverse theories explain the origin of NBTI by different mechanisms, such as reaction-diffusion or switching traps [7], [8].

For aging simulations, transistor aging models may adapt selected parameters of the underlying model cards. As an alternative, subcircuits that mainly consist of controlled sources can be designed around the unchanged transistor to model its degradation.

The EDA tools provide basic transistor aging models, but they are tool specific and not consistent as well as very simple or confidential. Their feasibility for a particular technology appears hard to assess.

3. HCI AND NBTI MODELING

Our study captures HCI at the base 5V NFET and NBTI of the base 5V PFET in the XU035 technology. PFET HCI and NFET PBTI are not significant. The
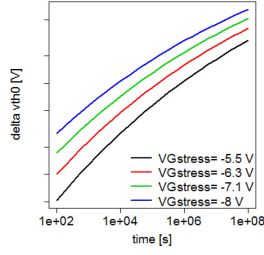
Fig. 1. Predicted evolution of BSIM parameter vth0 due to NBTI

Fig. 2. Predicted evolution of BSIM parameters u0 and rdsw due to HCI

devices were characterized according to JEDEC standards [9] and the stress-measure-stress procedure. For NBTI, the PFET was stressed at high and constant Vgs and at the maximum temperature specified for the technology. BTI recovery was not taken into account. For HCI, the NFET was stressed at high and constant V_{DS} at room temperature, and V_{GS} was set such that the substrate current was at its maximum. During the measurement phases, we recorded multiple characteristics: saturation current IDSAT, linear current IDLIN, maximum transconductance GMAX, constant current threshold voltage VTHI, and extrapolated threshold voltage VTH.

To derive transistor aging models, we set up circuit simulations that mimicked the measurements. We chose to set up the transistor aging models by adapting selected parameters of the underlying BSIM3 models [10] to benefit from the built-in physics of the BSIM model. The parameter selection was based on simulation-based sensitivity analyses to investigate the impact of BSIM parameters on the characteristics above. We achieved reasonable results with the following approaches.

Depending on the gate to source voltage Vgs and the time t, we mapped the PFET NBTI degradation onto the BSIM parameter vth0 with 4 parameters p_1, p_2, p_3, and p_4.

$$\Delta vth0 = p_1 \cdot 10^{\left(p_2 \cdot |V_{gs}|^{p_3} \cdot t^{p_4}\right)} \qquad (1)$$

$$vth0_{aged} = vth0_{fresh} - \Delta vth0 \qquad (2)$$

Note that $vth0_{fresh} < 0$ for a PFET. As visualized in Fig. 1, the model in (1) captures a saturation of the degradation which fits the expectations from physics. Our approach allowed to well represent the measured behaviors of VTHI (see Fig. 4) and the other electrical characteristics.

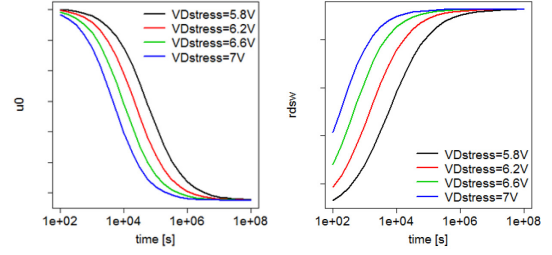The NFET HCI model was setup to capture the degradation in all electrical characteristics: IDSAT,

IDLIN, GMAX, VTH, and VTHI. To our knowledge, such an approach is beyond the state of the art that usually considers one or two characteristics. We defined a general part of the HCI model that depends on the drain to source voltage Vds, the time t, and 5 parameters p_1, p_2, p_3, p_4, and p_5.

$$y' = p_1 \cdot V_{ds}^{p_2} \cdot t^{(p_3 + p_4 \cdot V_{ds})} \qquad (3)$$

$$y = \frac{y'}{1 + p_5 \cdot y'} \qquad (4)$$

To model the observed HCI degradation, we applied (3) and (4) to adapt the BSIM parameters u0, rdsw, and vsat.

$$u0_{aged} = \frac{u0_{fresh}}{1 + y_{u0}} \qquad (5)$$

$$rdsw_{aged} = rdsw_{fresh} \cdot (1 + y_{rdsw}) \qquad (6)$$

$$vsat_{aged} = vsat_{fresh} \cdot (1 + y_{vsat}) \qquad (7)$$

Fig. 2 shows how the BSIM parameters u0 and rdsw evolve over time and stress according to (5) and (6). As for NBTI, the HCI model includes a saturation of the degradation over time t and stress voltage Vds.

4. Integration of aging models into different EDA environments.

As outlined in Sec. 2, EDA tools come with built-in transistor aging models. In addition, they provide application programming interfaces (APIs) to include custom, user-defined transistor aging models. We implement our models into these APIs to consistently support different EDA environments. In this paper, we focus on Cadence and Mentor environments.

Fig. 3 shows the methodology that we employed to implement the transistor aging models. Different EDA tools must deliver the same results and use the
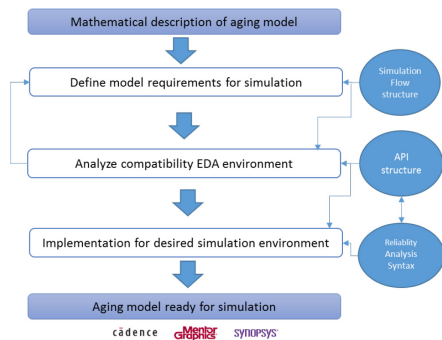
Fig. 3. Necessary steps to integrate aging models
across different EDA environments

same mathematical model description. The necessary information for aging calculation and device degradation in the aged netlist was determined by a detailed analysis of the model requirements. In addition, a compatibility analysis ensured that these requirements were met by the EDA environments, and the specifics of the simulation flows and API capabilities needed to be taken into consideration.

We applied our models in circuit level simulations of single PFET and NFET instances to validate our approaches. We achieved a reasonable accuracy with respect to the measurement data for PFET NBTI and NFET HCI for various stress conditions and in both EDA environments. Selected results are demonstrated in Fig. 4 and Fig. 5. The EDA environments identically evaluate the aging models. Nevertheless, we observe differences between the simulators when evaluating VTHI, VTH, and GMAX (i.e. in the near-threshold regime) degradation. These deviations result from simulator properties, such as their detailed use of BSIM models, post processing capabilities, and, potentially, simulation settings.

5. Conclusions

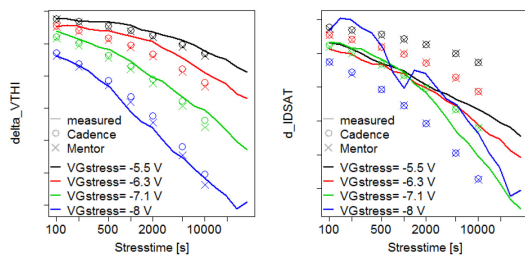In this study, we addressed two aspects of transistor aging modelling: deriving empirical aging models

Fig. 4. Impact of NBTI on PFET VTHI and IDSAT,
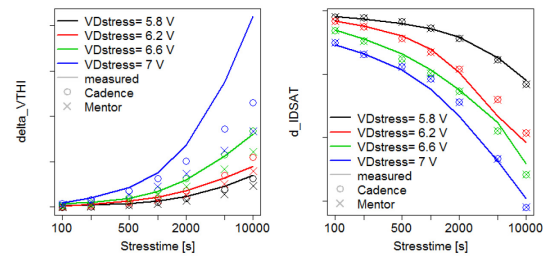comparison of measurements and aging simulations

Fig. 5. Impact of HCI on NFET VTHI and IDSAT,
comparison of measurements and aging simulations

from measurements and consistently implementing these models in different EDA environments. We focused on X-FAB's XU035 technology, in particular on NBTI degradation of the base PFET and HCI degradation of the base NFET.

Our empirical models were set up and calibrated to capture the degradation in multiple electrical characteristics: IDSAT, IDLIN, GMAX, VTH, and VTHI which, to our knowledge, goes beyond the state of the art. The transistor aging models were consistently integrated into two different EDA environments, Cadence and Mentor. Corresponding aging simulations show a good fit between measurement data and both simulation environments.

Improving the model accuracy and supporting further EDA environments might be subjects to future research.

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