Versatile 3D GaN processing for integrated high-aspect-ratio vertical nanodevices

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Since the birth of high-power 2D gallium nitride (GaN) light-emitting diodes (LEDs), immense optimization and investigation have been carried out in the last few years, not only to enhance the material quality and device performance but also to further extend its application realm. InGaN/GaN LEDs have been broadly employed in general illumination and backlight units because of their higher luminous efficacy and longer lifetime compared to conventional light sources. By forming the materials in 3D nanowire (NW) structures, light-switchable sensors can be developed for photoelectrochemical detection of NADH in life sciences [1]. Meanwhile, because of their superior characteristics in switching speed, operation temperature, and power loss, GaN field-effect transistors (FETs) also gain remarkable research interests for power switching applications, in which vertical 3D GaN NW FETs have recently been introduced as a novel device concept [2]. Therefore, by sharing a common material platform, a monolithic integration of multiple 3D GaN-based nanodevices (i.e., LEDs, sensors, and FETs) on a single chip has been considered as an ultimate goal to yield compact smart-optoelectronic sensing systems.

Although GaN nanostructures with a vertical architecture have been successfully created, their processing reliability remains a major challenge. Here, we report on the advanced development of versatile 3D GaN processing that has been applied in various nanodevices (i.e., nanoLED arrays, nanoFETs, and biochemical nanosensors). To fabricate the well-ordered high-aspect-ratio nanostructures, a top-down approach consisting of nanophotolithography and hybrid etching was employed. In this case, both GaN NWs and fins, with smooth a-plane sidewalls, fine morphology, and different material stacks, could be realized down to 50 nm feature size from the subsequent processes of SF_6/H_2-based inductively coupled plasma dry reactive ion etching (ICP-DRIE) and KOH-based wet chemical etching (Fig. 1). As top and bottom surfaces of the structures are distantly separated by about 3.5 – 5 µm, device planarization plays a critical role for the feasibility of top metal contact deposition. Thus, polymer filling with different insulating materials has been carefully investigated (e.g., positive photoresist, spin-on-glass (SOG), and benzocyclobutene (BCB)), in which their results were characterized in scanning electron microscope and confocal laser scanning microscope (Fig. 2). In this case, the height of the spin-coated and cured polymer should be adjusted in regard to the targeted process steps. For the photoresist, the revealed etch rate was ~123nm/min in O_2-plasma based ICP etching at a pressure of 10 Pa (Fig. 3). Moreover, in FET processing, the Cr gate contact was applied on the NW and fin sidewalls as the third electrode besides top (drain) and bottom (source) electrodes after atomic layer deposition (ALD) of thin SiO_2 or Al_2O_3 gate dielectric (Fig. 4(a)). Whereas, for the nanosensors, the filling polymer during planarization has to be removed to realize hanging top contact, so that the freely exposed NW or fin sidewalls can be functionalized with organic molecules as sensitive sensing layers (Fig. 4(b)). Besides their detailed process flow, the performances of the developed 3D devices will be discussed.

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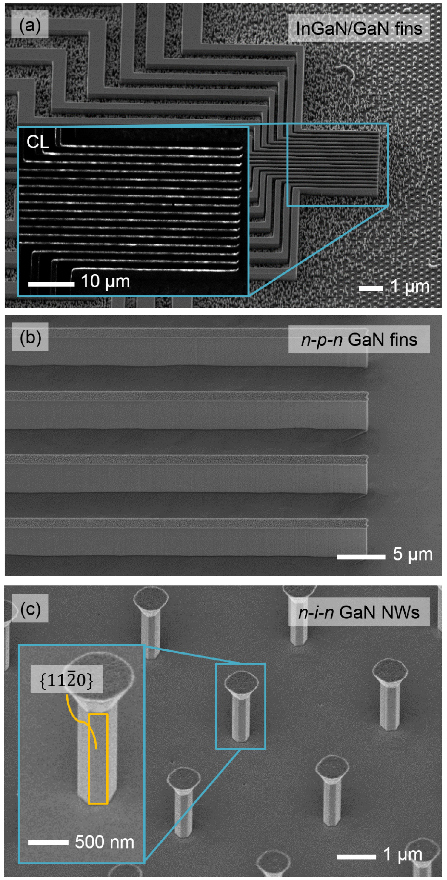

Figure 1. SEM images of various 3D GaN nanostructures produced by top-down approach: (a) 1 µm InGaN/GaN LED microfin array after ICP-DRIE and and its corresponding cathodoluminescence (CL) result (right) showing the monochromatic emission at the peak wavelength of 465 nm; (b) vertical *n-p-n* GaN microfins for vertical finFET after ICP-DRIE and wet chemical etching; (c) vertical n-i-n GaN nanowires (NWs) with smooth a-plane sidewalls.

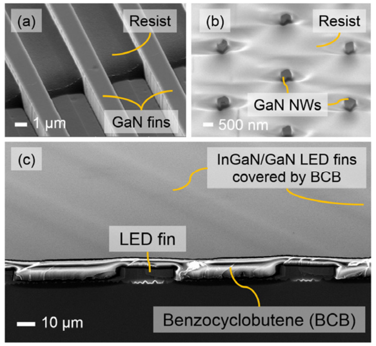

Figure 2. Planarization of 3D GaN nanostructures with polymer filling materials of positive photoresist for (a) fin and (b) NW arrays and (c) benzocyclobutene (BCB) for LED microfin array.

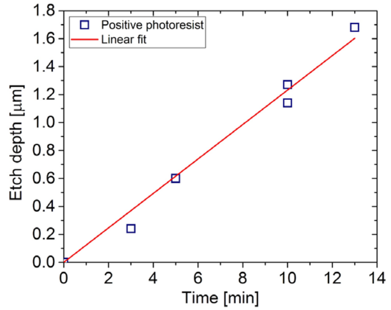

Figure 3. Etch depth of a positive photoresist layer obtained from O_2-based ICP etching at a pressure of 10 Pa for different etch durations.

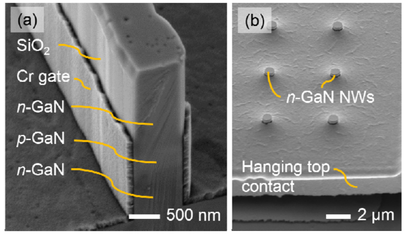

Figure 4. (a) Cr gate at the sidewalls of a finFET. (b) Ti/Cr/Au hanging top contact for vertical NW-based chemical sensors.