BASIC ELECTRONICS

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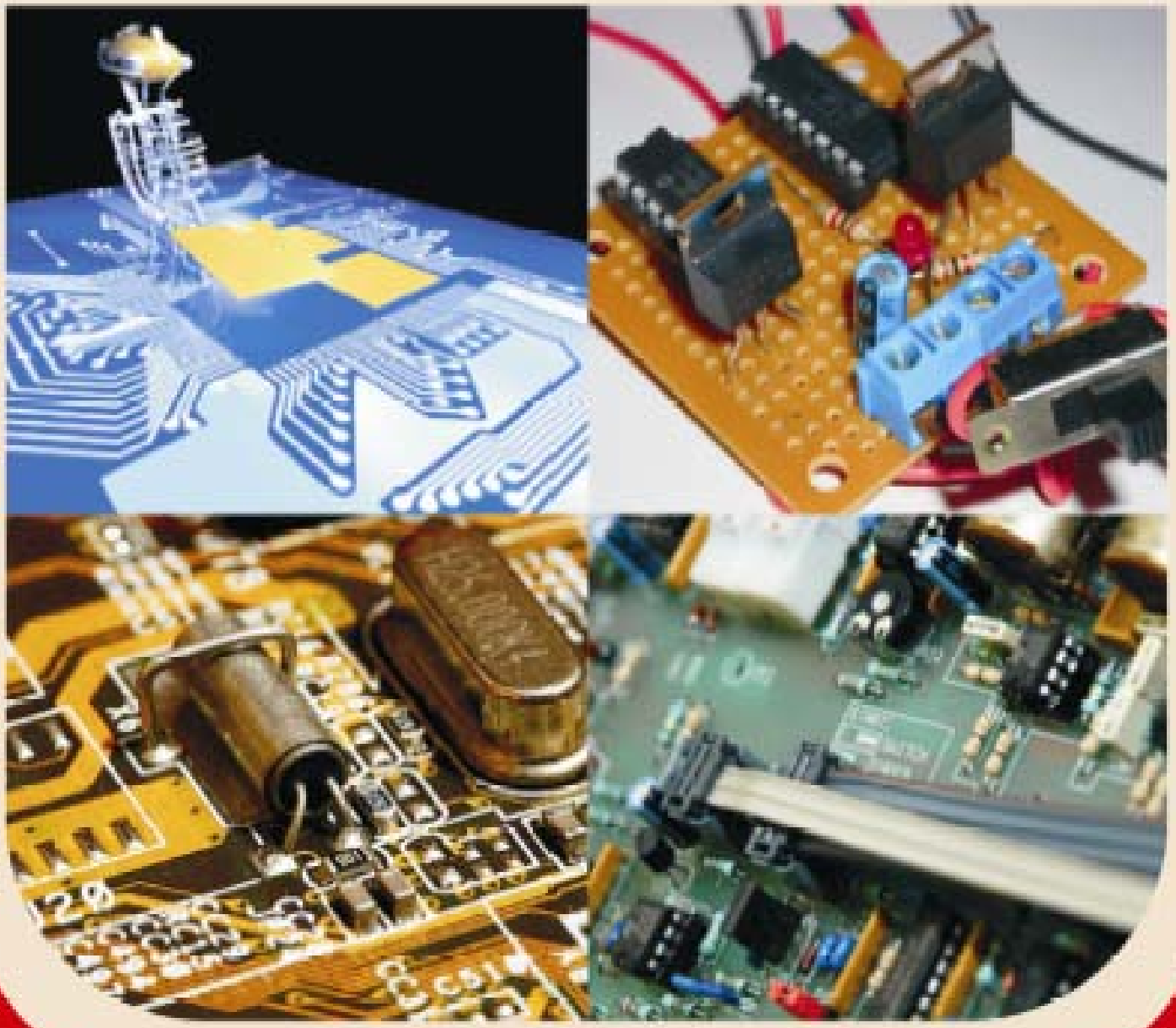

P. S. Aithal

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Detailed Contents

Preface

The purpose of this book is to provide an in-depth information on fundamentals of electronics to the student community to improve their general understanding on the subject. The book has been designed as a textbook for the beginners in all branches of Engineering according to the latest syllabus of Visvesvaraya Technological University, Belgaum, Karnataka. The emphasis is given on basic concepts & fundamental aspects of the functions of electronic components, circuits and devices.

The book has been divided into eight units. The first Unit is **SEMICONDUCTOR DIODES AND APPLICATIONS,** which contains p-n junction diode and its Characteristics and Parameters, Diode approximations, DC load line, Temperature dependence of p-n characteristics, AC equivalent circuits, Zener diodes, Half-wave diode rectifier, Ripple factor, Full-wave diode rectifier, Other full-wave circuits, Shunt capacitor - Approximate analysis of capacitor filters, Power supply performance, and Zener diode voltage regulators. The second Unit is **TRANSISTORS,** which contain Bipolar Junction transistor, Transistor Voltages and currents, amplification, Common Base, Common Emitter and Common Collector Characteristics, DC Load line and Bias Point. The third Unit is on **BIASING METHODS,** which contains Base Bias, Collector to Base Bias, Voltage divider Bias, Comparison of basic bias circuits, Bias circuit design, and Thermal Stability of Bias Circuits. The fourth Unit is on **OTHER DEVICES,** which contains Silicon Controlled Rectifier (S.C.R), SCR Control Circuits, S.C.R applications, Unijunction transistor, UJT applications, Junction Field effect Transistors, JFET Characteristics, and FET Amplifications.

The fifth Unit focus on **AMPLIFIERS & OSCILLATORS,** which includes Decibels and Half power points, Single Stage CE Amplifier and Capacitor coupled two stage CE amplifier, Series voltage negative feedback and Additional effects of Negative feed back, the Barkhausen Criterion for Oscillations, BJT RC phase shift oscillator, Hartley, Colpitts and crystal oscillator. The sixth Unit deals with **INTRODUCTION TO OPERATIONAL AMPLIFIERS,** which includes Ideal OP-AMP, Saturable property of an OP-AMP, inverting and non inverting OP-AMP circuits, need for OP-AMP, Characteristics and applications - voltage follower, addition, subtraction, integration, differentiation and Cathode Ray Oscilloscope (CRO). The seventh Unit contains **COMMUNICATION SYSTEMS & NUMBER SYSTEMS** with Block diagram of communication system, Modulation, Radio Systems, Superhetrodyne Receivers, and decimal system, which includes Binary, Octal and Hexadecimal number systems, addition and subtraction, fractional number, and Binary Coded Decimal numbers. Finally, the eighth Unit focus on **DIGITAL LOGIC**, which includes Boolean algebra, Logic gates, Half-adder, Full-adder, and Parallel Binary adder.

Every attempt has been made to make this book error free and useful for the students. Two sample question papers have been given at the end. Each unit starts with the unit objectives and ends with unit questions, objective type questions and assignment problems. Any constructive suggestion and criticism regarding the improvement of this book will be acknowledged.

—Author

Acknowledgements

I derive immense pleasure in placing on record my deep sense of appreciation, gratitude and indebtedness to CA. A. Raghavendra Rao, President, A. Shama Rao Foundation, Mangalore, for encouraging me by providing all the facilities & support to prepare this book.

I wish to express my sincere thanks to Mr. A. Srinivas Rao, Vice-President, A. Shama Rao Foundation, Mangalore, and Mrs. Shashikala Rao, Secretary, A. Shama Rao Foundation, Mangalore, for their support.

I also thank all my colleagues at Srinivas Institute of Management Studies, Srinivas Institute of Technology, and Srinivas School of Engineering, Mangalore, for their kind help. My special thanks are due to my parents, my wife P. Shubhrajyotsna Aithal, my daughter Architha and my son Adarsh for their constant encouragement throughout the period of writing this book.

I am whole heartedly grateful to the Publisher of Acme Learning Private Limited, New Delhi. In conclusion, I thank all those who have helped me directly or indirectly to write and publish this book.

—Author

About the Author

Dr. P. Sreeramana Aithal has 20 years experience in Education, Research & Training. He is presently working as Director at Srinivas Integrated Campus, Surathkal, Mangalore. Having four Master degrees in Physics with Electronics, Information Technology, and E-Business, he got his first Ph.D. degree in Physics from Mangalore University in the area of nonlinear optical materials and second Ph.D. degree in Business Management from Manipal University, Manipal, in the area of mobile banking. He worked as Post Doctorial Research Fellow at "Lasers & Quantum Optics Division, Physical Research Laboratory, Ahmedabad for two years from 1999–2000. In the year 2002, he has been selected for the prestigious Oversee Fellowship of Dept. of Science & Technology, Govt. of India – Better Opportunity for Young Scientists in Chosen Area of Science & Technology (BOYSCAST) Fellowship and did one year Post Doctorial Research at Centre for Research & Education in Optics & Lasers (CREOL), at University of Central Florida, Orlando, U.S.A. During his Post Doctorial Research at Ahmedabad & USA, he has worked in the area of Nonlinear Optics, Photonics, Optical Limiters and Optical Solitons. Dr. Aithal has got SERC Young Scientist Project on Nonlinear Optics funded by Dept. of Science & Technology, India. Dr. Aithal also has a visiting associate-ship at Physical Research Laboratory, Ahmedabad, and Visiting Professor-ship of Grimsby Institute of Further & Higher Studies, Grimsby, U.K. He has 24 research publications in refereed International Journals in the area of Nonlinear Optics and Photonics, and 08 publications in mobile business. He has presented more than 60 research papers in National & International Conferences/Seminars. Presently he is guiding research scholars for their M.Phil. and Ph.D. degree in Electronics, Photonics, Information technology and business management. The personal website of Dr. P.S. Aithal is www.psaithal.blogspot.com where the readers/ students can download Power Point presentations and additional information related to this book.

UNIT 1

SEMICONDUCTOR DIODES AND APPLICATIONS

OBJECTIVES

In order to understand the functions of electronic circuits, first we should understand how the basic electronic components functions. As a part of it, in this Unit we will study semiconductor diode, the basic active component used in electronic circuits to control and rectify the current, and its applications. The Unit objectives are :

(1) To Study p-n junction diode, its characteristics, parameters, and approximations.

(2) To analyze DC load line and Temperature dependence of p-n diode characteristics, and AC equivalent circuits.

(3) To study Zener diode, its characteristics and parameters.

(4) To construct Half-wave rectifier, Full-wave rectifier, and other full-wave circuits using semiconductor diode, and study Ripple factor of these circuits.

(5) To analyze capacitor filter.

(6) To study Power supply performance and Zener diode voltage regulator.

1.1 INTRODUCTION

Electronics is the branch of Physics deals with the study of generation, motion, manipulation, control and detection of electrons in vacuum and semiconductors under applied electric or magnetic field. The branch is originated after invention of vacuum tube diode which is a two element electronic rectifying device by J. A. Fleming (U.K.) in the year 1904. In 1906, Lee De Forest added a third element, called the *control grid,* to the vacuum diode, resulting in the first amplifier, the *triode*. In the early 1930s the four-element tetrode and five-element pentode gained prominence in the electron-tube industry. The era of semiconductor electronics is started after invention of semiconductor diode in 1926, by L.O. Grondahl and P.H. Geiger (USA). They found rectifying properties in a (semiconducting) copper oxide-copper junction and by 1938 W. Schottky (Germany) developed a theoretical explanation for it. The p-n-diode finally was described by W. Schockley (USA) in 1949, even after J. Bardeen, W.H. Brattain and W. Schockley had invented the transistor in 1947.

1.1.1 P-N Junction Diode

P-type semiconductor can be fabricated by doping small amount of trivalent atoms to tetravalent materials like Silicon (Si) or Germanium (Ge). Similarly, N-type semiconductor can be fabricated by doping small amount of pentavalent atoms to Silicon or Germanium. Due to the process of doping, P-type semiconductor has more number of holes in valance band than number of electrons in conduction band and hence has holes as majority charge carriers. Similarly, N-type semiconductor has more number of electrons in conduction band than number of holes in valance band and hence has electrons as majority charge carriers. Thus a P-type semiconductor consists of positive charged holes as majority charge carriers, negative charged immobile impurity ions (acceptor ions) and neutral immobile Si atoms in its crystal structure. Similarly, an N-type semiconductor consists of negatively charged electrons as majority charge carriers, positively charged immobile impurity ions (donor ions) and neutral immobile Si atoms in its crystal structure. Additionally, due to the room temperature, P-type semiconductor has small amount of free electrons and N-type semiconductor has small amount of holes as minority charge carriers.

1.1.2 Construction of P-N Junction Diode

A P-N junction is formed by joining a piece of P-type semiconductor to a piece of N-type semiconductor such that the crystal structure remains continuous at the boundary as shown in Fig. 1.1. Such a device which has one P-N junction is called a **semiconductor diode**.

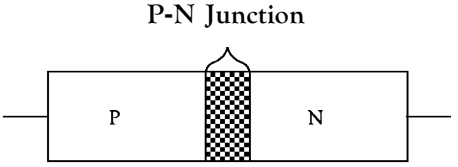


Figure 1.1 *P-N junction*

It should be noted that a PN junction can not be formed by simply joining or welding the two pieces together, because it would produce a discontinuous crystal structure. Special fabrication techniques are used to prepare P-N junctions.

While fabricating a P-N junction, the following processes takes place:

(i) The holes from P-region diffuse to N-region, where they combine with free electrons.

(ii) The free electrons from N-region diffuse to P-region, where they combine with the holes.

(iii) The diffusion of holes (from P-region to N-region) and free electrons from N-region to P-region takes place due to the reason that there is a difference of concentrations in the two regions. This difference in concentration creates a concentration gradient across the junction. It results in the diffusion of mobile charge carriers across the junction. Moreover, the electrons and holes move at random in all directions due to thermal energy. In doing so, some carriers manage to cross over the junction.

(iv) The diffusion of holes and free electrons across the junction takes place for a short time. After a few recombination of holes and free electrons in the vicinity of the junction, a retraining force is automatically set up. This force is produced due to depletion region, which

exists on either side of the junction. As a result of this, further diffusion of holes and free electrons from one region to the other is stopped by this depletion layer. The formation of this depletion region is due to availability of uncovered negative acceptor ions in P-region and positive donor ions in N-region in the junction, as shown in Fig. 1.2. The additional holes trying to diffuse to the N-region are repelled by the uncovered positive charge of the donor ions. Similarly, the electrons trying to diffuse into P-region, are repelled by the uncovered negative charge of the acceptor ions. Hence, the further diffusion of free electrons and holes across the junction is stopped.

Thus the region containing the uncovered acceptor and uncovered donor ions in the vicinity of the P-N junction is called depletion region. Since the depletion region contains immobile ions, which are electrically charged, the depletion region is also called space-charge region. Due to the presence of only immobile ions, the depletion region behaves as insulator. This space-charge region establishes a potential difference across the junction (designated as V_B), even when the junction is not connected across any external voltage source as shown in Fig. 1.3. This electric potential (V_B) is called **junction potenti**al or **barrier potential**. At room temperature, the junction potential or barrier voltage is 0.7 V for Si diode and 0.3 V for Ge diode.

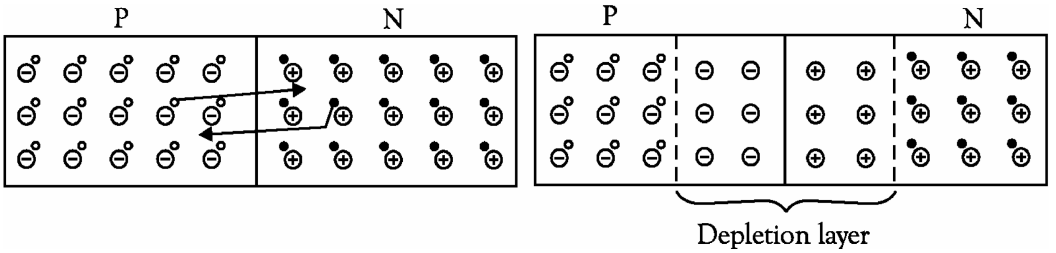


Figure 1.2 *Formation of depletion region in PN junction*

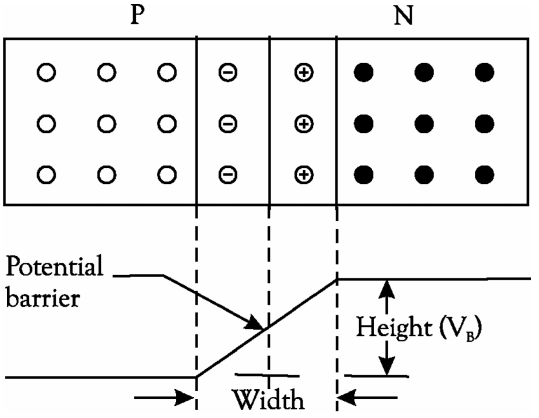


Figure 1.3 *Junction potential or barrier voltage of a P-N junction diode*

1.1.3 Biasing of P-N Junction Diode

A P-N junction connected to an external voltage source is called a biased P-N junction. Such a P-N junction finds variety of applications in electronics. By applying an external voltage, the width of the depletion region and hence the current flowing through the P-N junction can be controlled.

There are two ways of connecting the external voltage source across the P-N junction diode. They are :

(1) **Forward Bias:** In forward bias, the positive terminal of external voltage source (battery) is connected to P-type region and the negative terminal of the voltage source is connected to N-type region of Diode as shown in Fig. 1.4. This configuration reduces the width of depletion region (which results reduced V_B) and large amount of current flows through the junction. In practice, to forward bias a P-N junction and to conduct current, the external applied potential should be greater than barrier potential of the diode.

(2) **Reverse Bias:** In reverse bias, the positive terminal of external voltage source (battery) is connected to N-type region and the negative terminal of the voltage source is connected to P-type region of Diode as shown in Fig. 1.5. This configuration increases the width of depletion region (which results increased V_B) and no current flows through the junction. However, at room temperature, a small amount of current (in nano Amperes) flows through the reverse biased junction due to availability of minority charge carriers. This current is called **reverse saturation current** and is increases with increase in temperature.

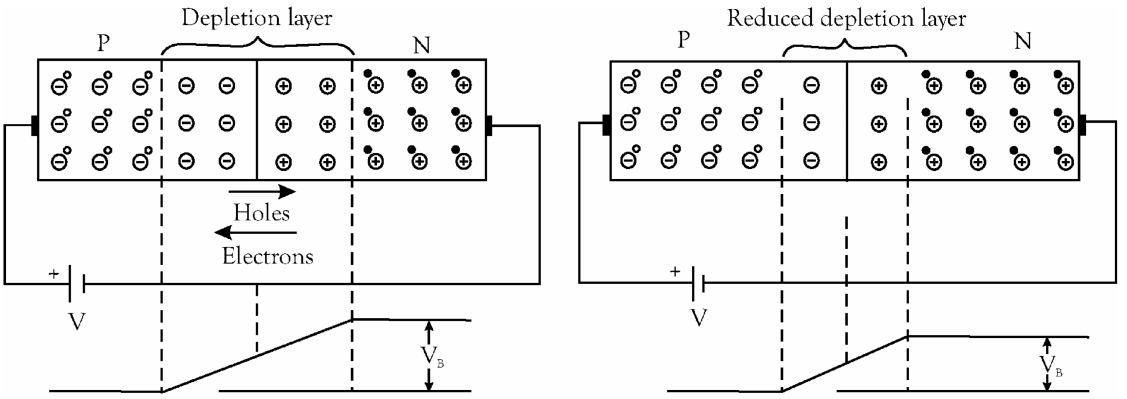


Figure 1.4 *P-N junction with forward bias*

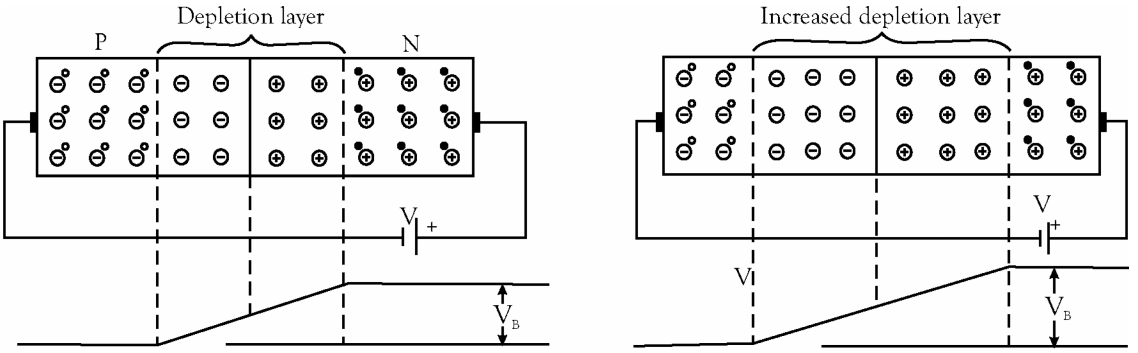


Figure 1.5 *P-N junction with reverse bias*

If we increase the reverse bias to a larger value by increasing the applied reverse voltage, the depletion region breakdown abruptly and large amount of reverse current starts flowing through the junction. The applied voltage at which such abrupt current flow occurs is known as **break-down voltage(V_{BR})**.

1.1.4 Characteristics and Parameters

Diode Characteristics

Figure 1.6 shows the static voltage-current characteristics for a low-power P-N junction diode.

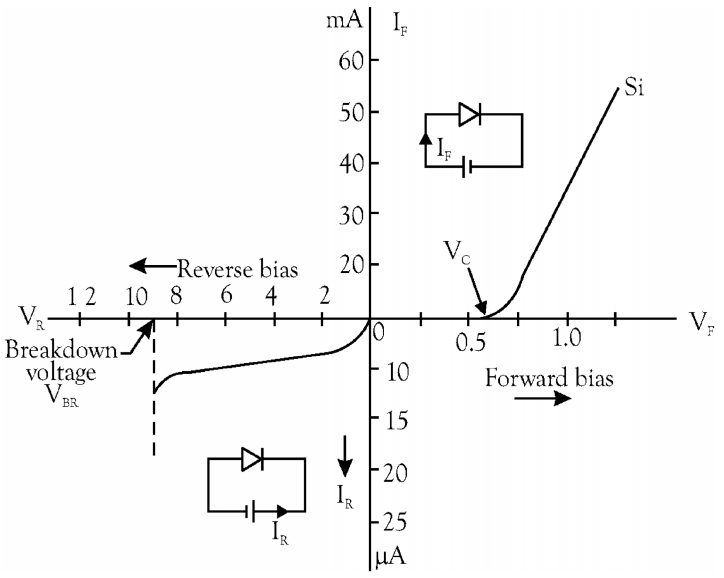


Figure 1.6 *Voltage-current (V-I) characteristics for a P-N junction diode*

(i) Forward Characteristic

When the diode is forward-biased and the applied voltage is increased from zero, hardly any current flows through the diode in the beginning. It is so because the external voltage is being opposed by the internal barrier voltage V_B whose value is 0.7 V for Si and 0.3 V for Ge. As soon as V_B is neutralized, current through the diode increases rapidly with increasing applied battery voltage. It is found that a small voltage of 1.0 V produces a forward current of about 50 mA. The diode will burn and fail to function if forward voltage is increased beyond a certain safe limit. The forward voltage at which the current I_B starts to flow is called **knee voltage** or **Cut-in voltage** (or **Cut-off voltage or off-set voltage**).

(ii) Reverse Characteristic

When the diode is reverse-biased, majority carriers are blocked and only a small current (due to minority charge carriers) flows through the diode. As the reverse voltage increases from zero, the reverse current very quickly reaches its maximum or saturation value I_O, which is also known as leakage current or reverse saturation current. It is of the order of nanoamperes (nA) for Si and microamperes (μA) for Ge. As seen from Fig. 1.6, when reverse voltage exceeds a certain value called breakdown voltage V_{BR}, the leakage current suddenly and sharply increases. The curve indicates zero resistance at this point.

Diode Parameters

(1) Bulk resistance (r_B):

It is the resistance offered by the diode in forward direction above the knee voltage. Obviously, it is the sum of the resistance values of the *P*-type and N-type semiconductor materials of which the diode is made of.

$$r_B = r_P + r_n$$

Usually, it is very small. It is given by

$$r_B = \frac{V - V_R}{I_F}$$

(2) Junction resistance (r_j):

Its value for forward-biased junction depends on the magnitude of *forward dc* current. Obviously, it is a *variable* resistance.

$r_j = 25\ \text{mV}/I_F\ \text{mA}$ for Germanium diode

$r_j = 50\ \text{mV}/I_F\ \text{mA}$ for Silicon diode

(3) Dynamic or a.c. resistance:

$$r_{ac} = r_d = r_B + r_j$$

For large values of forward current, I_F, r_j is negligible. Hence, $r_{ac} = r_B$.

For small values of I_F, r_B is negligible as compared to r_j.

Therefore, $r_{ac} = r_j$

(4) Forward voltage Drop:

It *is* given by the relation

$$\text{forward voltage drop} = \frac{\text{power dissipated}}{\text{forward dc current}}$$

(5) Reverse Saturation Current (I_O):

When the P-N junction is reverse biased, at room temperature, a small amount of current (in nano Amperes) flows through the reverse biased junction due to availability of minority charge carriers. This current is called **reverse saturation current** and is increases with increase in temperature.

(6) Reverse Breakdown voltage V_{BR}:

If we increase the reverse bias to a larger value by increasing the applied reverse voltage, then the depletion region breakdown abruptly and large amount of reverse current starts flowing through the junction. The applied voltage at which such abrupt current flow occurs is known as **break-down voltage (V_{BR})**.

(7) Reverse dc resistance (R_R):

$$R_R = \frac{\text{reverse voltage}}{\text{reverse current}}$$

(8) Equation of Diode current:

The analytical equation which describes both the forward and reverse characteristics is called the Boltzmann's diode equation given by:

$$I = I_O\left(\frac{qV}{e^{\eta kT}} - 1\right)$$

where,

I = The net current flowing through the diode

I_O = "Reverse saturation current", the diode leakage current density in the absence of light

V = Applied voltage across the terminals of the diode

q = Absolute value of electron charge

k = Boltzmann's constant; and

T = Absolute temperature (K)

η = ideality factor, a number between 1 and 2 which typically increases as the current decreases. At low current, η = 1 for germanium diode and η = 2 for silicon diode.

After simplification we can write,

$$I = I_0(e^{40V} - 1)$$
$$= I_0\left(e^{40V}\right) \qquad \text{if } V > 1 \text{ volt} \qquad \text{for germanium diode}$$

$$I = I_0(e^{20V} - 1)$$
$$= I_0\left(e^{20V}\right) \qquad \text{if } V > 1 \text{ volt} \qquad \text{for silicon diode}$$

1.1.5 Diode Approximations

(1) First Approximation: Ideal Diode Model

An ideal diode acts like a perfect conductor (zero offset voltage) during forward bias and perfect insulator(zero diode current) during reverse bias. Hence it acts like a short circuited switch during forward bias and open circuited switch during reverse bias as shown in Fig. 1.7.

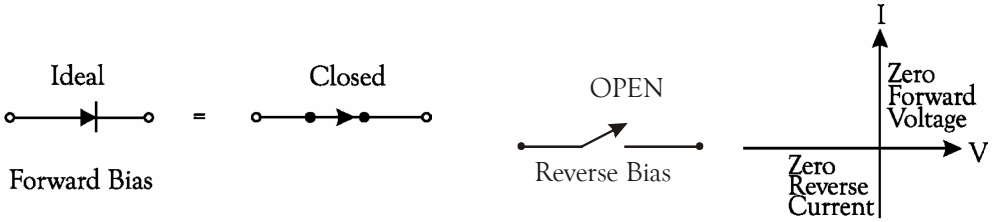


Figure 1.7 *(a) Ideal diode equivalent (b) its characteristics*

(2) Second Approximation: Based on Offset Voltage

In second approximation, the off-set voltage of the diode is taken into account. Usually this model is used when the source voltage is small. In this approximation, a practical diode (made of Si) is equated to an ideal diode in series with a battery of 0.7 V, as shown in Fig. 1.8. If the source voltage is greater than 0.7 V, the switch closes and the diode voltage is 0.7 V. If the source voltage is less than 0.7 V or if the source voltage is negative, the switch is open.

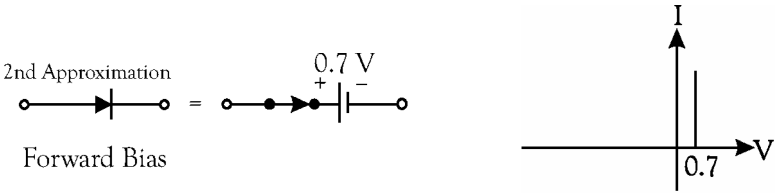


Figure 1.8 *(a) Switch and battery equivalent circuit (b) Second approximation model*

(3) Third Approximation: Piece wise linear Model

The equivalent circuit for the third approximation is a switch in series with a battery of 0.7 V and a resistance of R_B *as shown in Fig. 1.9 (a).* After the external circuit has overcome the barrier potential, the diode current produces an *IR* drop across the bulk resistance. Therefore, the total voltage across the silicon diode becomes, $V_F = 0.7 + I_F \cdot R_B$

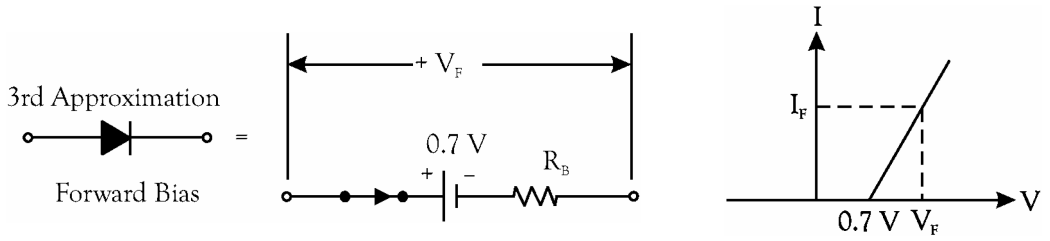


Figure 1.9 *(a) Piece wise linear equivalent circuit (b) Piece wise model of diode*

1.1.6 DC Load Line

The load line is a tool used to find the exact value of diode current and voltage. To draw the DC load line for a diode, connect it as shown in Fig. 1.10. Here, V_S is the source voltage, and R_S is the current limiting resistor. The diode is forward biased and the voltage drop across it due to barrier potential is V_B volts.

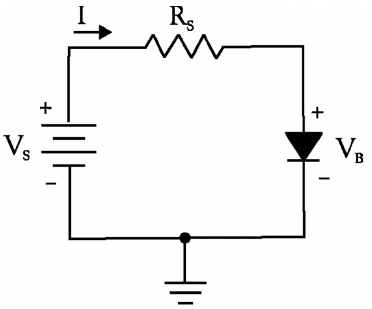


Figure 1.10 *Circuit for drawing DC load line*

The current flowing through the circuit is $I = (V_S - V_B)/ R_S$ ...(1.1)

For example, if V_S = 2 V, and R_S = 100 Ω, then $I = (2 - V_B)/100 = (2 - 0)/100$ = 20 mA

Plotting this graph (V = 0 volt, I = 20 mA) gives the point on the vertical axis of Fig. 1.11. This point is called **saturation point** because it represents maximum current.

Let V_B = 2 V, then Eqn (1.1) becomes $I = (2 V - 2V) / 100 Ω = 0$.

Plotting this plot (V_B = 2 V, I = 0), gives the point on the horizontal axis of Fig. 1.11. This point is called **cut-off point** because it represents minimum current.

By selecting other voltages, we can calculate and plot additional points. Because the Eqn. (1.1) represents a linear equation, all points will lie on the straight line as shown in Fig. 1.11. This straight line is called the **DC load line**.

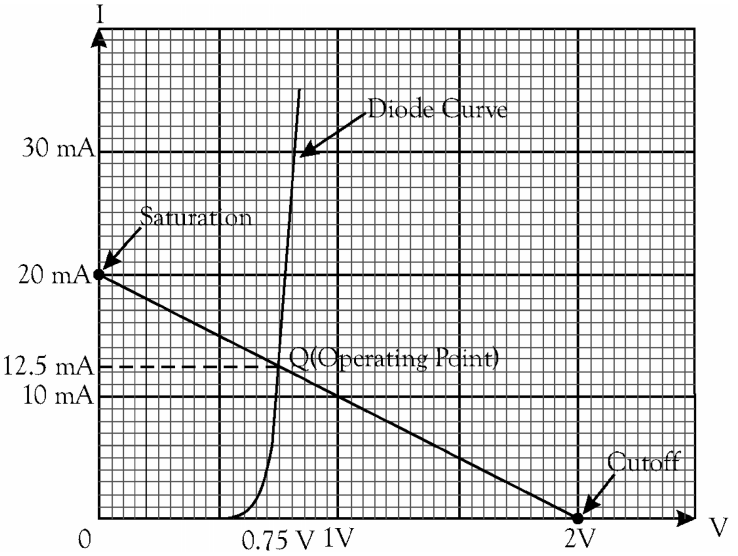


Figure 1.11 *DC load line and operating point of P-N junction diode*

When we superimpose the diode characteristic curve on DC load line, the point of intersection is called **Quiescent Point** (Q-point) or **operating point** because it represents the voltage across the diode at a given current flow through the diode.

In the Fig. 1.11, the current is maximum for V = 0, the Eqn. (1.1) gives $I = V_S/R_S$ => Saturation point of DC load line. Similarly, when I = 0, $V = V_S$, => Cut-off point of DC load line.

1.1.7 Temperature Dependence of p-n Junction Characteristics

The barrier voltage of a P–N junction depends upon three factors namely density, electronic charge and temperature. For a given PN junction, the first two factors are constant, thus making the value of barrier voltage V_B dependent only on temperature. It has been observed that for both germanium and silicon, the value of V_B decrease by 2 mV/°C. Mathematically, the decrease in barrier voltage, $\Delta V_B = - 0.002 \times \Delta t$, where Δt is the increase in temperature in °C.

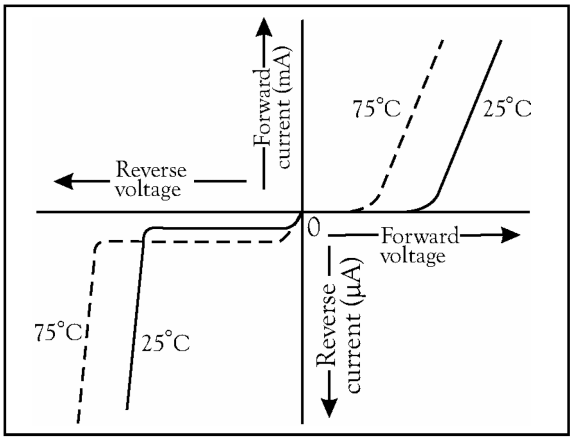


Figure 1.12 *Effect of temperature on the diode characteristic*

As shown in Fig. 1.12, in the reverse bias region, the breakdown voltage (V_{BR}) is increasing with the increase in temperature and the reverse saturation current (I_O) is increasing to almost double in magnitude for every 10°C increase in temperature.

1.1.8 AC Equivalent Circuits

When we apply ac signal to a P-N junction, it becomes periodically forward and reverse biased. When a forward biased junction is suddenly reverse biased, a reverse current flows which is large initially but gradually decreases to the level of saturation current (I_O). This effect can be equated as it is a discharging capacitor and represented by a capacitance called diffusion capacitance (C_D). Similarly, a reverse biased P–N junction behaves like a junction capacitor (parallel plate capacitor) with depletion region acts like dielectric medium between P-type and N-type plates. This junction capacitance is called **transition capacitance (C_T).**

For ac signal, a forward biased junction offers ac resistance r_{ac} along with barrier voltage (V_B) and a parallel diffusion capacitance (C_D). Similarly, a reverse biased junction offers a reverse resistance R_R connected in parallel with the transition capacitance (C_T). Thus an ac equivalent circuit of P-N junction diode during forward bias is shown in Fig. 1.13 (a) and during reverse bias is shown in Fig. 1.13 (b).

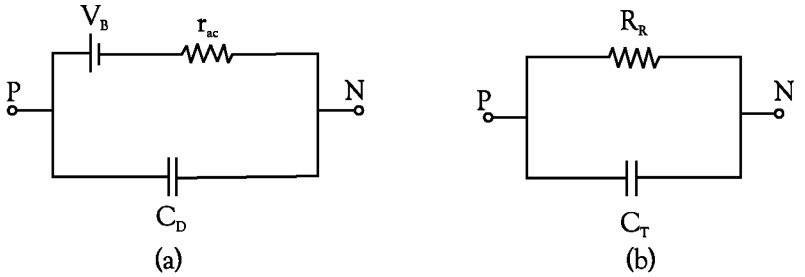


Figure 1.13 *(a) AC equivalent circuit for forward bias. (b) AC equivalent circuit for reverse bias.*

1.2 ZENER DIODE

1.2.1 Principle

A Zener diode is a special purpose diode prepared by sandwiching heavily doped P-type and N-type semiconductors. Zener diode is specially designed to operate in breakdown region called **Zener breakdown**, where current is limited only by external resistance and the power dissipation of the diode. i.e., once the applied voltage under reverse bias is equal to breakdown voltage, the current increases very rapidly and the diode voltage stays essentially constant. This property of Zener diode can be used for voltage regulation. The satisfactory explanation for the breakdown of the junction is given by an American Scientist C.E. Zener in 1934, and hence the device is named after him. In Zener diode, at low reverse voltage below 6 V, **Zener breakdown** becomes predominant and higher reverse voltage above 6 V, **avalanche breakdown** becomes predominant.

Avalanche Breakdown: Due to applied reverse bias, the minority charge carriers cross the depletion region and gain enough kinetic energy to knock bound electrons out of the covalent bonds. These electrons will in-turn collide with other atoms and will increase the number of electrons and holes available for conduction. This multiplication effect of free carriers is called avalanche breakdown.

Zener Breakdown: Due to heavy doping, the Zener diode will have extremely narrow depletion region of the order of only 150 – 200 Å, hence, there exists a high electric field, in the order of 10^6 V/cm across the junction. This field provides a high electrical force which is responsible for tearing electrons out of the covalent bonds directly, rather than by collision. This is Zener breakdown.

1.2.2 Construction

A Zener diode is a silicon P-N junction heavily doped diode always operated in reverse bias and it has sharp breakdown voltage called Zener voltage (V_Z). The corresponding reverse current flowing through the Zener is called Zener current (I_Z). Such a characteristic is obtained by addition of suitable quantities of an impurity material to silicon.

The symbol of Zener diode is shown in Fig. 1.14 (a), and the equivalent circuit is shown in Fig. 1.14 (b) & (c). When the Zener diode is operated in the breakdown region, it can be considered as a constant voltage source.

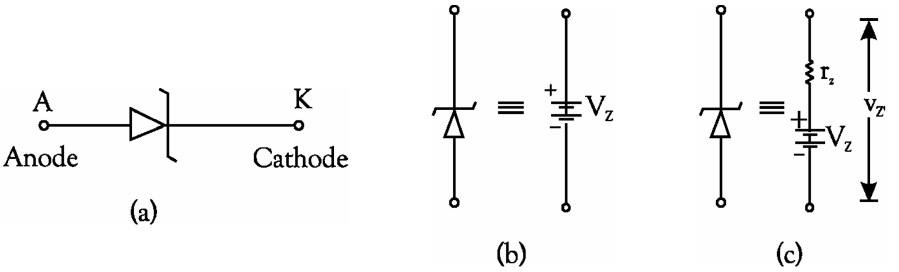


Figure 1.14 *Zener diode (a) Symbol, (b) Ideal Equivalent circuit, (c) Practical equivalent circuit*

1.2.3 V-I Characteristics

The V-I characteristics of a Zener diode is shown in Fig. 1.15.

(i) During forward bias, the Zener diode acts like ordinary P-N junction diode and its characteristic is shown in first quadrant of the graph.

(ii) During reverse bias, at a particular reverse voltage called Zener voltage (V_Z), Zener breakdown occurs and it acts like constant voltage source. Thus a Zener diode of a known breakdown voltage can be used as reference voltage in voltage regulators.

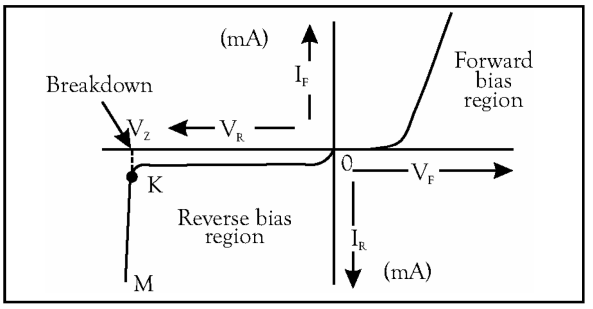


Figure 1.15 *V-I characteristics of Zener diode*

Zener Diode Specifications

(1) Zener Voltages

The manufacturers specify the value of breakdown voltage known as the Zener voltage, V_Z at some value of test current, I_{ZT}. This is on the linear portion of the reverse characteristic and corresponds to approximately one-quarter of the maximum power dissipation capability of the diode. Zener diodes are available at various V_Z values from 2.4 to 200 V with accuracies between 5% and 20%, depending upon the cost.

(2) Power Dissipation

Power dissipation in the Zener diode is the product of V_Z and reverse current, I_Z, with maximum power ratings ranging from 150 mW to 50 W.

(3) Breakover current

Since there is some curvature of the reverse characteristic at low values of I_Z, there may be some specified value of current, I_{ZK} in the neighborhood of the breakover knee, where the voltage across the diode starts to differ greatly from V_Z.

(4) Dynamic Impedance

The Zener dynamic impedance, Z_Z, is defined as:

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} \qquad ...(1.2)$$

This impedance is usually evaluated in the region of the specified test current I_{ZT}, and is the reciprocal of the slope of the reverse characteristic. Ideally, Z_Z is zero for a perfectly vertical breakdown curve, but in practice may vary from several ohms to several hundred ohms, depending upon the particular Zener diode voltage and the operating current. This specification provided by the manufacturer, will helps to describe how "vertical" is the reverse characteristic of Zener diode.

(5) Zener diodes used in Practical Circuits

1N4728 – 1N4732 series Zener diodes are commonly used in electronic circuits with following specifications:

Series No.	Nominal Zener voltage (V_Z in Volts) at nominal I_{ZT}	Test Current I_{ZT} (mA)
1N4728	3.3	76
1N4729	3.6	69
1N4730	3.9	64
1N4731	4.3	58
1N4732	4.7	53

1.2.4 Applications

The important applications of Zener diode are:

(1) As a voltage regulator in regulated power supplies.
(2) As a fixed reference voltage in transistor biasing circuits.
(3) As peak clippers and limiters in wave shaping circuits.
(4) As a meter protector against damage from accidental applications.

1.2.5 Comparison of Zener Diode with P-N Junction Diode

S. No.	Zener Diode	P-N Junction Diode
1	A Zener diode is a silicon P-N junction heavily doped diode always operated in reverse bias breakdown condition.	Comparatively lightly doped and operated in forward bias condition.
2	Dynamic Zener resistance is very small in reverse breakdown region	The resistance in reverse bias is very high.
3	In operating region current flows from N-region to P-region within the diode.	In operating region current flows from P–region to N–region within the diode
4	Power dissipation capacity of Zener diode is high.	Power dissipation capability of P-N diode is very low compared to Zener diode.
5	Zener diode is mainly used in voltage regulators	P-N junction diode is mainly used in rectifiers and other wave shaping circuits.

1.3 HALF-WAVE DIODE RECTIFIER

1.3.1 Principle

A half-wave rectifier is a circuit, which uses one P-N junction diode to convert a.c. voltage into pulsating d.c. voltage. Half-wave rectifier functions using the principle of unidirectional conduction of semiconductor junction diode.

1.3.2 Circuit

The circuit of half-wave rectifier consists of a single diode in series with a load resistor as shown in Fig. 1.16 (b). The input to the half-wave rectifier is supplied from the 50 Hz a.c. supply, whose waveform is shown in Fig. 1.16 (a).

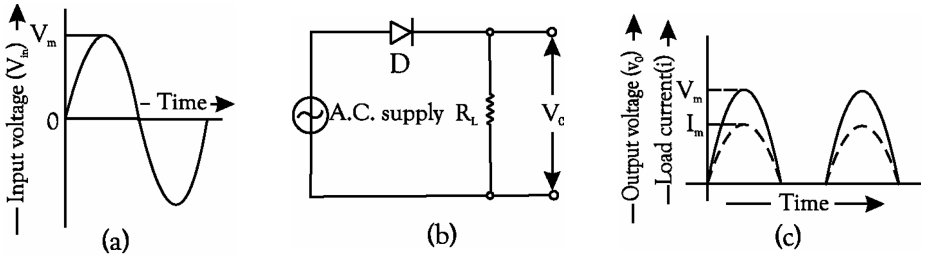


Figure 1.16 *(a) Input waveform, (b) Half-wave rectifier circuit, (c) Output waveform*

1.3.3 Working

The working of a half-wave rectifier circuit may be studied by considering the positive and negative half cycles of the a.c. input voltage separately.

(i) During the positive half cycle of the a.c. input voltage, the diode is forward biased and conducts for all instantaneous voltages greater than the offset voltage (0.7 V for silicon and 0.3 V for germanium diodes). However, for all practical purposes, we assume that the diode is forward biased, whenever the a.c. input voltage goes above zero. While conducting, the diode acts as a short-circuit, so that the circuit current flows and produces a voltage across the load resistor (R_L). The voltage produced across the load resistor has the same shape as that of the positive input half cycle of a.c. input voltage as shown in Fig. 1.16 (c). The waveform of diode current (which is equal to the load current) is also shown in Fig. 1..16 (c).

(ii) During the negative half-cycle of the a.c. input voltage, the diode is reverse biased and hence it does not conduct. Thus there is no current flow or voltage drop across load resistor R_L i.e., $i_D = 0$ and $V_O = 0$. The net result is that only the positive half cycle of the a.c. input voltage appears across R_L. It means that only the positive half cycle of the a.c. input voltage is utilized for delivering a.c. power. It is evident that the output voltage (V_O) is not a steady d.c. but it is a pulsating d.c. wave having a ripple frequency equal to the input voltage frequency. It will be interesting to know that we can see the waveform of output voltage on an oscilloscope connected

across R_L. If we measure the output voltage (or output current) by a d.c. meter, it will indicate some average positive value for both voltage and current.

1.3.4 Output Waveform

Fig. 1.17 shows the output waveform of the half-wave rectifier. The circuit generates only one-half cycle of the a.c. input voltage at output, therefore it is popularly known as a half-wave rectifier.

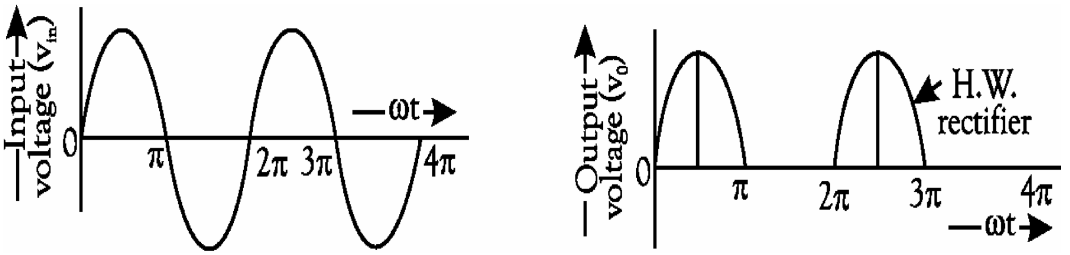


Figure 1.17 *Input and output waveforms of half-wave rectifier*

1.3.5 Device Parameters

(i) Average Values of Output Voltage and Load Current:

The instantaneous value of the sinusoidal a.c. input voltage is given by the relation,

$$v = V_m \sin \omega t = V_m \sin \theta$$

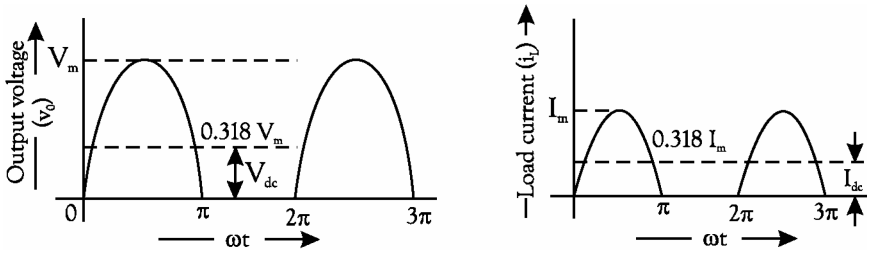


Figure 1.18 *Average values of output voltage and load current in a half-wave rectifier*

Now let I_m = Maximum value of diode current or load current. It is the current through the resistor R_L.

V_{dc} = Average or d.c. value of output (or load) voltage across the load resistor, and

I_{dc} = Average or d.c. value of load current.

Fig. 1.18 (a) shows the waveform of an output voltage of a half-wave rectifier. 1t indicates that there

is an output voltage (varying sinusoidally) for a period from 0 to π and nothing for a period from π to 2π. The average or d.c. value of the output voltage is given by the relation,

$$V_{dc} = \frac{\text{Area under the curve over the full cycle}}{\text{Base}}$$

$$= \frac{\int_0^{\pi} v.\, d\theta}{2\pi} = \frac{1}{2\pi}\int_0^{\pi} V_m . \sin\theta .\, d\theta$$

$$= \frac{V_m}{2\pi}\left|\left(-\cos\theta\right)_0^{\pi}\right| = \frac{V_m}{2\pi}\left(+1-\left(-1\right)\right)$$

$$= \frac{V_m}{\pi} = 0.318\, V_m \qquad \text{...(1.3)}$$

The above expression indicates that the average or d.c. value of the output voltage is 31.8 per cent of the maximum a.c. input voltage.

Let us now find the average or d.c. value of load current. It may be found by dividing the d.c. value of output voltage (V_{dc}) by the value of load resistor (R_d). Mathematically, the average or d.c. value of load current is given by,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi . R_L} = \frac{I_m}{\pi}$$

$$= 0.318\ I_m \qquad \text{...(1.4)}$$

The above expression indicates that the average or d.c. value of load current is 31.8% of the maximum load current.

(ii) Form Factor (F)

It is the ratio of rms value of maximum load current to average value of maximum load current.

F = (rms value of I_m)/(average value of I_m) = 0.5 I_m / 0.318 I_m = 1.57

(iii) Peak Inverse Voltage

It is the maximum voltage across the diode in the reverse direction. Its value in present case is V_m.

(iv) Efficiency

It is the ratio of output power to total input power supplied to the circuit.

$$\eta = P_{out}/P_{in}$$

Here, $P_{out} = I_{dc}^2.R_L$; $P_{in} = I_{rms}^2 (R_d + R_L)$ where R_d is forward resistance of the diode.

Then $\eta\ \% = [(I_{dc}^2.R_L) / I_{rms}^2 (R_d + R_L)]\ \times 100$ ...(1.5)

By neglecting r_d, η = 40.6 %

Hence, the maximum possible efficiency of half-wave rectifier is 40.6 %.

(v) Ripple factor (γ)

It is the ratio of voltage (or ripple current) in output to d.c. voltage component in output (or current) and denoted by γ

Thus $\gamma = V_r(rms) / V_{dc} = I_{r(rms)} / I_{dc}$

By simplifying the value of $I_{r(rms)}$ in terms of I_{rms} we can write

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

or

$$\gamma = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = 1.21 \qquad ...(1.6)$$

Thus the ripple factor of half-wave rectifier is 1.21

1.4 FULL-WAVE DIODE RECTIFIER

1.4.1 Principle

A full-wave rectifier is a circuit, which allows a unidirectional current to flow through the load during the entire input cycle as shown in Fig. 1.19. The result of full-wave rectification is a d.c. output voltage that pulsates every half-cycle of the input.

1.4.2 Circuit

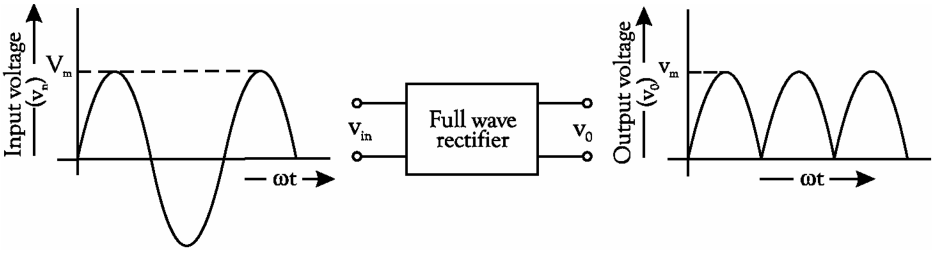


Figure 1.19 *Full wave rectifier, with input and output voltage waveforms*

The circuit diagram of a full wave rectifier is shown in Fig. 1.20. The input ac signal V_{in} is taken by a transformer of primary voltage V_1 and secondary voltage V_2. The center-tap on the secondary winding of a transformer is, usually, taken as the ground or zero voltage reference point. The voltage between the center-tap and either end of the secondary winding is half of the secondary voltage, *i.e.*, $V_S = V_2/2$,

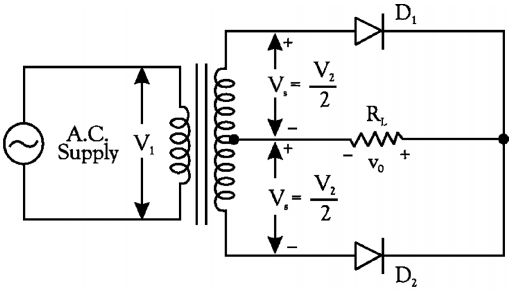


Figure 1.20 *Center-tapped full-wave rectifier*

1.4.3 Working

The working of a center-tapped full-wave rectifier circuit may be discussed as follows:

(i) During the positive input half-cycle, the polarities of the secondary voltage are as shown in Fig. 1.21 (a). This forward biases the diode D_1 and reverse-biases the diode D_2. As a result of this, the diode D_1 conducts some current whereas the diode D_2 is OFF. The current through load R_L is as indicated in the figure.

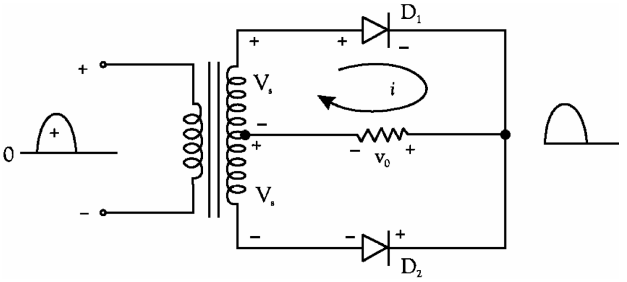


Figure 1.21 *(a) Function of full-wave rectifier during positive half-cycle*

(ii) During the negative input half-cycle, the polarities of the secondary voltage are as shown in Fig. 1.21 (b). This reverse-biases the diode D_1 and forward-biases the diode, D_2. As a result of this, the diode D_1 is OFF and the diode D_2 conducts some current. The current through the load R_L is as indicated in the figure.

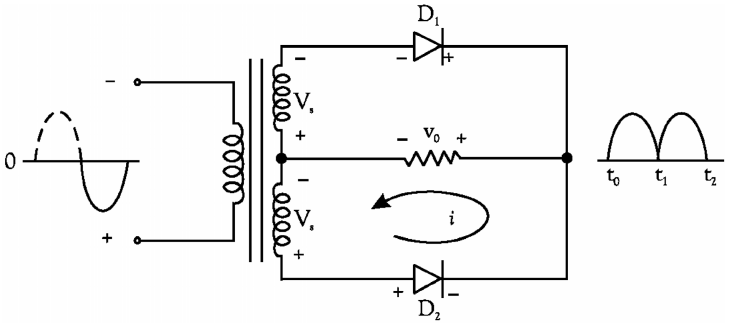


Figure 1.21 *(b) Function of full-wave rectifier during negative half-cycle*

Thus, it may be noted that current through the load flows in the same direction, during both the positive and negative half-cycle of input signal. Therefore, the output voltage developed across load R_L is full-wave rectified d.c. voltage as shown in Fig. 1.22.

1.4.4 Output Waveform

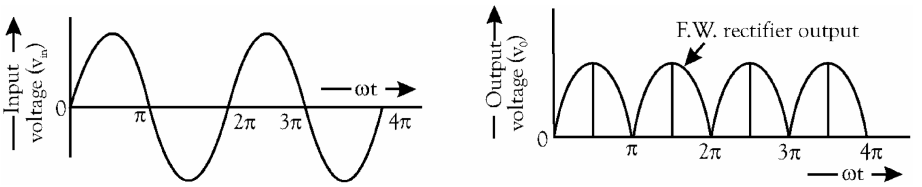


Figure 1.22 *Input and output waveforms of full-wave rectifier*

1.4.5 Device Parameters

(i) Average Values of Output Voltage and Load Current:

We know that the equation for the voltage across each half of the secondary winding,

$V_S = V_m \sin \omega t = V_m \sin \theta$

where V_S = Instantaneous value of the voltage across each half of the secondary winding.

We also know that the average or d.c. value of the output voltage,

V_{dc} = (Area under the curve over a half-cycle) / base

$$= \frac{\int_0^{\pi} v_s \, . \, d\theta}{\pi} = \frac{\int_0^{\pi} V_m \sin \theta \, d\theta}{\pi} = \frac{1}{\pi} \int_0^{\pi} V_m \, . \sin \theta \, d\theta$$

$$V_{dc} = \frac{V_m}{\pi} \left| (-\cos \theta) \right|_0^{\pi} = \frac{V_m}{\pi} \left[+1 - (-1) \right] = \frac{2 V_m}{\pi} = 0.636 \, V_m \qquad \ldots(1.7)$$

From the above relation it is noted that the average value of a full-wave rectifier is 0.636 V_m and is as shown in Fig. 1.23 (a), and this value is twice that of a half-wave rectifier.

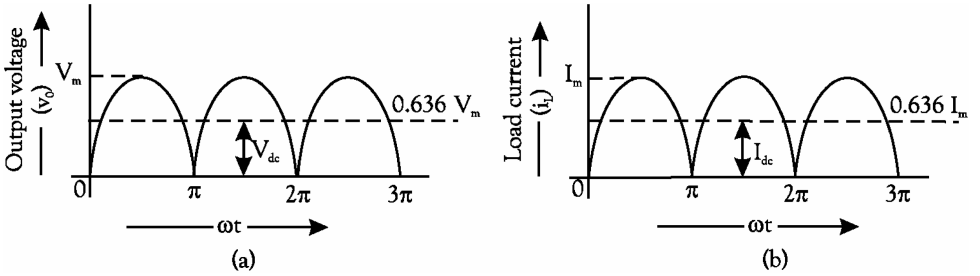


Figure 1.23 *Average values of output voltage and load current in a full-wave rectifier*

The average or d.c. value of load current is given by,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2\,V_m}{\pi\,.\,R_L} = \frac{2\,I_m}{\pi} = 0.636\,I_m \qquad ...(1.8)$$

From the above relation it is evident that average value of load current is 0.636 I_m and is as shown in Fig. 1.23 (b), and this value is twice that of a half-wave rectifier.

(ii) Peak Inverse Voltage of a Diode

The anode voltage of the diode D_1 is + V_m (where V_m is the maximum half secondary voltage) and the anode voltage of D_2 is $-V_m$. Since D_1 is forward biased, its cathode is at the same voltage as its anode (neglecting barrier potential) i.e., + V_m. This is also the voltage on the cathode of the diode D_2. The total reverse voltage across the diode D_2 is : = V_m–(– V_m) = 2 V_m. Therefore, Peak–inverse voltage of each diode in a center-tapped full-wave rectifier,

$$PIV = 2\,V_m$$

(iii) Efficiency

We know that the efficiency of rectifier $\eta = P_{out}/P_{in}$

Here $P_{out} = I_{dc}^2.R_L$; $P_{in} = I_{rms}^2\,(R_d + R_L)$

$$\eta = \frac{I_{dc}^2 \times R_L}{I_{rms}^2\left(R_d + R_L\right)}$$

where R_d is the forward resistance of diode.

$$\eta = \frac{\left(\frac{2\,I_m}{\pi}\right)^2 \times R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 \times \left(R_d + R_L\right)} = \frac{8}{\pi^2} \times \frac{R_L}{R_d + R_L} = \frac{0.812}{1 + \frac{R_d}{R_L}} \qquad ... (1.9)$$

Efficiency will be maximum if $R_L >> R_d$. Thus η_{max} = 0.812 or 81.2%

From the above, it is evident that maximum efficiency of a full-wave rectifier is twice that of half-wave rectifier.

(iv) Ripple factor

The average value of load current in a full-wave rectifier is given by the relation, $I_{dc} = 2I_{rms}/\pi$

The r.m.s. value of the load current is given by : $I_{rms} = I_m/\sqrt{2}$

Then the expression for ripple factor γ is

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = 0.482 \qquad ...(1.10)$$

From the above result it is evident that ripple factor of a full-wave rectifier is 0.482 and is much smaller than that of a half-wave rectifier. Because of this reason, full-wave rectifier is used more commonly in actual practice.

1.4.6 Advantages and Disadvantages of Center-tapped Full-wave Rectifier

Advantages

1. The d.c. output voltage and load current values are twice than those of a half-wave rectifier.
2. The ripple factor is much less (0.482) than that of half-wave rectifier (1.21).
3. The efficiency is twice that of half-wave rectifier. For a full-wave rectifier, the maximum possible value of efficiency is 81.2%, while that of half-wave rectifier is 40.6%.

Disadvantages

1. The output voltage is half of the secondary voltage.
2. The peak-inverse voltage (PIV) of a diode is twice that of the diode used in the half-wave rectifier.
3. It is expensive to manufacture a center-tapped transformer, which produces equal voltages on each half of the secondary winding.

1.5 OTHER FULL-WAVE CIRCUITS

1.5.1 Bridge Rectifier

It is most frequently used rectifier circuit for electronic dc power supplies. It uses four diodes connected across the main supply.

(1) Circuit Diagram

The circuit diagram of bridge rectifier is shown in Fig. 1.24.

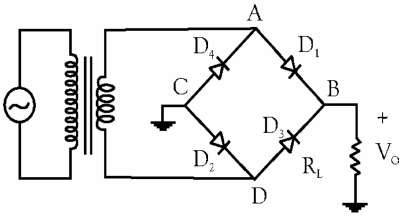


Figure 1.24 *Circuit diagram of bridge rectifier*

(2) Working

(i) During positive half-cycle of input voltage, as shown in Fig. 1.25 (a), the diodes D_1 and D_2 are forward biased and conduct some current in the direction as indicated in the figure. A voltage is developed across the resistor R_L due to the current flow through it. The voltage waveform looks like the positive half of the input cycle. At this time the diodes D_3 and D_4 are reverse biased.

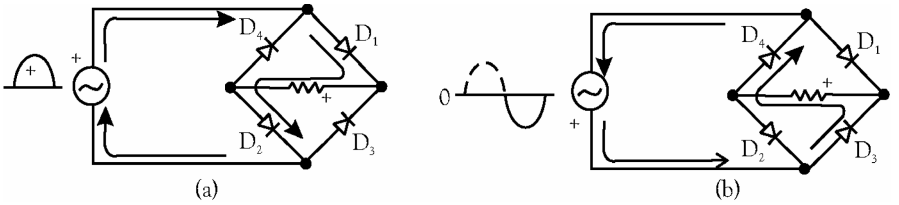


Figure 1.25 *Working of bridge rectifier (a) during positive cycle (b) during negative cycle*

(ii) When the input voltage is negative as shown in Fig. 1.25 (b), the diodes D_3 and D_4 are forward biased and conduct some current in the same direction through R_L as during the positive half-cycle. During this time, the diodes D_1 and D_2 are reverse biased. As a result of this action, a full-wave rectified output voltage is developed across the resistance R_L.

(3) Device parameters

(i) Average Values of Output Voltage and Load Current:

The average values of output voltage and load current for bridge rectifier are:

$$V_{dc} = \frac{2V_m}{\pi} \text{ and } I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi . R_L} \qquad ...(1.11)$$

where V_m = Maximum value of secondary voltage.

(ii) Peak Inverse Voltage of a Diode:

At a given half-cycle, two diodes are reverse biased and have a maximum reverse voltage equal to the maximum secondary voltage (V_m). Thus, peak-inverse voltage of a diode in a bridge rectifier, is PIV= V_m

(4) Advantages and Disadvantages of Bridge Rectifier

Advantages

1. It can be used in applications allowing floating output terminals *i.e.,* no output terminal is grounded.
2. The transformer is less costly as it is required to provide only half the voltage of an equivalent center-tapped transformer used in a full wave rectifier circuit.
3. No center-tap is required on the transformer.

Disadvantages

It has only one disadvantage that it uses four diodes as compared to two diodes for center-tapped full-wave rectifier. But ready availability of low cost silicon diodes have made it more economical despite its requirement of four diodes. Besides this, PIV rating required of the diodes, in a bridge rectifier, is only half of that for a center-tapped full-wave rectifier. This is a great advantage, which offsets the disadvantage of using four diode instead of two in a full-wave rectifier circuit.

1.5.2 Comparison of Rectifiers

S. No.	Item	Half-wave	Full-wave	
			Center-tapped	Bridge
1.	Number of diodes	1	2	4
2.	Peak-inverse voltage of diode	V_m	$2\,V_m$	V_m
3.	D.C. Output voltage	$0.318\,V_m$	$0.636\,V_m$	$0.636\,V_m$
4.	Ripple factor	1.21	0.482	0.482
5	Efficiency (%)	40.6%	81.2%	81.2%

1.6 FILTERS

Filter is an electronic circuit used to minimize the ripple content in rectified output of a rectifier. The output of various rectifier circuits is pulsating. It has a dc value and some ac variations called ripples. This type of output is not useful for driving sophisticated electronic circuits / devices. The sophisticated circuits require a very steady dc output that approaches the smoothness of the output of the battery. A circuit that converts a pulsating output from a rectifier into a steady dc level is known as filter because it filters out the pulsations in the signal (Fig. 1.26).

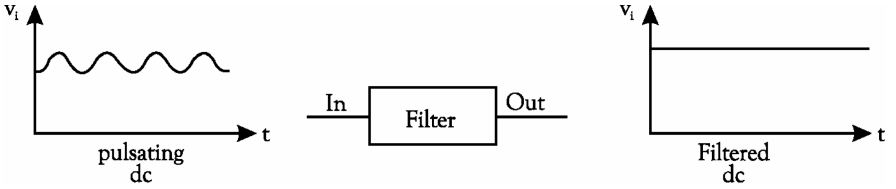


Figure 1.26 *Idea of basic filter.*

There are different types of filters popularly used in practice. They are :

1. Series inductor filter
2. Shunt capacitor filter
3. LC filter (or L-type filter)
4. π-filter

1.6.1 Shunt Capacitor Filter

In this circuit, a suitable single capacitor C is connected across the rectifier and in parallel with the load

R_L to achieve filtering action. This type of filter is known as *capacitor input filter.* This filter circuit depends for its operation on the property of a capacitor to charge up (*i.e.,* store energy) when conducting and to discharge (*i.e.,* deliver energy) during the non-conduction cycle. In simple words, a capacitor opposes any *change in voltage.* When connected across a pulsating dc voltage, it tends to smoothen out or filter out the voltage pulsations (or ripples).

The filtering action of the simple capacitor filter when used in a half-wave rectifier is shown in Fig. 1.27.

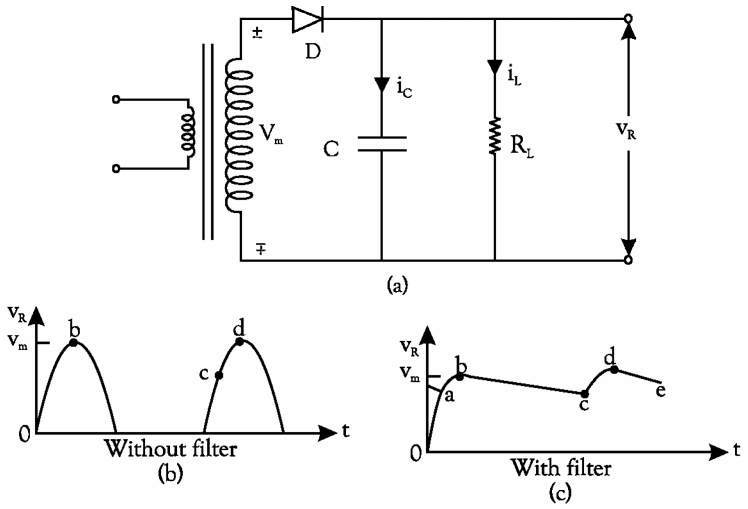


Figure 1.27 *Simple capacitor filter (a) Circuit, (b) Output without filter (c) Output with filter*

1.6.2 Approximate Analysis of Capacitor Filter

When positive half-cycle of the ac input is applied, the diode is forward-biased and hence is turned ON. This allows C to quickly charge up to V_m [point b in Fig. 1.27 (c)] because charging time constant is almost zero. It is so because there is no resistance in the charging path except diode forward resistance which is negligible. Hence, capacitor follows the charging voltage as shown. After being fully charged, the capacitor holds the charge even if the input ac supply to the rectifier goes negative.

During the negative half-cycle, the capacitor attempts to discharge. However, it cannot discharge through D which, being now reverse-biased is OFF. Hence, it discharges through R_L from point b to c in Fig. 1.27 (c) and its voltage decreases small amount. The discharging time constant (= CR_L) is usually 100 times more than the charging time. Hence, C does not have sufficient time to discharge appreciably. It is seen that even during negative half-cycle of the input supply, the capacitor maintains large voltage across R_L.

During the next positive half-cycle, when rectifier voltage exceeds the capacitor voltage represented by point c in Fig. 1.27 (c), C is again charged quickly to V_m as represented by point d. Once more, input voltage goes negative, opening the diode, and forcing C to discharge through R_L during the interval d to e. In this way, R_L sees nearly constant dc voltage across it at all times.

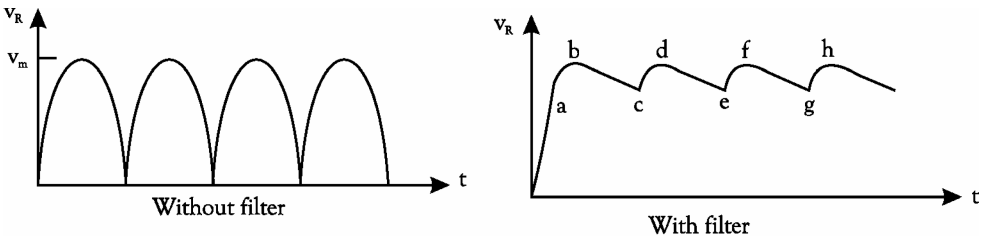


Figure 1. 28 *Output of a capacitor filter in full-wave rectifier*

The filtering action of this simple capacitor filter on a full-wave rectifier is shown in Fig. 1.28. It is seen that as compared to a HW rectifier

(i) dc load voltage increases slightly towards V_m

(ii) ripple voltage has been reduced by half.

This decreased ripple is because of shorter discharge time before the capacitor is re-energised by another pulse of current.

1.6.3 Device Parameters

(1) Load Current

The load current has the same waveshape as V_R because load is purely resistive. It can be understand that during periods a, b and c, d etc. current is supplied by the diode and during period b, c and d, e etc., by the capacitor.

(2) PIV

When diode is reverse-biased, the voltage across, it is the sum of

(i) capacitor voltage which is almost equal to V_m.

(ii) secondary voltage V_m.

Hence, PIV is $2V_m$.

(3) Ripple Factor

Its value is given by the formula

$$\gamma = \frac{1}{4\sqrt{3} f\, CR_L}$$

Also, $$\gamma = \frac{2890}{CR_L} \qquad \text{... (1.12)}$$

where f = 50 Hz, C is in μF and R_L in ohms.

Effect of Increasing Filter Capacitance

A capacitor has the basic property of opposing changes in voltage. Hence, a bigger capacitor would tend to reduce the ripple magnitude. It has been found that increasing the capacitor size has following effect.

1. increases V_{dc} towards the limiting value V_m.
2. reduces the magnitude of ripple voltage.
3. reduces the time of flow of current pulse through the diode.
4. increases the peak current in the diode.

Advantages of Capacitor Filter

1. The circuit has less number of components.
2. The ripple voltage is low because the circuit has low ripple factor.
3. Capacitor filter is suitable for high voltage at small value of load currents.

Disadvantages of Capacitor Filter

1. Voltage regulation is very poor.
2. Ripple factor depends on load resistance.
3. Ripple content increases with decrease in load resistance.

1.6.4 Voltage Regulation

In an unregulated power supply, output voltage changes whenever input supply voltage or load resistance changes. It is never constant. The change in voltage from no-load to full-load condition is called voltage regulation. The aim of a voltage regulator circuit is to reduce these variations to zero or, at least, to the minimum possible value. Voltage regulation is the next stage of filter.

The percentage regulation or simply, regulation of a power supply is given by

$$\% \text{ regulation} = \frac{V_{max} - V_{min}}{V_{max}} \times 100 \qquad \text{...(1.13)}$$

where

V_{max} = maximum dc output voltage

V_{min} = minimum dc output voltage

In general,

$$\% \text{ regulation} = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100 \qquad \text{...(1.14)}$$

V_{NL} = no-load or open-circuit terminal voltage of the sypply

V_{FL} = full-load terminal voltage of the supply

1.7 POWER SUPPLIES

1.7.1 Principle

A regulated power supply is an electronic circuit designed to keep the output voltage nearly constant under varying input voltage conditions and varying load conditions. A dc regulated power supply consists of various stages as shown in Fig. 1.29.

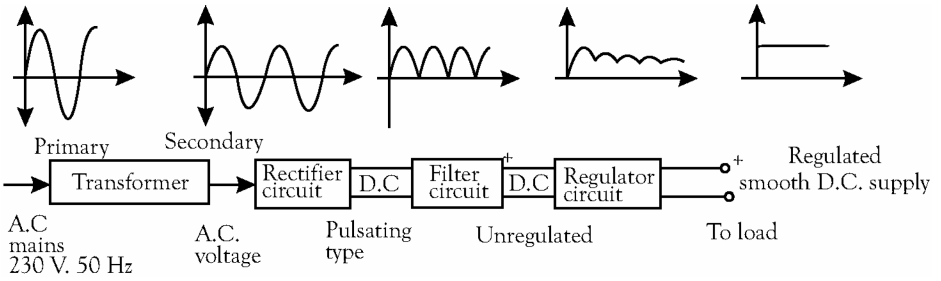


Figure 1.29 *Regulated dc power supply*

In regulated power supply, an ac voltage (of 230 V, 50 Hz) is step downed by means of a suitable transformer and converted into pulsating voltage by means of a rectifier circuit. To remove the ripple content of the signal, a filter circuit is used. The output of the filter circuit is a smooth dc voltage but unregulated. By means of a voltage regulator circuit as the last stage, the power supply provides constant dc voltage at the output. Presently, the complete regulator circuit is available in IC (Integrated Circuit) form.

1.7.2 Power Supply Performance Parameters

(1) Source Effect

In power supply, if the input ac voltage (line voltage) varies due to certain reasons, then there is a tendency of variation in output dc voltage (load voltage) of the regulator.

Source regulation (SR) is defined as the change in regulated dc load voltage for a specified range of line voltage typically 230 V ± 10%.

$$SR = V_{HL} - V_{LL}$$

where, V_{HL} = load voltage with high line voltage

V_{LL} = load voltage with low line voltage

The percentage of load voltage is defined as

$$\% SR = \frac{SR}{V_{nom}} \times 100 \qquad ...(1.15)$$

where V_{nom} is nominal load voltage.

(2) Load Effect

The load regulation is the change in regulated output voltage when the load current is changed from minimum to maximum.

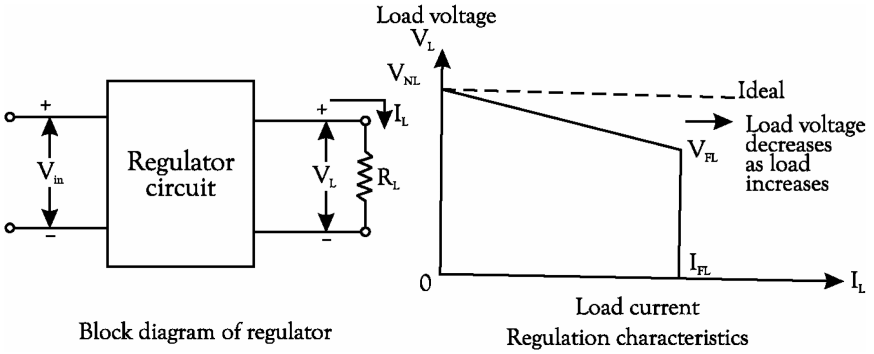


Figure 1.30 *Load regulation in power supply*

The load regulation (LR) is expressed as

$$LR = V_{NL} - V_{FL}$$

where, V_{NL} = load voltage with no load current

V_{FL} = load voltage with full load current

It can be expressed in percentage as follows:

$$\% \text{ LR} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 \qquad \text{...(1.16)}$$

The graph of load current against load voltage is called regulation characteristics of power supply (Fig. 1.30). Less load regulation, better is the performance of the regulator.

(3) Output Resistance

It is defined as change in output dc voltage for corresponding change in load current when input ac voltage and the temperature of the system are constant.

$$R_{out} = \frac{\Delta V_{out}}{\Delta I_L}\Big|_{V_{in} \text{ and temperature constant}} \qquad \text{...(1.17)}$$

(4) Voltage Stability Factor (S_V)

It is defined as change in output dc voltage for corresponding change in input ac voltage when load current and the temperature of the system are constant. Smaller the value of S_V, better the performance the power supply.

$$S_V = \frac{\Delta V_{out}}{\Delta V_{in}}\Big|_{I_L \text{ and temperature constant}} \quad \text{... (1.18)}$$

(5) Temperature Stability Factor

It is defined as follows:

$$S_T = \frac{\Delta V_{out}}{\Delta T}\Big|_{V_{in} \text{ and } I_L \text{ constant}} \quad \text{...(1.19)}$$

The value of S_T must be as small as possible for good power supply.

(6) Ripple Rejection (RR)

It is a factor which indicates how effectively the regulator circuit rejects the ripples and attenuates it from input to output. If V_R is the ripple voltage, then the Ripple rejection is defined as

$$RR = \frac{\text{Ripple content in output}}{\text{Ripple content in input}} = \frac{V_{R(out)}}{V_{R(in)}}$$

In decibels it is written as:

$$RR' = 20 \text{ Log}_{10} RR \text{ dB} \quad \text{...(1.20)}$$

1.7.3 Zener Diode Voltage Regulators

Principle

A voltage regulator provides constant output voltage irrespective of small variations in input voltage. Zener diode is specially designed to operate in breakdown region called **Zener breakdown**, where current is limited only by external resistance and the power dissipation of the diode. i.e., once the applied voltage under reverse bias is equal to breakdown voltage, the current increases very rapidly and the diode voltage (V_Z) stays essentially constant. This property of Zener diode can be used for voltage regulation.

Circuit

Fig. 1.31 shows a circuit of Zener diode shunt regulator. Since the Zener is connected in parallel (or shunt) with the load, therefore the circuit is known as shunt regulator. A resistance, (R_S) is connected in series with the Zener to limit current in the circuit. Therefore, the resistance R_S is also known as series current limiting resistor. The output voltage (V_L) is taken across the load resistance (R_S). For proper operation, the input voltage (V_S) must be greater than the Zener voltage (V_Z). This ensures that Zener operates in the reverse breakdown region.

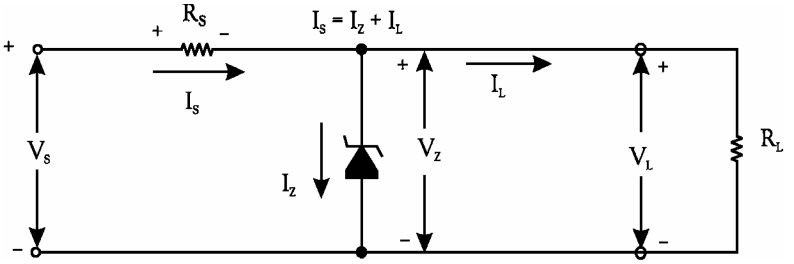


Figure 1.31 *Circuit diagram of Zener diode voltage regulator*

The input current (*i.e.,* current through the limiting resistor) is given by

$$I_S = \frac{V_S - V_Z}{R_S}$$

where V_S is the dc input voltage to the regulator and V_Z is the Zener voltage.

If the reverse resistance of Zener diode is r_Z, then there is a voltage drop across it which is equal to $I_Z . r_Z$. Therefore, the voltage across the terminals of the Zener diode is

$$V_L = V_Z + I_Z . r_Z \qquad ...(1.21)$$

If the Zener resistance is negligible, then the load voltage, $V_L = V_Z$ and the current through the load resistance is given by the relation,

$$I_L = \frac{V_L}{R_L} \text{ and } I_Z = I_S - I_L \qquad ...(1.22)$$

Working

The working of Zener diode regulator may be discussed under the two heads, namely regulation with varying input voltage and regulation with varying load resistance.

1. Regulation with varying input voltage: Consider the regulator circuit as shown in Fig. 1.32 (a). Here the load resistance (R_L) is kept fixed and the input voltage (V_S) varies within the limits.

(i) If the input voltage increases, the input current (I_S) also increases. This increases the current through Zener diode, without affecting the load current (I_L). The increase in input current will also increase the voltage drop across series resistance (R_S), thereby keeping the load voltage (V_L) as constant.

(ii) On the other hand, if the input voltage decreases, the input current (I_S) also decreases. As a result, the current through Zener (I_Z) will also decreases. Consequently, the voltage drop across series resistance (R_S) will be reduced. Thus the load voltage (V_L) and load current (l_L) remains constant.

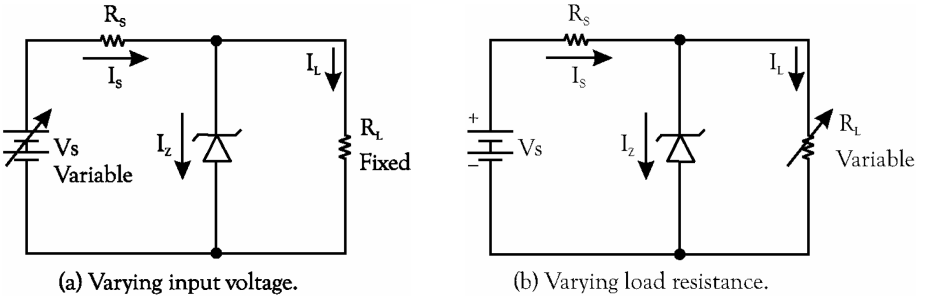


Figure 1.32 *Zener regulation with (a) varying input voltage, (b) Varying load resistance*

2. Regulation with varying load resistance: Consider the regulator circuit as shown in Fig. 1.32 (b). Here the input voltage (V_S) is kept fixed and the load resistance (R_L) varies. The variation of load resistance changes the load current (I_L) through it, thereby changing load voltage (V_L) across it.

(i) When the load resistance (R_L) decreases, the load current (I_L) increases. This causes the Zener current (I_Z) to decrease. As a result of this, the input current and the voltage drop across series resistance (R_S) remains constant. Thus the load voltage (V_L) remains constant.

(ii) On the other hand, if the load resistance increases, the load current decreases. As a result, the Zener current increases. This again keeps the values of input current and voltage drop across series resistance (R_S) as constant. Thus the load voltage (V_L) remains constant.

Optimum Value of Current Limiting Resistor (R_S):

The value of current limiting resistor must be properly selected to fulfill the following two requirements:

1. When the input voltage is minimum and the load current is maximum, sufficient current must be supplied to keep the Zener diode within its breakdown region (or regulating region).
2. When the input voltage is maximum and the load current is minimum, the Zener current must not increase the maximum rated value.

The optimum value of current limiting Resistor (R_S) can be determined by using the following two equations for maximum and minimum values of Zener current:

$$I_{Z(\max)} = \frac{V_{S(\max)} - V_Z}{R_S} - I_{L(\min)} \quad \text{...(i)}$$

$$I_{Z(\min)} = \frac{V_{S(\min)} - V_Z}{R_S} - I_{L(\max)} \quad \text{...(ii)}$$

From equation (i), we find that the minimum value of current limiting resistor,

$$R_{S(min)} = \frac{V_{S(max)} - V_Z}{I_{Z(max)} + I_{L(min)}} \quad ...(1.23)$$

and from equation (ii), the maximum value of current limiting resistor,

$$R_{S(max)} = \frac{V_{S(min)} - V_Z}{I_{Z(min)} + I_{L(max)}} \quad ...(1.24)$$

The value of current limiting resistor (R_S) should be chosen in such a way that its value should be between R_S(max) and R_S(min) i.e.,

R_S (min) < R_S < R_S (max)

Disadvantages of Zener-diode Shunt Regulator:

Following are the disadvantages of a Zener diode shunt regulator:

1. The maximum load current, which can be supplied to load resistor (R_L) is limited to I_Z (max) - I_Z (min) which is usually of few milli amperes.
2. A large amount of power is wasted in the Zener-diode and the series resistance (R_S) in comparison with the load power.
3. The regulation factor and the output resistance are not very low.

SOLVED PROBLEMS

1. *A variation of 0.02 V across a 3.8 V Zener produces a current change from 20 mA to 22 mA. Calculate the dynamic resistance of the device ?*

Solution:

Given : The change in Zener voltage = ΔV_Z = 0.02 V

The change in Zener current = ΔI_Z = 22 – 20 = 2 mA

The dynamic resistance $r_Z = \Delta V_Z / \Delta I_Z = 0.02 / 2 \times 10^{-3} = 10\ \Omega$

2. *A 4.7 V Zener has a resistance of 15Ω. What is the terminal voltage, when the current is 20 mA?*

Solution:

Given V_Z = 4.7 volts; r_Z = 15Ω and I_Z = 20 mA = 20 X 10^{-3} A.

We know that the terminal voltages of a Zener diode,

Then $V_Z = (V_Z + I_Z \cdot r_Z) = 4.7 + (20 \times 10^{-3}) \times 15 = 5$ V.

Rectifiers:

3. *The input of a Half-wave rectifier is V = 200 sin 40 t. If R_L = 1KΩ, and forward resistance of the diode is 30 Ω, find (i) The dc current through the diode, (ii) The ac value of current in the circuit, (iii) dc output voltage, (iv) dc power input, (v) Rectifier efficiency ?*

Solution:

Given: Vi = 200 sin 40 t —— (i) then V_m = 200 V,

$I_m = V_m/R_f + R_L$ = 200 / 1030 = 194 mA

(i) $I_{dc} = I_m/\pi$ = 194/π = 62.8 mA

(ii) $I_{rms} = I_m/2$ = 194/2 = 97 mA

(iii) Output dc voltage = $I_{dc} \times R_L$ = 62.8 x 10^{-3} x 1 x 10^{+3} = 62.8 V

(iv) Input ac Power = $P_{ac} = (I_{rms})^2 \times R_F + R_L$ = 0.097 x 0.097 x 1030 = 9.69 W

(v) Output dc Power = $P_{dc} = (I_{dc})^2 \times R_L$ = $(0.0628)^2$ x 1 x 10^{+3} = 3.94 W

(vi) Rectifier Efficiency = $\eta = (P_{dc}/P_{ac}) \times 100$ = 3.94/9.69 x 100 = 40.66

4. *In a Half-Wave Rectifier, the input is 300 sin 314 t. Find its average output voltage.* *(VTU 99)*

Solution:

Given : V_m = 300 V

Average output voltage = $V_{dc} = V_m/\pi$ = 300/3.14 = 95.5 V

5. *In a Centre- tap Full-Wave-Rectifier, the load resistance is 1.5 KΩ. Each has a forward resistance of 6 Ω. The voltage across half the secondary winding is 220 V. Find the Ripple Factor and Rectifier Efficiency.*

Solution:

Given : V_{rms} = 220 V,

(i) Peak value of Voltage = $V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 220$ = 311 V

(ii) Peak value of load current $I_m = V_m/R_f + R_L$ = 311 / (6 + 1500) = 0.207 A

(iii) DC load current $I_{dc} = 2I_m/\pi$ = 2 x 0.207 / 3.14 = 0.132 A

(iv) RMS value of load current $I_{rms} = I_m/\sqrt{2}$ = 0.207/√2 = 0.146 A

(v) Ripple Factor =

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{0.146}{0.132}\right)^2 - 1} = 0.473$$

(vi) Rectification Efficiency, $\eta = (P_{dc}/P_{ac}) = (I_{dc}^2 \times R_L)/(I_{rms}^2(R_F + R_L))$

= $[(0.132)^2 \times 1500] / (0.146)^2 \times (6 + 1500)$ = 0.814 or 81.4 %

6. *In a Bridge Rectifier the input is from 230 V, 50 Hz mains. Calculate D.C. output voltage.*

Solution:

Given: Input Voltage = 230 V (r.m.s)

Peak value of voltage $V_m = \sqrt{2}$ x r.m.s = √2 x 230 = 325 V

∴ D.C. Output Voltage $V_{dc} = 2V_m/\pi$ = (2 x 325)/π = 207 V

Filters:

7. *If a capacitor of 1000 μF is used as a filter in (a), calculate the Ripple Factor and (b) D.C. Output.*

(March 99, V.T.U.)

Solution:

Given $C = 1000\ \mu F$

Taking Load Resistance $R_L = 100$ ohms

(a) Ripple Factor $\gamma = 1/ (4\sqrt{3}fCR_L)$

$= 1/(4 \times \sqrt{3} \times 50 \times 1000 \times 10^{-6} \times 100 = 0.028$

(b) D.C. Output

$$V_{dc} = \left(\frac{4 f R_L C}{4 f R_L C + 1} \right) V_m$$

Now, $4fCR_L = (4 \times 50 \times 100 \times 1000 \times 10^{-6}) = 20$

$\therefore$ $V_{dc} = (20/21)\ V_m = (20/21)\ 325 = 309.5$ V.

8. *Calculate the value of capacitor has to be used for the capacitor filter of a full wave rectifier to get a ripple of 0.01 %. The rectifier supplies a load of 3 KΩ while the supply frequency is 50 Hz.*

Solution:

Given: $\gamma = 0.01\%$, $R_L = 3$ KΩ, and f = 50 Hz.

For a capacitor filter in full wave rectifier circuit $\gamma = 1 /(4\sqrt{3}\ f\ CR_L) \times 100\ \%$

$0.01 = 1 / (4\sqrt{3} \times 50 \times C \times 3000) \times 100$

or $C = 5.55$ mF.

9. *In a Full Wave Rectifier with a capacitor filter, the load current from the circuit operating from 230 V, 50 Hz supply is 10 mA. Estimate the value of capacitor required to keep the ripple factor less than 1%.*

(VTU July 2004)

Solution:

Given: $V_S(rms) = 230$ V, f = 50 Hz, $I_L = 10$ mA, $\gamma = 1\ \% = 0.01$

Then $V_{sm} = \sqrt{2}\ V_s(rms) = \sqrt{2} \times 230 = 325.269$ V

$V_{dc} = 2V_{sm}/\pi$ for full wave rectifier or $I_{dc} = 2V_{sm}/\pi R_L$

or $R_L = 2V_{sm}/\pi I_L = (2 \times 325.269) / (\pi \times 10 \times 10^{-3}) = 20.7$ KΩ.

Then the value of Capacitor:

$\gamma = 1/(4\sqrt{3}fCR_L)$

$0.01 = 1/(4\sqrt{3} \times 50 \times C \times 20.7 \times 10^{+3}) \times 100$

or $C = 1/(4\sqrt{3} \times 50 \times 0.01 \times 20.7 \times 10^{+3}) \times 100$

or $C = 1.39 \times 10^{-5}$ F $= 13.94\ \mu F$

Power Supply Performance Parameters

10. *The output voltage of a d.c. power supply system varies from 40 V to 39.6 V when the load current is raised from zero to its maximum specified level. The voltage also increases to 40.5 V when the a.c. supply increases by 10%. Calculate the load and source effects, and the load and line regulation.*

Solution:

Given:

Formula:

(1) Load effect = ΔV_o for $\Delta I_{L\,(max)}$

= 40 – 39.6 = 0.4 V = 400 mV

(2) Load regulation = $[(\Delta V_o \text{ for } \Delta I_{L(max)}) / V_o] \times 100 = [400 \text{ mV}/40] \times 100 = 1.0\ \%$

(3) Source effect = ΔV_o for 10% change in V_S

= 40.5 - 40 = 0.5 V = 500 mV

(4) Line regulation = $(\Delta V_o$ for 10% change in $V_S)/V_o \times 100$

= (500 mV/40) × 100 = 1.25%

Zener diode voltage regulators

11. *For a Zener regulator shown in Fig. 1. 33, calculate the range of input voltage for which output remain constant ? Given : V_Z = 6.1 V, I_{Zmin} = 2.5 mA, I_{Zmax} = 25 mA, r_Z = 0 Ω*

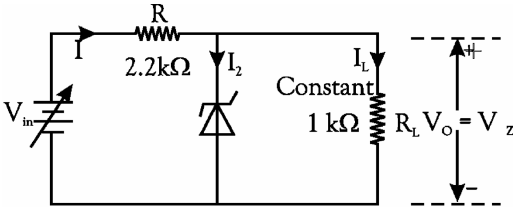


Figure 1.33 *Zener diode voltage regulator*

Solution:

Given : R_L = 1 KΩ, V_Z = 6.1 V,

Then $I_L = V_Z/R_L = 6.1/1000 = 6.1$ mA (is always constant)

For $V_{in(min)}$, $I_Z = I_{Zmin} = 2.5$ mA

$\therefore$ $I = I_{Zmin} + I_L = (2.5 + 6.1)$ mA $= 8.6$ mA

$\therefore$ $V_{in(min)} = V_Z + IR = 6.1 + 8.6 \times 10^{-3} \times 2.2 \times 10^3 = 25.02$ V

For $V_{in(max)}$, $I_Z = I_{Zmax} = 25$ mA

$\therefore$ $I = I_{Zmax} + I_L = (25 + 6.1)$ mA $= 31.1$ mA

$\therefore$ $V_{in(min)} = V_Z + IR = 6.1 + 31.1 \times 10^{-3} \times 2.2 \times 10^3 = 74.52$ V

Thus the range of input voltage is 25.02 V to 74.52 V, for which the output will be constant.

12. *Design a zener voltage regulator for the following specifications:*

Output voltage Vo = 5V, Input voltage V_i *= 12 ± 3 V,* I_{Zmin} *= 10 mA, Load current* I_L *= 20 mA, and Zener wattage* P_Z *= 500 mW.*

Solution:

Given: $V_{in(min)} = 12 - 3 = 9$ V, $V_{in(max)} = 12 + 3 = 15$ V, $I_L = 20$ mA (should be constant), $V_O = V_Z = 5$ V, $P_Z = 500$ mW.

(i) The maximum power dissipation is corresponding to I_{Zmax}.

$$\therefore \quad P_Z(\text{given}) = V_Z I_{Zmax} \Rightarrow 500 \times 10^{-3} = 5 \times I_{Zmax}$$

$$\therefore \quad I_{Zmax} = 100 \text{ mA}$$

(ii) Since I_L = constant, For $V_{in(max)}$, $I_Z = I_{Zmax}$

$$\therefore \quad I = I_L + I_{Zmax} = 20 + 100 = 120 \text{ mA}$$

and $$V_{in(max)} = V_Z + I R_{min}$$

$$\therefore \quad R_{min} = (15 - 5) / 120 \times 10^{-3} = 83.33\ \Omega$$

When $R = R_{min}$, for $V_{in(max)}$ = the current I will be at its maximum i.e., I_Z will be at its maximum.

(iii) To calculate R_{max}, I must be minimum i.e., I_Z must be minimum = 10 mA.

$$\therefore \quad I = I_L + I_{Zmin} = 20 + 10 = 30 \text{ mA}$$

$$\therefore \quad V_{in(min)} = V_Z + I \times R_{max}$$

$$\therefore \quad R_{max} = (9 - 5) / (30 \times 10^{-3}) = 133.33\ \Omega$$

Thus R must be greater than 83.33 Ω and less than 133.33 Ω for proper regulating action.

13. *Determine the minimum and maximum load currents for which the Zener diode will maintain regulation in Fig. 1.34. What is the minimum* R_L *that can be used ?* V_Z *= 8 V,* I_{Zmin} *= 5 mA, and* I_{Zmax} *= 50 mA. Assume that* r_Z *= 0*

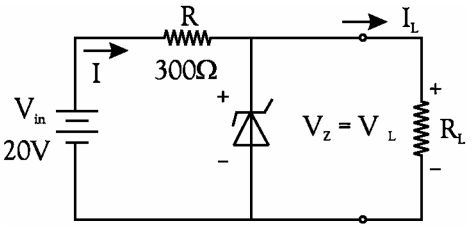


Figure 1.34 *Voltage regulator*

Solution:

Given: $V_Z = 8$ V, $I_{Zmin} = 5$ mA, $I_{Zmax} = 25$ mA, $V_{in} = 20$ V.

Total current $I = (V_{in} - V_Z) / R = (20 - 8) / 300 = 40$ mA

Now $I = I_L + I_Z$ = constant

For $I_{L(min)}$, $I_Z = I_{Zmax}$

$\therefore$ $I_{L(min)} = I - I_{Zmax} = 40 - 25 = 15$ mA ...(i)

For $I_{L(max)} = I_Z - I_{Z(min)}$

$\therefore$ $I_{L(max)} = I - I_{Zmin} = 40 - 5 = 35$ mA ...(ii)

So, load current can vary from 15 mA to 35 mA for which the output will be constant.

The minimum value of R_L corresponding to maximum value of I_L. Hence

$R_{L(min)} = = V_Z / I_{L(max)} = 8 / (35 \times 10^{-3}) = 228.57\ \Omega$ ...(iii)

14. *A zener diode connected in series with a current-limiting resistor, supplied by a 30 V supply, is required to be designed as an 8.2 V reference source. Select suitable components and calculate the circuit current when the supply voltage drops to 25 V. Given : $V_Z = 8.2$ V, $I_Z = 20$ mA.*

Solution:

If $V_S = 30$ V

$R_S = (V_S - V_Z) / I_Z = (30 - 7) / 20 \times 10^{-3} = 1.15\ K\Omega$ ...(i)

P_D for R_S, $P_{RS} = I_Z^2 R_S = (20\ rnA)^2 \times 1.15\ K\Omega = 0.529$ W ...(ii)

If $V_S = 25$ V

$I_Z = (V_S - V_Z) / R_S = (25 - 7) / 1.15 \times 10^{+3} = 15.65$ mA ...(iii)

EXERCISES

I. Descriptive Type Questions

1. With circuit diagram, explain forward bias and reverse bias operations of a semiconductor junction diode.
2. Sketch typical forward and reverse characteristics for a germanium and for a silicon diode. Discuss the characteristics.
3. What is the purpose of a d.c load line ? Write the equation for drawing a d.c.load line for a series circuit made up of supply voltage V_S, a resistor R_S and a diode *D*. *(VTU Jan 2008)*
4. Sketch the complete equivalent circuits for forward-biased and reverse-biased diodes. Also, sketch the a.c. equivalent circuit for a forward-biased diode. Briefly explain each circuit.
5. What are the different types of junction breakdown that can occur in a reverse-biased diode ? Explain in brief?
6. Draw the *V-I* characteristics for a Zener diode. Explain the shape of the characteristics and identify the important points.
7. (a) Draw the circuit for a half-wave rectifier and explain its working. (b) Give any 4 device parameters. (c) List its advantages and disadvantages.
8. Draw the circuit for a full-wave rectifier and explain its working. (b) Give any 4 device parameters. (c) List its advantages and disadvantages. *(VTU June 2009)*
9. Draw the circuit of a bridge rectifier and explain its working. (b) Give any 4 device parameters. (c) List its advantages and disadvantages. *(VTU Jan 2008)*
10. With the help of a circuit diagram and waveforms explain the working of a capacitive filter.
11. Define 'power supply source effect' and 'load effect', and, write the equations for each. Also write equations for 'line regulation' and 'load regulation.
12. With neat diagram explain Zener diode voltage regulator. Discuss the performance of the Zener diode in terms of the source and load effects. *(VTU Jan 2007, 2008)*
13. Draw and explain the V-I characteristic of Si and Ge diodes. *(VTU Jan 2010)*
14. Draw the circuit of a half wave rectifier and explain its working with necessary waveforms. *(VTU Jan 2010)*
15. What is a P-N Junction? Draw and explain the V-I characteristics of P-N Junction. *(VTU Jan 2009)*
16. Derive an expression for ripple factor and output DC voltage of a full-wave rectifier with C filter. *(VTU Jan 2009)*
17. Draw the circuit of a full-wave bridge rectifier and show that ripple factor = 0.48 and efficiency = 81%. *(VTU June 2008)*
18. Explain the operation of a half-wave rectifier with capacitor filter with the help of a circuit diagram and relevant waveforms. *(VTU Jan 2007)*

II. Multiple Choice Questions

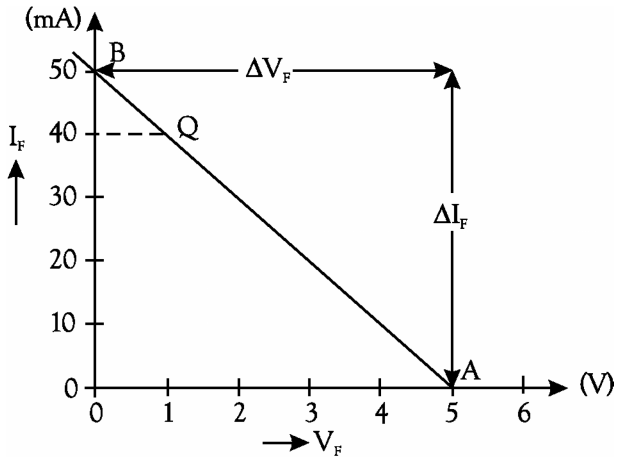
1. The cut-in voltage of a Si p-n diode is about
   (a) 0.6 V (b) 0.6 mV
   (c) 1.2 V (d) 1.2 mV
2. The ripple factor for a full-wave rectifier is _____
   (a) 0.482 (b) 0.5
   (c) 1.21 (d) –1.21
3. The Zener resistance of a Zener diode, which exhibits. 50 mV change in V_z for a 2.5 mA change in I_z is _____
   (a) 10 Ω (b) 40 Ω
   (c) 20 Ω (d) 25 Ω
4. The average output voltage of half wave rectifier with an input of 300 Sin 314t is _____
   (a) 100 V (b) 95.49 V
   (c) 90.49 V (d) 90.0 V
5. The depletion region capacitance effect occurs in a diode when it is _____
   (a) Forward Biased (b) Reverse Biased
   (c) Unbiased (d) All of these
6. When the diode is forward biased it is equivalent to _____
   (a) Open Switch (b) Closed Switch
   (c) High Resistance (d) None
7. When the diode is reverse biased it is equivalent to _____
   (a) OFF Switch (b) ON Switch
   (c) High Resistance (d) None
8. The resistance of the P-N Junction diode is equal to _____
   (a) Ohmic resistance of P-N diode (b) Junction resistance
   (c) Reverse resistance (d) Algebraic sum of A & B
9. The conventional current in P-N junction diode flows _____
   (a) From positive to negative (b) From negative to positive
   (c) In the direction opposite to the electron flow
   (d) Both A & C
10. Cut-in Voltage of germanium diode is _____
    (a) 0.6 V (b) 0.3 V
    (c) 1.3 V (d) 0.3 mV

11. The output voltage of Zener diode voltage regulator is equal to _____
    (a) V_{in} (b) V_S
    (c) V_Z (d) V_{ac}
12. In Full-Wave rectifier, the ripple voltage is _____ of Half-wave rectifier.
    (a) Double (b) Half
    (c) Equal (d) Quarter
13. Ripple voltage of Half-wave rectifier is _____
    (a) 0.482 (b) 1.21
    (c) Equal to Full-wave rectifier (d) 0.89
14. Efficiency of Half-wave rectifier is _____
    (a) 40.6 % (b) 50 %
    (c) 81.2 % (d) 89 %
15. Zener diode is _____ doped compared to semiconductor P-N Junction diode.
    (a) Lightly (b) Heavily
    (c) Equally (d) Un-doped
16. In Zener diode, which of the following is true _____
    (a) At low reverse voltage below 6V, Zener breakdown becomes predominant
    (b) At low reverse voltage below 6 V, avalanche breakdown becomes predominant
    (c) At high reverse voltage above 6V, Zener breakdown becomes predominant
    (d) All the above.
17. 1N4728 is a _____
    (a) P-N Junction diode (b) Zener diode
    (c) NPN Transistor (d) JFET
18. Efficiency of Full-wave rectifier is about _____
    (a) 40.6 % (b) 50 %
    (c) 81.2 % (d) 89 %
19. Zener diode is used as a voltage regulator when it is _____ biased
    (a) Forward (b) Reverse
    (c) Unbiased (d) None of these
20. Zener diode acts as a _____ device
    (a) Constant current (b) Constant voltage
    (c) Constant power (d) Variable voltage

21. The barrier potential of silicon diode is approximately _____
    (a) 0.3 V (b) 0.1 V
    (c) 0.7 V (d) 1.2 V
22. A half-wave rectifier is fed from secondary of a transformer whose output voltage is 12.6 V. The dc voltage of the rectifier output is _____
    (a) 12.6 V (b) 5.66 V
    (c) 17.8 V (d) 11.32 V
23. In full-wave rectification, if the input frequency is 50 Hz, then the output frequency is _____
    (a) 50 Hz (b) 100 Hz
    (c) 0 Hz (d) None of above
24. In Half-wave rectification, if the input frequency is 50 Hz, then the output frequency is _____
    (a) 50 Hz (b) 100 Hz
    (c) 0 Hz (d) None of above
25. If the P-N junction is heavily doped, breakdown voltage will _____
    (a) Increases (b) Decreases
    (c) Remains constant (d) None of these

III. Numerical Problems

1. Calculate the load resistance for the circuit shown in following figure where V_S = 5 V to produce a 40 mA diode forward current.



Ans: Draw dc load line, From load line $R_S = \Delta V_F/\Delta I_F = 100\ \Omega$

2. A diode whose internal resistance is 20 Ω is to supply power to a 1 KΩ load from a 20 V, 50 Hz supply. Calculate (i) The peak load current, (ii) The dc load current, (iii) The ac load current, (iv) The dc diode voltage, (v) The total input power to the circuit, and (vi) the percentage of regulation from no-load to the given load.

   Ans: (i) I_m = 27.45 mA, (ii) I_{dc} = 8.74 mA, (iii) I_{rms} = 13.725 mA, (iv) DC diode voltage = 8.74 V, (v) Input power = 0.192 W, (vi) % of regulation = 2.97 %.

3. In a Half-wave rectifier circuit fed from 230 V, 50 Hz mains, it is desired to have a ripple factor, $\gamma \leq 0.005$. Estimate the value of the capacitance needed. I_L = 0.5 A. *(VTU 99)*

   Ans: V_{Smax} = 70.7 V, R_L = 141.4 Ω, C = 8166 μF.

4. A single phase Full-wave rectifier supplies power to a 1 KΩ load. The ac voltage applied to the diodes is 300 – 0–300 V. If diode resistance is 25 Ω and that of the transformer secondary is negligible, determine (i) Average load current, (ii) Average load voltage (iii) r.m.s. value of ripple voltage (iv) Rectifier Efficiency.

   Ans: V_m = 0.263 V, V_{dc} = 263 V, γ = 126.8, η = 79.1 %.

5. In a centre-tap Full-wave rectifier, the forward resistance of the diode is 10 Ω, the load resistance is 2 KΩ. The voltage across half the secondary winding is 220 V. Calculate the ripple factor and efficiency of rectification. If the capacitor of 25 μF is connected across the load what is the modified ripple factor ?

   Ans: I_{dc} = 0.098 A, γ = 0.51, η = 78.9, Modified γ = 0.057.

6. For a bridge rectifier circuit, the secondary voltage is given by $V_S = 50 \sin \omega t$, and the load resistance R_L = 8 KΩ. Calculate (i) DC output voltage, (ii) Percentage efficiency. Assume ideal diodes.

   Ans: I_{dc} = 0.04 A, V_{dc} = 31.8 V, η = 81.2 %.

7. Calculate the output dc voltage and efficiency for the bridge rectifier, given, Load resistance = 100 Ω, Diode forward resistance = 10 Ω, AC input voltage = 300 sin 314t.

   Ans: V_{dc} = 160 V, η = 67.6 %.

8. Design a Zener regulator for the following specifications : Output voltage V_O = 5V, Input voltage V_i = 12 ± 3 V, Load current I_L = 20 mA, Zener wattage P_Z = 500 mW. *(VTU 1999)*

   Ans: $V_O = V_Z$ = 5V, R_{max} = 160 Ω, R_{min} = 83.33 Ω.

9. Design a voltage regulator using Zener diode to meet the following requirements : Unregulated output = 20-30 Volts, Regulated output = 10 volts, Load current = 0-10 mA, I_{Zmin} = 2 mA, I_{Zmax} = 50 mA. Draw the circuit diagram and insert the component values. *(VTU 2002)*

   Ans: $V_O = V_Z$ = 10 V, $R_{Lmin} = V_O/I_{Lmax}$ = 1 KΩ, R_{max} = 833.33 Ω, R_{min} = 400 Ω.

10. A 9.1 V reference voltage source is to be designed using a low-power loaded Zener diode so as to produce the maximum possible load current. The circuit is operated from a 20 V supply. Determine the maximum load current that the circuit can produce. Given : P_D = 500 mW.

    Ans: $I_{Zm} = P_D/V_Z$ = 54.9 mA, R_S = 198.4 Ω, I_{Lmax} = 50 mA.

11. A 24 V, 600 mW Zener diode is used for providing a 24 V stabilized supply to a variable load. If the input voltage is 32 V, calculate (i) The value of series resistance required. (ii) Diode current when the load is 1200 Ω. *(VTU 2003)*

    Ans: R_{min} = 320 Ω, I_L = 20 mA, I_T = 25 mA, $I_Z = I_{Zmin}$ = 5 mA.

12. Design a Zener Regulator for the following specifications : Output voltage = 5 V, Load Current = 10 mA, Zener Wattage = 400 mW, Input Voltage = 10 V ± 2 V.

    Ans: R_L = 500 Ω, R_S = any value between 77.77 Ω to 300 Ω, V_Z = 5 V.

13. A diode with V_F = 0.7 V is connected as a half wave rectifier. The load resistance is 600 Ω and the (rms) ac input is 240 V. Determine the peak, output voltage, the peak load current and the diode peak reverse voltage. *(VTU Jan 2010)*

14. A Zener diode has a breakdown voltage of 10 V. It is supplied from a voltage source varying between 20-40 V in series with a resistance of 820 Ω. Using ideal Zener model, obtain the minimum and maximum Zener currents. *(VTU June 2009)*

15. Design a Zener Regulator with the following specifications : V_O = 12 V, V_{in} = (25 – 35) V, I_L = (35 – 55 mA) and I_Z = (25 – 45) mA. *(VTU June 2008)*

16. A full wave bridge rectifier supplies a load of 400 Ω in parallel with a capacitor of 500 μF. If the ac supply voltage is 230 sin 314 t Volts, find the (i) Ripple factor and (ii) DC load current.

    (VTU Jan 2007)

Answers to Multiple Choice Questions

1. (a)	2. (a)	3. (c)	4. (b)	5. (d)	6. (b)	7. (a)	8. (d)	9. (d)	10. (b)	11. (c)
12 (b)	13. (b)	14. (a)	15. (b)	16. (a)	17. (b)	18. (c)	19. (b)	20. (b)	21. (c)	22. (b)
23. (b)	24. (a)	25. (b).								

UNIT 2

TRANSISTORS

OBJECTIVES

In this Unit we will study Bipolar Junction Transistor, another basic active component used in electronic circuits to amplify or to switch the voltage or current. The Unit objectives are :

(1) To study constructional features of Bipolar Junction Transistors of different types.

(2) To analyze Transistor Voltages and currents.

(3) To study Amplification process using transistor.

(4) To study and compare Common Base, Common Emitter, and Common Collector configuration characteristics.

(5) To study and analyze DC Load line and Bias Point of transistors.

2.1 BIPOLAR JUNCTION TRANSISTOR

2.1.1 Introduction

An electronic component used to transfer a signal from low resistance region to high resistance region, or vice versa, is called transistor (TRANsfer reSISTER). Transistor is a semiconductor component used in electronic circuits. There are two types of transistors: (1) Bipolar Bi-Junction Transistor (BJT) (2) Field Effect Transistor (FET). BJT has two types of charge carriers as electrons and holes (hence bipolar) and two P-N junctions (bi-junction). Based on construction, Bipolar transistors are divided into two types as : (1) N-P-N transistor and (2) P-N-P transistor. Transistors are used in electronic circuits mainly for two purposes : (1) applications related to signal amplification in communication electronics, (2) applications related to switching of signal level in digital electronics.

BJT is first invented on 23 December, 1947, by Walter H. Brattain, William Shockley and John Bardeen at the Bell Telephone Laboratories, USA, and for this invention they got Noble Prize in 1956.

BJT consists of two back-to-back *P-N* junctions manufactured in a single piece of a semiconductor crystal. These two junctions give rise to three regions called emitter, base and collector and provided with terminals which are labelled as *E, B* and C. The two junctions are: emitter-base *(E/B)* junction and collector-base *(C/B)* junction. In a BJT following points are worth to note:

(1) Emitter is more *heavily doped* than any of the other regions because its main function is to supply majority charge carriers (either electrons or holes) to the base.

(2) Base forms the middle section of the transistor. It is very thin (10^{-6} m) as compared to either the emitter or collector and is very *lightly-doped.*

(3) Collectors main function (as indicated by its name) is to collect majority charge carriers from the emitter through the base.

(4) The collector region is made *physically larger* than the emitter region because it has to dissipate much greater power, and hence there is no possibility of inverting the transistor *i.e.,* making its collector as the emitter and its emitter as the collector.

(5) The conventional current direction is always opposite to the direction of flow of electrons.

2.1.2 Structure of NPN Transistor

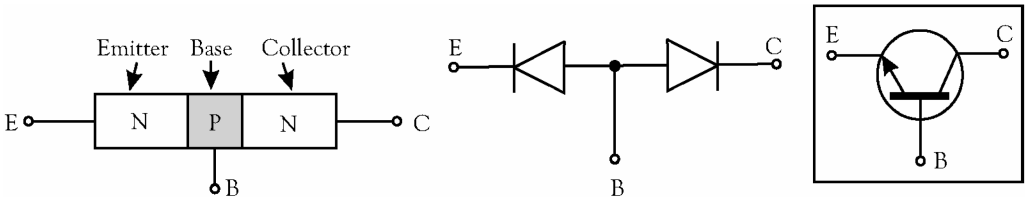


Figure 2.1 *(a) The structure of the NPN transistor, (b) Diode equivalent and (c) Its symbol*

In unbiased (without any external battery) transistor, during the fabrication, the depletion region penetrates more deeply into lightly doped side in order to include an equal number of impurity atoms in each side of the junction. The depletion region at emitter junction penetrates less in the heavily doped emitter and extends more in the base region. Similarly, depletion region at collector junction penetrates less in heavily doped collector and extends more in the base region. Since collector is slightly less doped than the emitter, the depletion layer width at the collector junction is more than emitter junction.

Fig. 2.2, shows the detailed internal structure of NPN transistor. The depletion region of E-B junction consists of +ve ions in emitter side and –ve ions in base side. Similarly, the depletion region of C-B junction consists of +ve ions in collector side and –ve ions in base side.

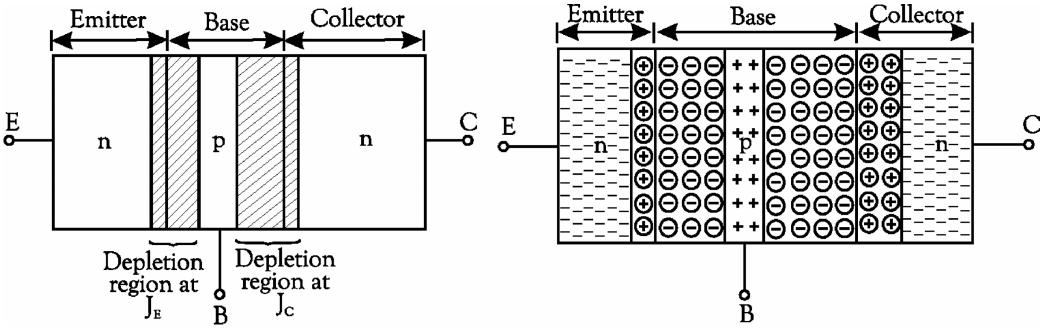


Figure 2.2 *Detailed structure of un-biased NPN transistor*

2.1.3 Structure of PNP Transistor

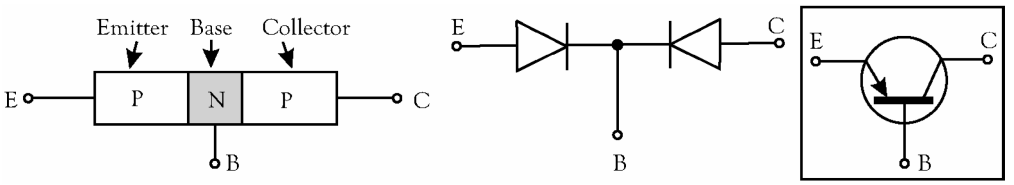


Figure 2.3 *(a) Shows the structure of the PNP transistor, (b) Diode equivalent and (c) Its symbol*

Fig. 2.4, shows the internal structure of PNP transistor. The depletion region of E-B junction consists of -ve ions in emitter side and +ve ions in base side. Similarly, the depletion region of C-B junction consists of -ve ions in collector side and +ve ions in base side.

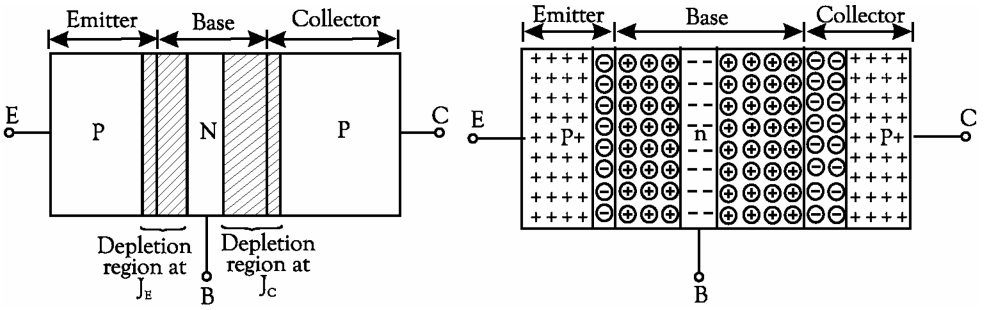


Figure 2.4 *Detailed structure of un-biased PNP transistor*

2.1.4 Transistor Configurations

A Bipolar Junction Transistor has three terminals; emitter, base and collector. If it is to operate in a circuit, four terminals are required, two terminals for input signal and two terminals for output signal. Usually, one of the terminals is made common to both input and output. Accordingly, following three configurations are possible.

(i) Common Base *(CB)* configuration

(ii) Common Emitter *(CE)* configuration

(iii) Common Collector *(CC)* configuration

These configurations, using an NPN transistor, are given in Fig. 2.5. It is noted that the common terminal is always grounded.

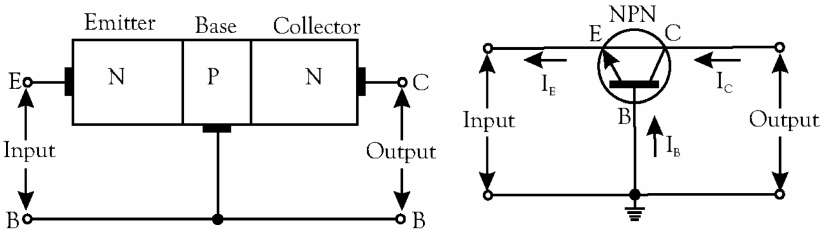


Figure 2.5 (a) *Common Base Configuration*

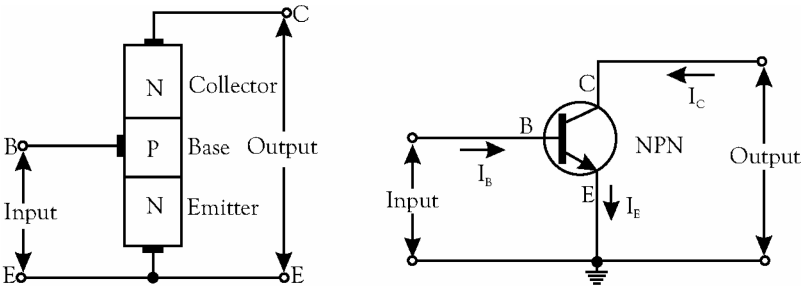


Figure 2.5 (b) *Common Emitter Configuration*

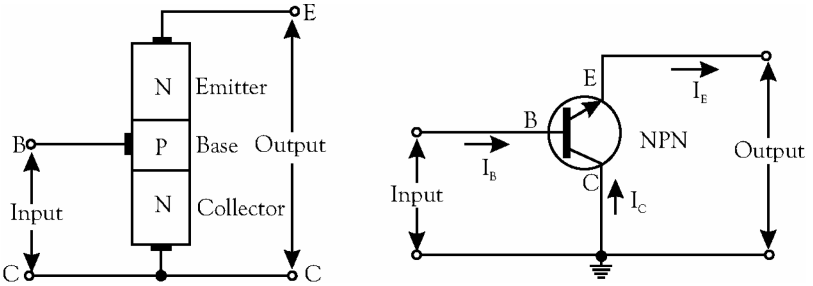


Figure 2.5 (c) *Common collector configuration*

2.1.5 Principle of Operation of NPN Transistor

For proper operation of a transistor, the essential conditions are :

(1) Emitter – Base Junction should be forward biased and

(2) Collector – Base Junction should be reverse biased.

Fig. 2.6. shows the NPN transistor with forward bias to emitter-base junction and reverse bias to collector-base junction. The forward bias causes the electrons in the N-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the P-type base, they tend

to combine with holes. As the base is lightly doped and very thin, only a few electrons (less than 2%) combine with holes to constitute base current I_B. The remainder (more than 98%) cross over into the collector region to constitute collector current I_C. In this way almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base currents, i.e., $I_E = I_B + I_C$.

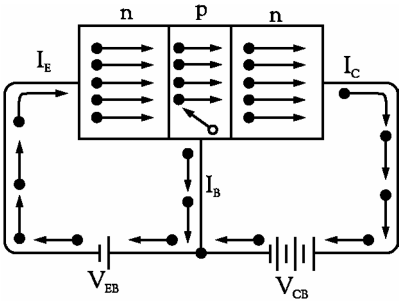


Figure 2.6 *Operation of NPN transistor*

2.1.6 Principle of Operation of PNP Transistor

Fig. 2.7 shows the basic connection of PNP transistor. The forward bias causes the holes in the P-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes cross into n-type base, they tend to combine with the electrons. As the base is lightly doped and very thin, only few holes (less than 2%), combine with the electrons. The remainder (more than 98%) cross into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It may be noted that current conduction within PNP transistor is by holes. However, in the external connecting wires, the current is still by electrons.

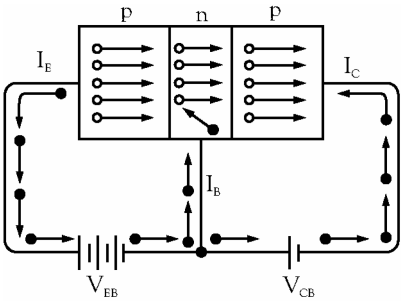


Figure 2.7 *Operation of PNP transistor*

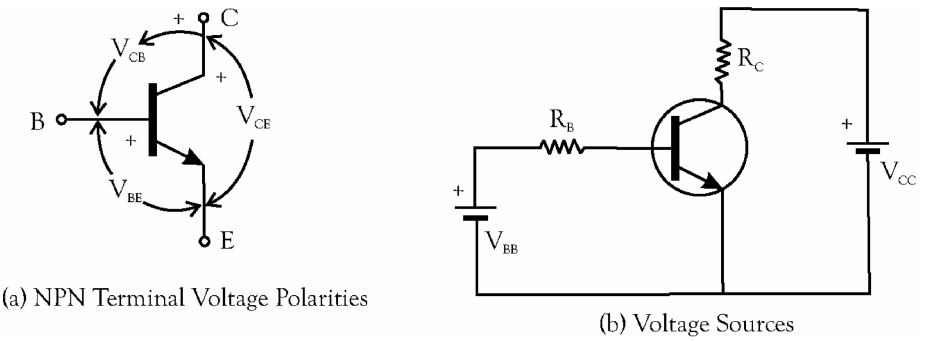
2.1.7 Why NPN Transistor is Commonly Used?

NPN transistor is commonly used in electronic circuits for following reasons :

1. NPN transistor has electrons as majority charge carriers which moves in conduction band due to applied potential difference. PNP transistor has holes as majority charge carriers which moves in valance band due to applied potential difference. As a result, NPN transistors are faster in switching than PNP transistors.
2. NPN transistor, when used as an amplifier, needs positive DC supply for collector terminal where as PNP transistor, when used as an amplifier needs negative DC supply for collector terminal.

2.2 TRANSISTOR VOLTAGES AND CURRENTS

2.2.1 Transistor Voltages



(a) NPN Terminal Voltage Polarities

(b) Voltage Sources

Figure 2.8 *Voltage in NPN transistor*

In an NPN transistor, the base is biased to a higher positive voltage than the emitter, and, in turn, the collector is at a higher potential than the base. Fig. 2.8(a) gives the polarities of the terminal voltages. The direction of the arrow head indicates the transistor bias polarities as also the conventional current direction.

Fig. 2.8(b) shows the voltage source connections. The base bias voltage (V_{BB}) is applied through base resistor R_B, and the supply voltage (V_{CC}) is applied through R_C. The negative terminals of V_{CC} & V_{BB} are connected at the transistor emitter terminal. In order to ensure that the CB junction remains reverse-biased, V_{CC} is always much larger than V_{BB}, then the collector (N-side) is positive and the base (P-side) is negative.

Typical base-emitter voltages are 0.7 V for a silicon transistor and 0.3 V for a germanium transistor. Usually collector voltages are of in the range between 3 V and 20 V, but in some cases they may exceed 20 V.

In a PNP transistor the base is made more negative than the emitter (Fig.2.9(a)). The arrowhead pointing inwards from the emitter (positive) to the base (negative), and the collector is made more negative than the base.

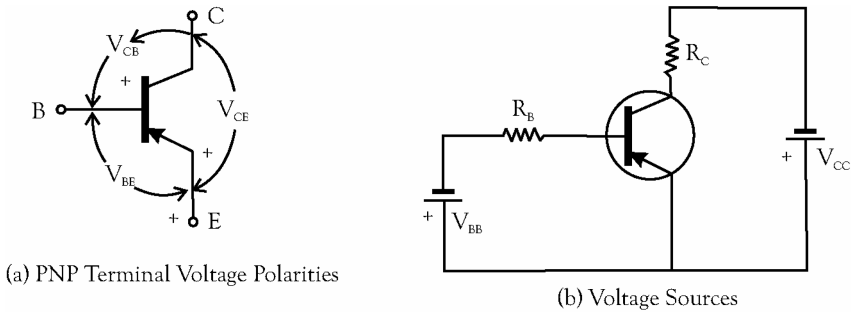


Figure 2.9 *Voltage in PNP transistor*

Fig. 2.9 (b) gives the circuit which shows the two voltage sources connected through resistors. The positive terminals of V_{CC} and V_{BB} are connected at the emitter. With V_{CC} larger than V_{BB} the P-type collector is more negative than the N-type base, ensuring that the C-B junction is reverse-biased.

All transistors (both NPN & PNP) are usually operated by forward biasing the B-E junction and reverse-biasing the C-B junction.

2.2.2 Transistor Currents

(1) Current Gain of a Transistor in Common-Base Configuration

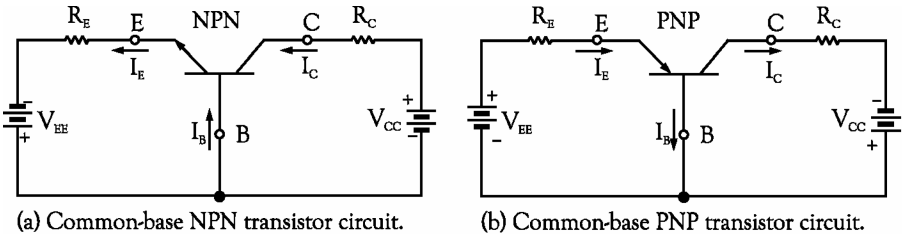


Figure 2.10 *Common base configuration*

Consider a transistor (either NPN or PNP) in a common-base configuration as shown in Fig. 2.10 (a) or (b). Here the emitter current is the input current and collector current is the output current. *The ratio of the transistor output current to the input current is called current gain of a transistor.* Since the input current and output current may be either direct current or alternating current, we define two types of current gains namely d.c. current gain and a.c. current gain.

(a) Common-base d.c. current gain (α): It is defined as the ratio of collector current I_C to emitter current I_E and is usually designated by α, or α_{dc} or h_{FB}, Mathematically, the common-base d.c. current gain is expressed as,

$$\alpha = I_C/I_E \qquad ...(2.1)$$

We know that in a transistor, the collector current is always less than the emitter current.

Therefore current-gain of a transistor in common-base configuration is always less than unity. For example, if $I_C = 9.7$ mA and $I_E = 10$ mA, then common-base d.c. current gain,

$$\alpha = 9.7/10 = 0.97$$

(b) Common-base a.c. current gain (α_0): It is defined as the ratio of small change in collector current (ΔI_C) to a small change in emitter current (ΔI_E) for a constant collector-to-base voltage (V_{CB}). It is designated by α_0, or α_{ac} or h_{fb}. Mathematically, the common-base a.c. current gain.

$$\alpha_0 = \Delta I_C / \Delta I_E \qquad ...(2.2)$$

The term α_0 is also called common-base short-circuit current gain or small signal current gain.

It may be noted that current gain of a transistor in a common-base configuration (α) is less than unity. But still it is called current gain. It is due to the fact that the output resistance of a common-base transistor is much higher than the input resistance. This produces a large voltage gain and hence the large power gain.

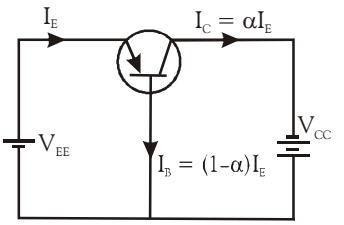


Figure 2.10 *(c) Base and collector currents in terms of emitter current*

Now,

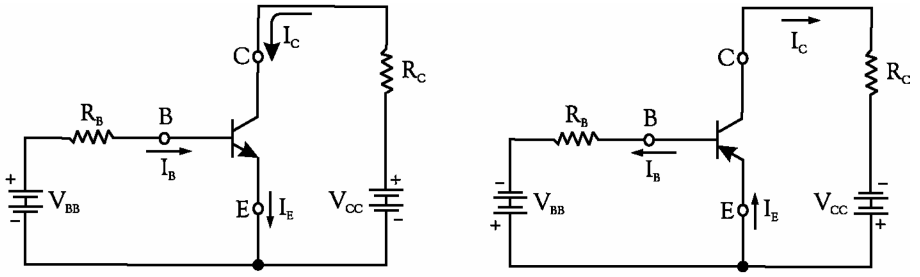
$I_C = \alpha I_E$

$I_B = I_E - I_C = I_E - \alpha I_E$

$I_B = (1 - \alpha) I_E$

This is shown in Fig. 2.10 (c). ...(2.3)

(2) Current Gain of Transistor in Common-Emitter Configuration



(a) Common-emitter NPN transistor circuit. (b) Common-emitter PNP transistor circuit.

Figure 2.11 *Common emitter configuration*

Consider a transistor (either NPN or PNP) connected in a common-emitter configuration as shown in Fig. 2.11 (a) and (b). Here, the base current is the input current and the collector current is the output current. The ratio of collector current to base current is called current gain (β) of the transistor. Since the base current and collector current may be direct or alternating current, therefore we define

two types of current gains namely d.c. current gain and a.c. current gain.

(a) Common-emitter d.c. current gain (β): It is defined as the ratio of collector current (I_C) to corresponding base current (I_B) and is designated by β, or β_{dc} or h_{FE}. Mathematically, the common-emitter d.c. current gain is given by the relation,

$$\beta = I_C/I_B \qquad ...(2.4)$$

or $$I_C = \beta I_B$$

Since collector current of a transistor is much larger than the base current, the value of β is much greater than unity. Typical values of β may range from 20 to 250. It is also called common-emitter dc forward transfer ratio and is written as h_{FE}. It is possible for β to have as high a value as 500.

(b) Common emitter a.c. current gain (β_0): It is defined as the ratio of small change in collector current (ΔI_C) to the corresponding small change in base current (ΔI_B) for a constant collector-to-emitter voltage (V_{CE}). It is designated by β_0 or β_{ac} or h_{fe}. Mathematically common-emitter a.c. current gain is given by the relation,

$$\beta_0 = \Delta I_C/ \Delta I_B \qquad ... (2.5)$$

The term β_0 is also called common-emitter short circuit current gain or small-signal common-emitter current gain. It is interesting to know that β_0 or h_{fe} is a parameter used in the analysis of small-signal transistor amplifier circuits. β_0 have a range of values similar to that mentioned for β. For all practical purposes, d.c. current gain and a.c. current gain are considered to be equal. *i.e.* $\beta = \beta_0$.

Relationship between α and β:

We know that emitter current (I_E) of a transistor is the sum of its base current (I_B) and collector current (I_C). i.e.,

$$I_E = I_B + I_C$$

Dividing the above equation on both sides by I_C,

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

Since $$\frac{I_E}{I_C} = \alpha \; and \; \frac{I_B}{I_C} = \beta \text{ then } \frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta}$$

$\therefore$ $$\alpha = \frac{\beta}{\beta + 1} \qquad ...(2.6)$$

The above expression may be written as

$$\alpha (\beta + 1) = \beta$$

$$\alpha . \beta + \alpha = \beta$$

$$\alpha = \beta - \alpha . \beta = \beta(1-\alpha)$$

or
$$\beta = \frac{\alpha}{1 - \alpha} \quad \text{...(2.7)}$$

Also using above eqns., we can deduce:

(i) $I_C = \beta I_B = \alpha I_E = \frac{\beta}{1 + \beta} \cdot I_E$

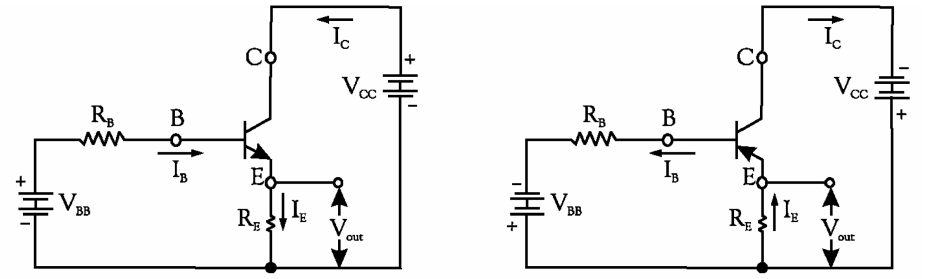
(ii) $I_B = \frac{I_C}{\beta} = \frac{I_E}{1 + \beta} = (1 - \alpha) I_E$

(iii) $I_E = \frac{I_C}{\alpha} = \frac{1 + \beta}{\beta} . I_C = (1 + \beta) I_B = \frac{I_B}{(1 - \alpha)}$

(iv) The three transistor dc currents always bear the following ratio

$I_E : I_B : I_C :: 1 : (1 - \alpha) : \alpha$

(3) Current Gain of a Transistor in Common-Collector Configuration:



(a) Common-collector NPN transistor circuit. (b) Common-collector PNP transistor circuit.

Figure 2.12 *Common collector configuration*

Fig. 2.12 (a) and (b) show a NPN and PNP transistor connected in a common-collector configuration respectively. The voltages V_{BB} forward-biases the emitter-base junction, and V_{CC} reverse-biases the collector-base junction of the transistor. Here, the collector is not at d.c. ground. But it is at a.c. ground. It is due to the fact, that the voltage of d.c. supply source (V_{CC}) has zero resistance to an a.c. signal. An external resistor R_E is connected from the emitter to ground. The output of the circuit is taken across the resistor R_E.

It may be noted that in a common-collector transistor circuit, the input current is the base current (I_B) and the output current is the emitter current (I_E). Therefore, common-collector current gain is given

by the relation,

$$\gamma = \frac{I_E}{I_B} = \frac{I_E}{I_C} \times \frac{I_C}{I_B} = \frac{1}{\alpha} \times \beta$$

Substituting the value of $\alpha = \beta / (1 + \beta)$ in the above equation, common-collector current gain (γ) becomes

$$\gamma = \frac{\beta}{\beta / (1+\beta)} = 1 + \beta \qquad ...(2.8)$$

It means that the output current of a common-collector transistor circuit is $(1 + \beta)$ times that of the input current. We know that $\beta >> 1$, therefore common-collector current gain $\gamma \approx \beta$.

(4) Leakage current in CB Transistor

Consider the CB transistor circuit shown in Fig. 2.13. The emitter current (due to majority carriers) initiated by the forward-biased emitter-base junction is split into two parts:

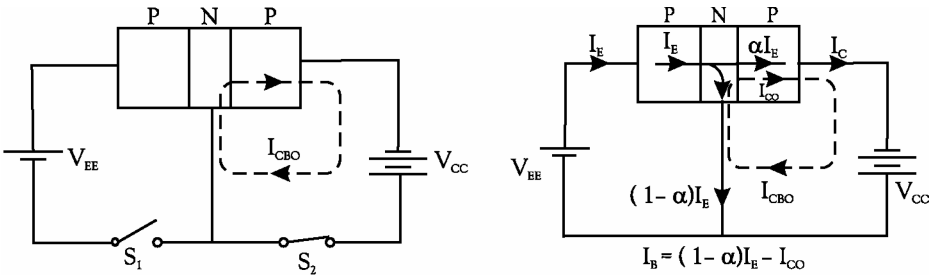


Figure 2.13 *Leakage current in CB configuration (a) Grounded emitter, (b) Current distribution*

(i) $(1 - \alpha)I_E$ which becomes base current I_B in the external circuit, and

(ii) αI_E which becomes collector current I_C in the external circuit.

Though C–B junction is reverse-biased for majority charge carriers (i.e., holes in this case), it is forward-biased for thermally-generated minority charge carriers (i.e., electrons in this case) are concerned. This current flows even when emitter is disconnected from its dc supply as shown in Fig. 2.13 (a) where switch S_1 is open. It flows in the same direction as the collector current of majority carriers. It is called leakage current I_{CBO}. The subscripts CBO stand for current from Collector to Base with emitter Open. Very often, it is simply written as I_{CO}.

It should be noted

(i) I_{CBO} is exactly like the reverse saturation current I_{RS} or I_O of a reverse-biased diode.

(ii) I_{CBO} is extremely temperature-dependent because it is made up of thermally-generated minority charge carriers. I_{CBO} doubles for every 10°C rise in temperature for Si and 6°C for G_e.

It is seen that total collector current is actually the sum of two components:

(i) current produced by normal transistor action i.e., component controlled by emitter current. Its value is αI_E and is due to majority carriers.

(ii) temperature-dependent leakage I_{co} due to minority carriers

$$\therefore \quad I_C = \alpha I_E + I_{CO} \qquad \text{...(2.9)}$$

$$\therefore \quad \alpha = \frac{I_C - I_{CO}}{I_E}$$

Since $I_{CO} \ll I_C$ *hence* $\alpha \cong \dfrac{I_C}{I_E}$

(iii) Substituting the value of $I_E = (I_C + I_B)$ in Eqn. (2.9) above, we get

$$I_C = \alpha(I_C + I_B) + I_{CO} \quad \text{or} \quad I_C(1 - \alpha) = \alpha I_B + I_{CO}$$

$$\therefore \quad I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CO}}{1 - \alpha}$$

(iv) Eliminating I_C from Eqn. (2.9) above, we get

$$(I_E - I_B) = \alpha I_E + I_{CO}$$

Rearranging the above equation, we get

$$I_B = (1 - \alpha) I_E - I_{CO} \qquad \text{...(2.10)}$$

(5) Leakage current in CE Transistor

Fig. 2.14 (a) shows a grounded-emitter circuit of an NPN transistor whose base lead is open. It is found that despite $I_B = 0$, there is a leakage current from collector to emitter. It is called I_{CEO}, the subscripts CEO standing for 'Collector to Emitter with base Open'.

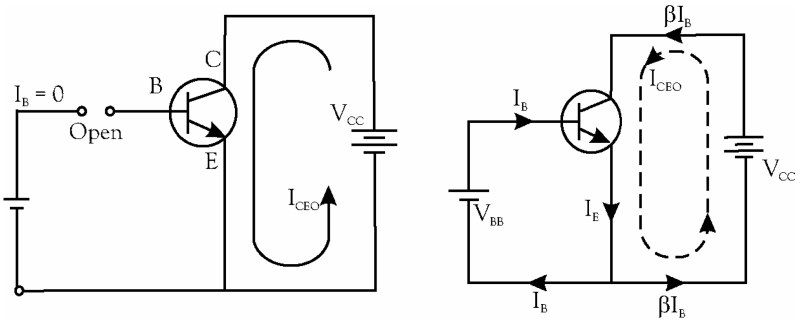


Figure 2.14 *(a) Grounded-emitter circuit of an NPN transistor, (b) Current distribution in CE circuit*

Taking this leakage current into account, the current distribution through a *CE* circuit becomes as shown in Fig. 2.14 (b).

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1+\beta) I_{CO} = \beta I_B + \frac{I_{CO}}{(1-\alpha)} \quad \text{...(2.11)}$$

$$\therefore \quad I_C = \frac{\alpha I_B}{1-\alpha} + \frac{\alpha I_{CO}}{1-\alpha} \quad \text{...(2.12)}$$

Now, $\beta I_B = \alpha I_E$, Substituting this value in above Eqn. (2.11), we get

$$I_C = \alpha I_E + I_{CEO} \quad \text{...(2.13)}$$

But we know that $I_B = I_E - I_C$

Substituting the value of I_C from above, we have

$$I_B = I_E - \alpha I_E - I_{CEO} = (1-\alpha) I_E - I_{CEO} \quad \text{...(2.14)}$$

(6) Thermal Runaway:

In a *CE* circuit, using Eqn. (2.11), we know that

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

The leakage current is extremely temperature-dependent. It almost doubles for every 6°C rise in temperature in Ge and for every 10°C rise in S_i. Any increase in I_{CO} is magnified $(1 + \beta)$ times *i.e.,* 200 to 300 times. Even a slight increase in I_{CO} will affect I_C considerably. As I_C increases, collector power dissipation increases which raises the operating temperature that leads to further increase in I_C. If this succession of increases is allowed to continue, soon I_C will increase beyond safe operating value thereby damaging the transistor itself — a condition known as *thermal runaway.* Hence, some form of stabilization is necessary to prevent this thermal runaway.

2.3 AMPLIFICATION

2.3.1 Transistor as an Amplifier

A transistor increases the strength of a weak signal and thus acts as an amplifier. Fig. 2.15 shows the basic circuit of a transistor amplifier. The weak input signal is applied between emitter-base junction and amplified output is taken across the load R_C connected in the collector circuit. In order to achieve faithful amplification, the input circuit should always remain forward biased. To do so, a d.c. voltage V_{BB} is applied in the input circuit in addition to the signal as shown. This d.c. voltage is known as bias voltage and its magnitude is such that it always keeps the input circuit forward biased regardless of the polarity of the ac signal.

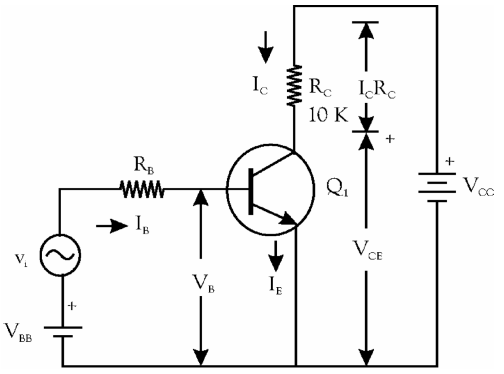


Figure 2.15 *Transistor as an amplifier*

As the input circuit has low resistance, a small change in signal voltage causes an appreciable change in emitter current. This causes almost the same change in collector current due to transistor action. The collector current flows through high load resistance R_C produces a large voltage across it. Thus a weak signal applied in the input circuit appears in the amplified form in the collector circuit. In this way a transistor acts like an amplifier.

2.4 COMMON BASE CHARACTERISTICS

Transistor characteristics represent relationship between different dc currents and voltages of a transistor. The three important characteristics called static characteristics of a transistor are :

1. Input characteristic
2. Output characteristic
3. Constant-current transfer characteristic.

The static characteristics of an NPN transistor connected in common-base configuration can be determined by using circuit as shown in Fig. 2.16. Milliammeters are included in series with the emitter and collector circuits to measure I_E and I_C. Similarly, voltmeters are connected across E and B to measure voltage V_{BE} and across C and B to measure V_{CB}. The two potentiometer resistors R_1 and R_2 supply variable voltage from the collector and emitter dc supplies.

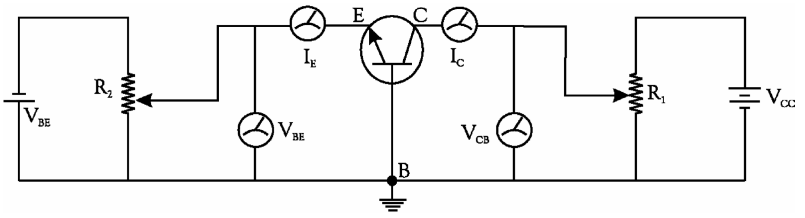


Figure 2.16 *Circuit diagram for static characteristics of CB configuration*

2.4.1 Input Characteristics

It is a graph between I_E and V_{BE} when voltage V_{CB} is kept constant. The method of determining this characteristic is as follows:

(1) Voltage V_{CB} is adjusted to a suitable value with the help of R_1 (Fig. 2.16).

(2) Voltage V_{BE} is increased in steps and corresponding values of I_E are noted from the milliammeter.

(3) Plot I_E verses V_{BE}. We get the input characteristics as shown in Fig. 2.17 one for Ge transistor and the other for Si transistor. Both curves are exactly similar to the forward characteristic of a P-N diode.

This characteristic may be used to find the input resistance of the transistor. Its value is given by the reciprocal of its slope.

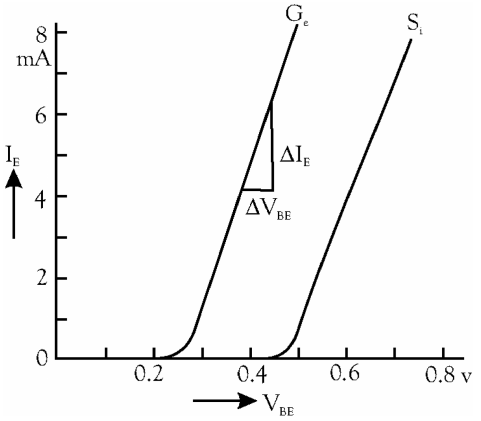


Figure 2.17 *Input characteristics of transistor in CB configuration*

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_E} \qquad \text{when } V_{CB} \text{ is constant}$$

This characteristic is hardly affected by changes either in V_{CB} or temperature.

2.4.2 Output Characteristics

It is a graph between I_C and V_{CB} when I_E is kept constant. The method of determining this characteristic is as follows:

(1) Emitter current I_E is kept suitable constant value by adjusting R_2.

(2) V_{CB} is increased from zero in a number of steps and the corresponding collector current I_C that flows is noted.

(3) Next, V_{CB} is reduced back to zero, I_E is increased to a value a little higher than before and the whole procedure is repeated. In this way, whole family of curves is obtained, A typical family of such curves is shown in Fig. 2.18.

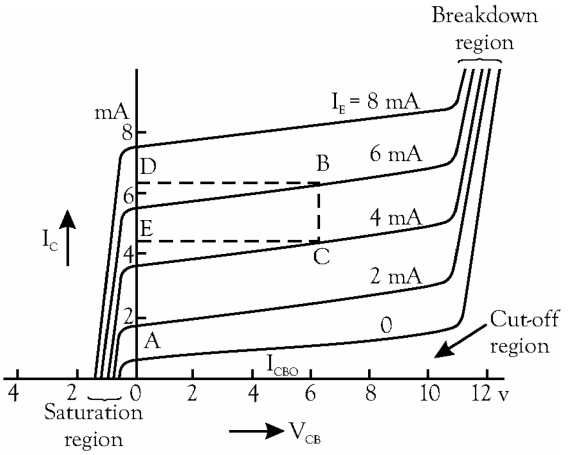


Figure 2.18 *Output characteristics of transistor in CB configuration*

From the output characteristic curve shown in Fig. 2.18, we can conclude that:

(1) The ac current gain, α_{ac} of the transistor is expressed as:

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} = \frac{DE}{BC} = \frac{(6.2 - 4.3)\,mA}{2mA} = 0.95$$

(2) I_C is practically independent of V_{CB} over the working range (active region) of the transistor, yet if V_{CB} is permitted to increase beyond a certain value, I_C eventually increases rapidly due to avalanche breakdown as shown.

(3) It is seen that I_C flows even when $V_{CB} = 0$. It is due to the fact that electrons are being injected into the base under the action of forward-biased E/B junction and are being collected by the collector due the action of the internal junction voltage at the C/B junction.

(4) A small amount of collector current flows even when emitter current $I_E = 0$, due to collector leakage current I_{CBO}.

(5) The output resistance (R_O) of the Transistor in CB configuration is very high due to horizontal nature of the graph in active region.

2.4.3 Current Transfer Characteristic

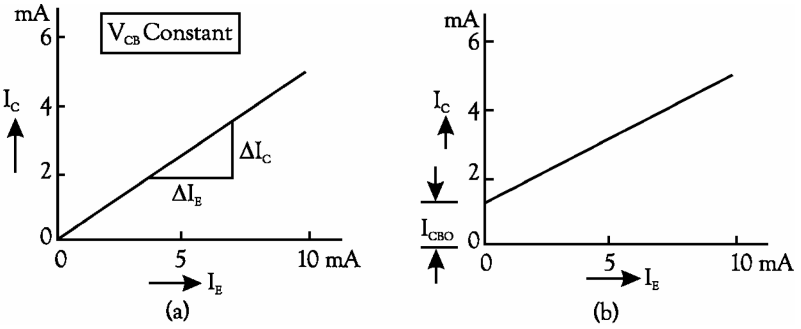


Figure 2.19 *Current transfer characteristics of CB configuration*

It shows how I_C varies with changes in I_E when V_{CB} is kept constant. For drawing this characteristic, first V_{CB} is set to a convenient value and then I_E is increased in steps and corresponding values of I_C is noted. A typical transfer characteristic is shown in Fig. 2.19 (a). Fig. 2.19 (b) shows a more detailed view of the portion near the origin.

It may be noted that CB connection is rarely used for audio-frequency circuits because (i) its current gain is less than unity and (ii) its input and output resistances are not suitable.

2.5 COMMON EMITTER CHARACTERISTICS

The static characteristics of an NPN transistor connected in common-Emitter configuration can be determined by using circuit as shown in Fig. 2.20. Milliammeters are included in series with the base and collector circuits to measure I_B and I_C. Similarly, voltmeters are connected across B and E to measure voltage V_{BE} and across C and E to measure V_{CE}. The two potentiometer resistors R_1 and R_2 supply variable voltage from the collector and base d.c. supplies.

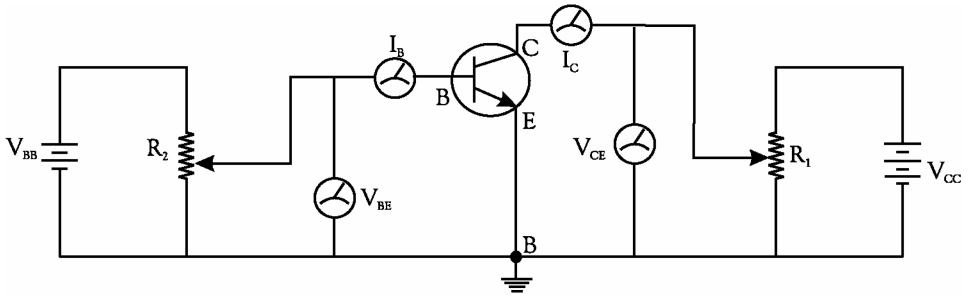


Figure 2.20 *Circuit diagram for static characteristics of CE configuration*

2.5.1 Input Characteristics

It is a graph between I_B and V_{BE} when V_{CE} is kept constant. The method of determining this characteristic is as follows:

(1) V_{CE} is maintained constant at a convenient value and then V_{BE} is increased in steps. Corresponding values of I_B are noted at each step.

(2) The procedure is then repeated for a different but constant value of V_{CE}.

A typical input characteristic is shown in Fig. 2.21. Like CB connection, the overall shape resembles the forward characteristic of a *P-N* diode. The reciprocal of the slope gives the input resistance R_{in} of the transistor.

$$R_{in} = \frac{1}{\frac{\Delta I_B}{\Delta V_{BE}}} = \frac{\Delta V_{BE}}{\Delta I_B}$$

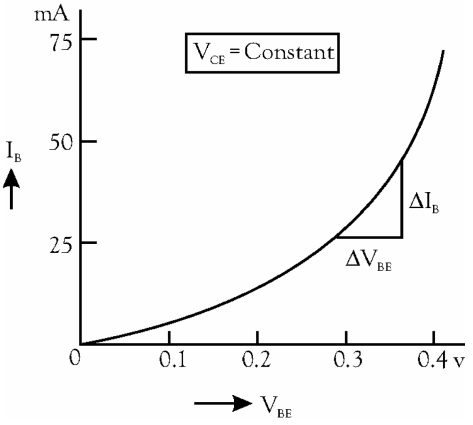


Figure 2. 21 *Input characteristics of transistor in CE configuration*

2.5.2 Output Characteristics

It is a graph between I_C and V_{CE} when I_B is kept constant. The method of determining this characteristic is as follows:

(1) I_B is set to a convenient value and maintained constant and then V_{CE} is increased from zero in steps and corresponding I_C is noted at each step.

(2) Next, V_{CE} is reduced to zero and I_B increased to another convenient value and the whole procedure is repeated. In this way, a family of output characteristic curves (Fig. 2.22) is obtained.

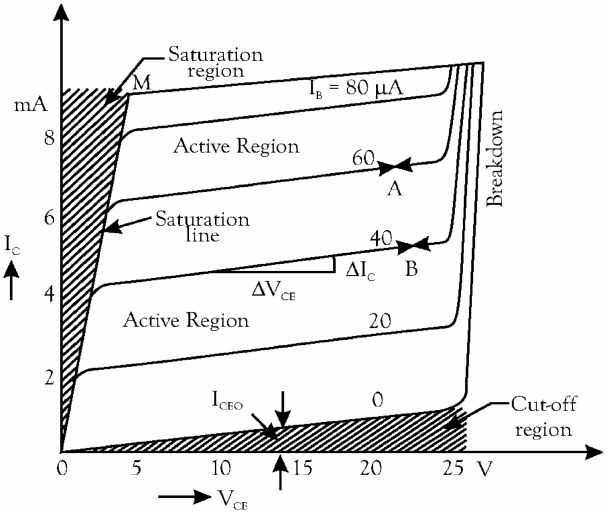


Figure 2. 22 *Output characteristics of transistor in CB configuration*

From the output characteristic curve shown in Fig. 2.22, we can conclude that:

1. As V_{CE} increases from zero, I_C rapidly increases to a near saturation level for fixed value of I_B.
2. As shown, a small amount of collector current flows even when $I_B = 0$. It is called I_{CEO}. Since main collector current is zero, the transistor is said to be cut-off.
3. If V_{CE} is allowed to increase too far, C–B junction completely breaks down and due to this avalanche breakdown, I_C increases rapidly and may cause damage to the transistor.
4. When V_{CE} has very low value (ideally zero), the transistor is said to be saturated and it operates in the saturation region of the characteristic. Here, change in I_B does not produce a corresponding change in I_C.
5. The transistor can be operated in active region when base-emitter junction is forward biased and collector-base junction is reverse biased.
6. The transistor can be operated in saturation region when both base-emitter junction and Collector-base junctions are forward biased.
7. The transistor can be operated in cut-off region when both base-emitter junction and Collector-base junctions are reverse biased.

This characteristic can be used to find β at a specific value of I_B and V_{CE}

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

The value of output resistance R_{out} ($= \Delta V_{CE}/\Delta I_C$) over the near horizontal part of the characteristic varies from 10 KΩ to 50 KΩ.

2.5.3 Current Transfer Characteristic

It indicates how I_C varies with changes in I_B when V_{CE} is kept constant at a given value. Such a typical characteristic is shown in Fig. 2.23 (a). Its slope gives

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

From Fig. 2.23 (b), it is seen that a small collector current flows even when $I_B = 0$. It is the common-emitter leakage current $I_{CEO} = (1 + \beta)/I_{CO}$. Like I_{CO}, it is also due to the flow of minority carriers across the reverse-biased C–B junction.

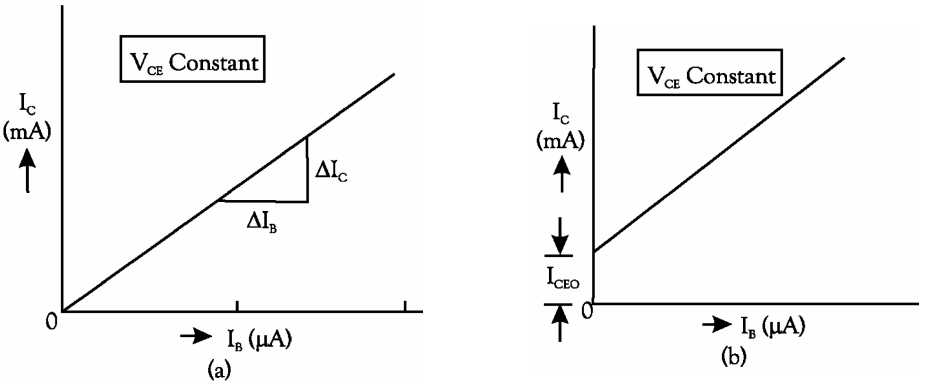


Figure 2.23 *Current transfer characteristics of CE configuration*

2.5.4 Why CE configuration is commonly used?

The common Emitter configuration is commonly used because:

(1) CE configuration is only configuration which provides both voltage gain and current gain greater than unity. Thus the power gain is maximum compared to CB & CC configurations.

(2) In CE configuration, the ratio of output resistance to input resistance is small (of 10Ω -100Ω). This makes CE configuration ideal for coupling between various transistor stages. However, in CB & CC connections, the ratio of output resistance to input resistance is very large so that coupling between stages is inefficient due to large mismatch of resistance.

2.6 COMMON COLLECTOR CHARACTERISTICS

The static characteristics of an NPN transistor connected in common-Collector configuration can be determined by using circuit as shown in Fig. 2.24. Ammeters are included in series with the base and

emitter circuits to measure I_B and I_E. Similarly, voltmeters are connected across B and C to measure voltage V_{CB} and across E and C to measure V_{CE}. The two variable dc supplies are used for biasing. The collector terminal is common to both the input (CB) and output (CE) circuits.

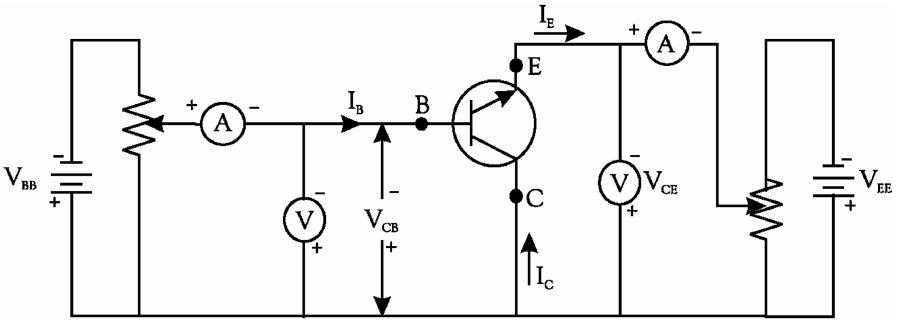


Figure 2. 24 *Circuit diagram for static characteristics of CC configuration*

2.6.1 Input Characteristics

It is a graph of input base current I_B versus input voltage V_{CB}, when V_{CE} is constant.

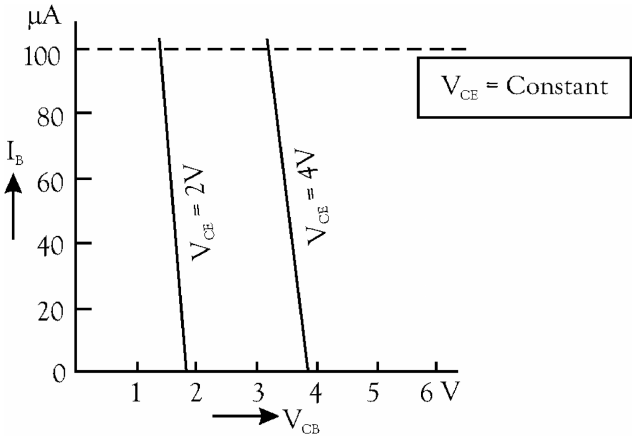


Figure 2.25 *Input characteristics of CC configuration*

From the Fig. 2. 24, we can write as $V_{CB} = V_{CE} - V_{BE}$. Moreover, as V_{CB} is increased, V_{BE} is reduced thereby reducing I_B which is shown in Fig. 2.25. It is also found that as V_{CB} increases, I_B is decreased.

2.6.2 Output Characteristics

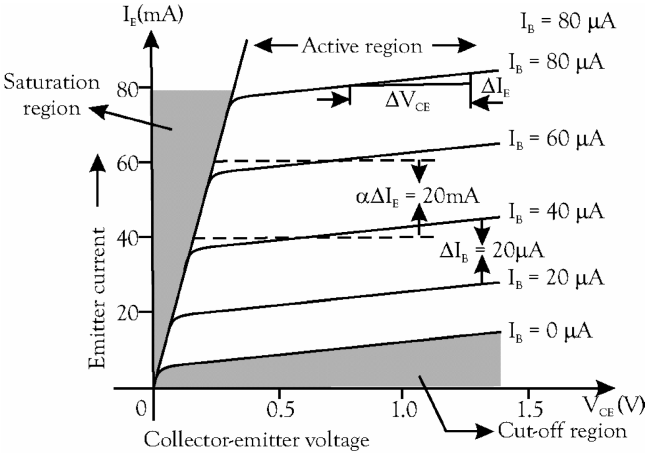


Figure 2.26 *Output characteristics of CC configuration*

The output characteristics is a graph between I_E and V_{CE} for several fixed values of I_B as shown in Fig.2.26. Since $I_C \cong I_E$, this characteristic is practically identical to that of the CE circuit.

2.6.3 Current Transfer Characteristic

It indicates how I_E varies with changes in I_B when V_{EC} is kept constant at a given value. Such a typical characteristic is shown in Fig. 2.27. The current gain of the transistor in CC configuration is:

$$\gamma = \frac{I_E}{I_B}$$

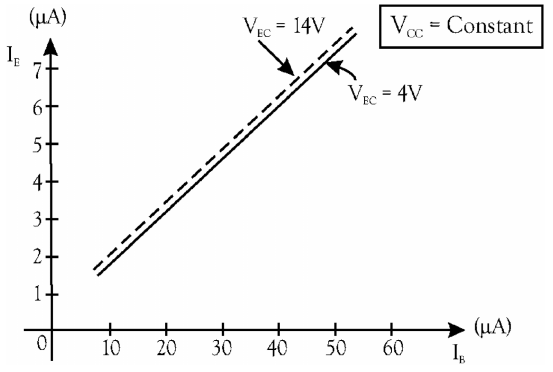


Figure 2. 27 *Current transfer characteristics of CC configaration*

2.6.4 Comparison of Transistor Configurations

Sr. No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1KΩ)	High (500 KΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 KΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output cufrrent	I_C	I_C	I_E
5.	Input votage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Less than unity
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

2.7 DC LOAD LINE & BIAS POINT

2.7.1 DC Load Line

For drawing the dc load line of a transistor, one need to know only its cut-off and saturation points.

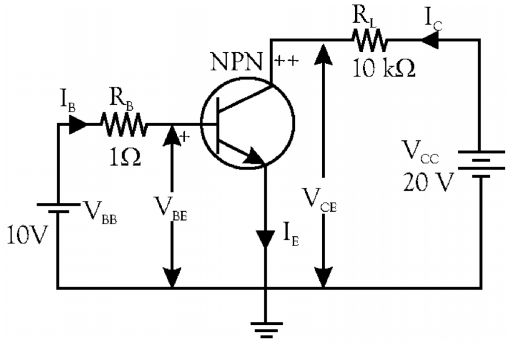


Figure 2.28 *CE circuit using NPN transistor*

DC load line of a transistor is a straight line joining cut-off & saturation points. For the CE circuit as shown in Fig. 2.28, the load line is drawn in Fig. 2.29. A is the cut-off point and B is the saturation point. The voltage equation of the collector-emitter is

$$V_{CC} = I_C R_L + V_{CE} \qquad \therefore \quad I_C = \frac{V_{CC}}{R_L} - \frac{V_{CE}}{R_L}$$

Consider the following two particular cases:

(i) when $I_C = 0$, $V_{CE} = V_{CC}$
— Cut-off point A

(ii) when $V_{CE} = 0$, $I_C = V_{CC} / R_L$
— saturation point B ...(2.15)

The dc load line can be drawn if only V_{CC} and R_L are known. Slope of the load line AB $= -1/R_L$.

2.7.2 Active Region

All operating points (like C, D, E etc., in Fig. 2.29) lying between cut-off and saturation points form the active region of the transistor. In this region, E-B junction is forward-biased and C-B junction is reverse biased - which are the conditions necessary for the proper operation of a transistor (Table 2.1).

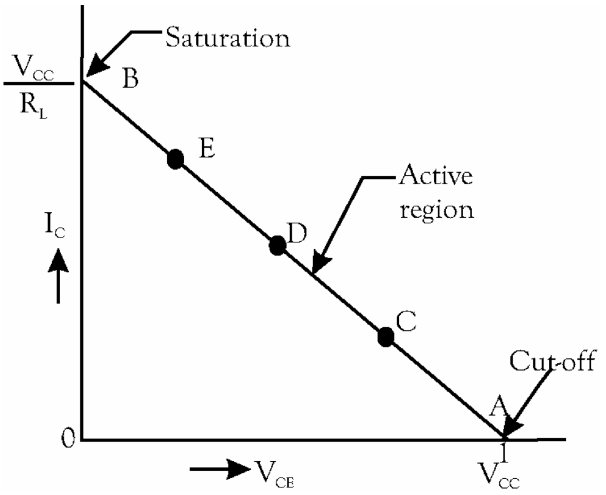


Figure 2.29 *DC load line and active region*

Table 2.1 Operating regions and biasing conditions

Region fo Operation	Emitter Base Junction	Collector Base Junction
Cut-off	Reverse biased	Reverse biased
Active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased

2.7.3 Bias Point (Q-Point)

It is a point on the dc load line, which represents the values of I_C and V_{CE} that exist in a transistor circuit when no input signal is applied. It is also known as the dc operating point or working point. The best position for this point is mid-way between cut-off and saturation points where $V_{CE} = ½ V_{CC}$ (like point D in Fig. 2.29). There are three cases for positioning Q-point:

(1) If the Q point is fixed near saturation point of the d.c. load line, then, during the negative half-cycle of the input signal, the transistor is driven into saturation. As a result, the negative peak of the input signal is clipped at output as shown in Fig. 2.30.

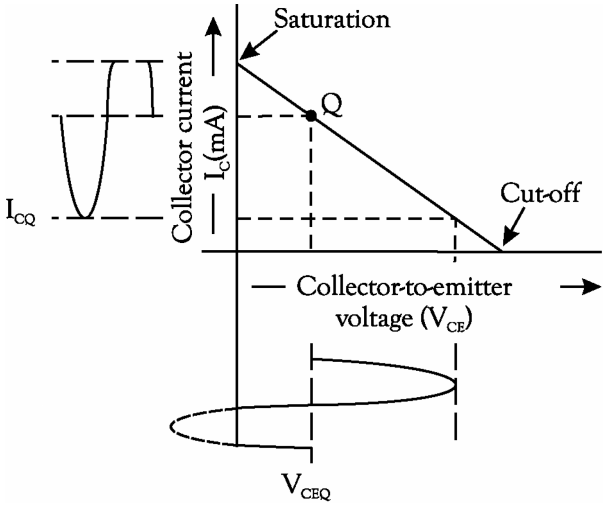


Figure 2.30 *Q point is fixed near saturation point of the d.c. load line*

(2) If the Q point is fixed near cut-off point of the d.c. load line, then, during the positive half-cycle of the input signal, the transistor is driven into cut-off. As a result, the negative peak of the input signal is clipped at output as shown in Fig. 2.31.

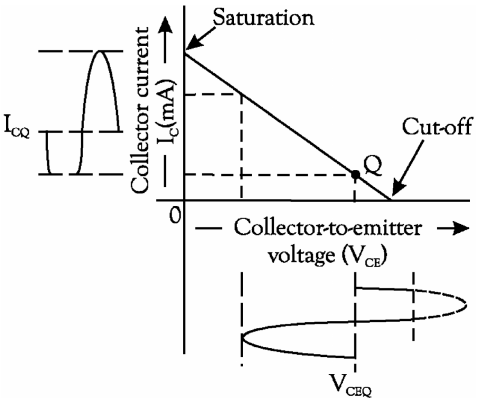


Figure 2.31 *Q point is fixed near cut-off point of the d.c. load line*

(3) On other hand, if the Q-point is fixed at the centre of the d.c. load line by proper bias, as shown in Fig. 2. 32, we get undistorted signal at the output.

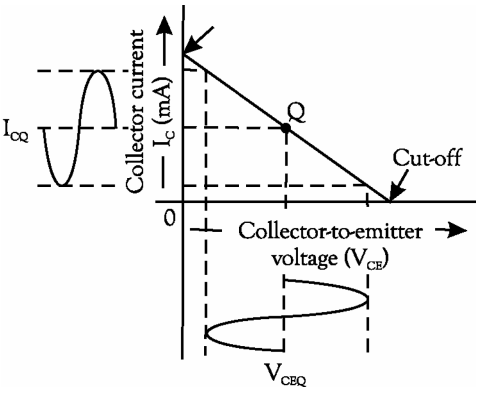


Figure 2.32 *Q point is fixed at the centre of the d.c. load line*

2.7.4 Factors Affecting Stability of Q-Point

It is found that even after the suitable selection of Q-point, it tends to shift from its position. It happens because of the following two reasons :

1. Inherent variations of transistor parameters: We know that the collector current for a common-emitter transistor amplifier is given by the relation,

$$I_C = \beta . I_B + (I + \beta) . I_{CO} \quad \ldots (2.16)$$

In the above equation the variables β, I_B and I_{CO} are found to be strongly dependent upon temperature. As the temperature increases, all the three variables also increase. This results in the increase of collector current and hence causes the operating point to shift towards the saturation point, resulting in clipping and bad distortion of the output. In some cases, a transistor may even burn out due to excessive collector current. But this problem can be solved by designing proper bias stabilization circuits.

2. Variation in parameter values of transistors of the same type: When the transistor is replaced by similar type due to aging, results fluctuation in specified parameters of the transistors provided by the manufacturer in the data sheet. This fluctuation gives rise to instability of the Q-point.

2.7.5 Stability Factor

The stability factor may be defined as the rate of change of collector current (I_C) with respect to the reverse saturation current(I_{CO}) keeping the common-emitter current gain (β) and base current (I_B) as constant. Mathematically, the stability factor is given by the relation,

$$S = \frac{dI_C}{dI_{CO}} \qquad \ldots (2.17)$$

The stability factor is a measure of bias stability of a transistor circuit. A higher value of stability factor indicates poor stability, whereas a lower value indicates good stability. If the rate of change of collector current (dI_C) is equal to the rate of change of reverse saturation current (I_{CO}), then the value of stability factor is unity (one). The unity is the lowest value of stability factor. It may be noted that if the value of stability factor is closer to the unity, the variation of collector current with the temperature will be less. Therefore, there will be less variation in the Q-point.

The stability factor may also be expressed alternatively by using the relationship between base current (I_B), collector current (I_C) and reverse saturation current (I_{CO}). We know that the value of collector current in a transistor is given by the relation,

$$I_C = \beta \, . \, I_B + (1 + \beta) \, I_{CO}$$

Differentiating the above expression with respect to I_C,

$$1 = \frac{d(\beta \, I_B)}{dI_C} + \frac{d(1+\beta) \, I_{CO}}{dI_C}$$

$$= \beta \times \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{CO}}{dI_C} \quad \ldots \text{(Assuming } \beta \text{ as constant)}$$

$$= \beta \times \frac{dI_B}{dI_C} + (1+\beta) \frac{1}{S} \quad \ldots \left(\because \; S = \frac{dI_C}{dI_{CO}} \right)$$

$$S = \frac{1+\beta}{1 - \beta \left(\frac{dI_B}{dI_C} \right)} \qquad \ldots (2.18)$$

The above expression can be used to determine the stability factor (S) of any biasing circuit.

(1) Stability Factor of Common Base Circuit

The collector current of a transistor in common base configuration, is given by the relation,

$$I_C = \alpha \, . \, I_E + I_{CO}$$

Differentiating this equation with respect to I_{CO},

$$\frac{dI_C}{dI_{CO}} = 0 + 1 \qquad \text{or} \qquad S = 1 \qquad \text{... (2.19)}$$

The value of stability factor indicates that the common base circuits are highly stable. Thus there is no need of bias stabilization in these circuits.

(2) Stability Factor of Common Emitter Circuit:

The collector current of a transistor in common emitter configuration is given by the relation,

$$I_C = \beta . I_B + (1 + \beta) I_{CO}$$

Differentiating this equation with respect to I_{CO}

$$\frac{dI_C}{dI_{CO}} = 0 + (1 + \beta) \qquad \text{or} \qquad S = 1 + \beta \qquad \text{... (2.20)}$$

In CE circuit, if $\beta = 100$, then the value of $S = 1 + 100 = 101$. It means that the collector current changes 101 times the change in reverse saturation current. This means that the collector current is highly dependent upon the reverse saturation current and hence upon the temperature. Thus there is a strong need to provide bias stabilization in common emitter circuits to improve the stabilization factor.

SOLVED PROBLEMS

1. *Find I_C, I_E and β_{dc} for a transistor, given that α_{dc} = 0.97 and I_B = 100 μA.*

Solution:

(i) We know that $I_C = (\alpha_{dc} \times I_B) / (1 - \alpha_{dc}) = (0.97 \times 100 \times 10^{-6}) / (1 - 0.97) = 3.23$ mA

(ii) $I_E = I_C / \alpha_{dc} = 3.23 \times 10^{-3} / 0.97 = 3.33$ mA

(iii) $\beta_{dc} = \alpha_{dc} / 1 - \alpha_{dc} = 32.33$

2. *For a certain transistor, α_{dc} = 0.985 and I_{CBO} = 10 μA. If the base current is 120 μA, find the emitter and collector currents.*

Solution:

Given: $\alpha_{dc} = 0.985, I_B = 120\ \mu A, I_{CBO} = 10\ \mu A.$

We know that $$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha} \Rightarrow = \frac{1}{1-\alpha}(\alpha I_B + I_{CBO})$$

$$= \frac{1}{1-0.985}(0.985 \times 120 + 10) = 8.547 \text{ mA} \qquad \text{...(i)}$$

Emitter current $I_E = I_C + I_B = 8.547 + (120 \times 10^{-3}) = 8.667$ mA ...(ii)

EXERCISES

I. Descriptive Type Questions

1. Draw a block diagram of an unbiased NPN transistor. Name each part and show the depletion regions and barrier potentials.
2. Draw a block diagram of an unbiased PNP transistor. Name each part and show the depletion regions and barrier potentials.
3. With the help of a neat block diagram, explain the principle of operation of an NPN transistor, showing the depletion regions and barrier potentials.
4. With the help of a neat block diagram, explain the principle of operation of an PNP transistor, showing the depletion regions and barrier potentials.
5. Write a note on various types of transistor configurations ?
6. With the help of a diagram, show the various currents in a transistor. Briefly explain the origin of each current. Write the equations of I_E, I_B and I_C.
7. Sketch the transistor common base input characteristics and output characteristics. Explain the shape of each set of characteristics.
8. Explain the transistor common-emitter configuration and draw a circuit for drawing the common-emitter characteristics. Draw the common-emitter input and output characteristics and explain their shapes.
9. Draw the common-collector input, output and current gain characteristics and explain their shapes.
10. What is dc load line? How to draw it ?
11. Define operating point ? What should be its exact position for full cycle amplification ?
12. Write a note on factors affecting the stability of Q-point ?
13. Why NPN transistors are commonly used ?
14. Write a note on (a) Reverse Saturation current in transistor, (b) Thermal runaway ?
15. Draw a block diagram of an un-biased n-p-n transistor. Identify each part of the device and show the depletion regions and barrier voltages. Briefly explain. *(VTU Jan 2010)*
16. Write equations for collector current (I_c) in terms of emitter current (I_E) and α_{dc}, and in terms of base current (I_B) and, α_{dc}. Define α_{dc} and β_{dc} and mention typical values for each. *(VTU Jan 2010)*
17. Draw the common emitter circuit. Draw the input and output curves and explain the terms activation region, cut-off region and saturation region. *(VTU June 2009, June 2008)*
18. Draw input and output characteristics of a transistor in common base configuration and explain in detail. *(VTU Jan 2009)*

19. Obtain the relationship between α_{dc} and β_{dc} ?
20. Show that a transistor can be used as an amplifier ? *(VTU June 2008)*

II. Multiple Choice Questions

1. The doping of the emitter region of a transistor is _____ the base region.
   (a) Greater than (b) Equal to
   (c) Less than (d) Much lesser than
2. If $\alpha = 0.95$, then the value of β of the transistor is _____
   (a) 190 (b) 19
   (c) 0.05 (d) 25
3. The input resistance is highest for _____
   (a) CB amplifier (b) CC amplifier
   (c) CE amplifier (d) None of these
4. For cascading of amplifier, one should use _____
   (a) CE configuration (b) CB configuration
   (c) CC configuration (d) None of these
5. In a transistor the part heavily doped is _____
   (a) Emitter (b) Base
   (c) Collector (d) All are equally doped
6. In active region, the collector – base junction is _____
   (a) Forward biased (b) Reverse biased
   (c) Forward to reverse biased (d) Not biased
7. In CE configuration, when collector current is zero, V_{CE} equals _____
   (a) $V_{CC}/(R_C + R_E)$ (b) V_{CC}
   (c) V_{CC}/R_C (d) V_{CC}/R_E
8. The relation between α and β is given by _____
   (a) $\alpha = \beta$ (b) $\alpha = \beta/(1 - \beta)$
   (c) $\alpha = \beta/(1 + \beta)$ (d) $\alpha = 1/\beta$
9. In saturation region, the collector – base and emitter-base junctions are _____
   (a) Forward biased (b) Reverse biased
   (c) Unbiased (d) None of these

10. Common – emitter gain (β_{dc}) of a transistor is given by _____
    (a) I_C/I_B (b) I_E / I_C
    (c) I_C/I_E (d) None of these
11. In a transistor, the current conduction is due to _____ carriers
    (a) Majority (b) Minority
    (c) Both (d) None of these
12. The stability factor S is the rate of change of collector current with respect to _____
    (a) Reverse Saturation current (b) Collector current
    (c) Emitter current (d) Base current
13. If we reverse bias E/B and C/B junctions, the transistor will be in _____ region
    (a) Saturation (b) Active
    (c) Cut-off (d) Amplification
14. The process of damaging the transistor due to temperature dependent leakage current is called ____
    (a) Transistor Cut-off (b) Thermal Cut-off
    (c) Thermal runaway (d) Stability damage
15. Which of the following amplifier configuration has very high output resistance ?
    (a) Common Base (b) Common Emitter
    (c) Common Collector (d) Operational Amplifier
16. Which of the following amplifier is very close to ideal amplifier ?
    (a) Common Base (b) Common Emitter
    (c) Common Collector (d) Operational Amplifier
17. Which of the following amplifier has voltage gain less than Unity ?
    (a) Common Base (b) Common Emitter
    (c) Common Collector (d) Operational Amplifier
18. For keeping Q-point of a transistor fixed, the value of Stability factor should be _____
    (a) Higher than Unity (b) Zero
    (c) Unity (d) Lower than Unity
19. Which of the following circuit has lowest stability factor _____
    (a) Common Base (b) Common Emitter
    (c) Common Collector (d) None of these

20. In common Emitter configuration, the relationship between Collector current and Collector leakage current is given by _____

(a) $I_C = \beta I_B - (1 - \beta) I_{CO}$ (b) $I_C = \beta I_B + (1 - \beta) I_{CO}$

(c) $I_C = \beta I_B + (1 + \beta) I_{CO}$ (d) $I_C = \beta I_B - (1 + \beta) I_{CO}$

21. If the Q-point of a transistor is fixed near saturation, _____ peak of input signal is clipped.

(a) Negative (b) Positive

(c) Both (d) None of these

22. If the Q-point of a transistor is fixed near cut-off, _____ peak of input signal is clipped.

(a) Negative (b) Positive

(c) Both (d) None of these

23. Stability factor of CE configuration is _____

(a) 1 (b) β

(c) $\beta + 1$ (d) None of these

24. In a transistor, the ratio of three currents is given by _____

(a) $I_E : I_B : I_C :: 1:(1 + \alpha) : \alpha$ (b) $I_E : I_B : I_C :: 1\ (1 - \alpha) : \alpha$

(c) $I_E : I_B : I_C :: 1:(1 + \beta) : \alpha$ (d) None of these

25. Thermal runaway leads to _____

(a) Fluctuations in output current (b) Enhanced temperature of transistor

(c) Damage of transistor (d) All of these

III. Numerical Problems

1. Calculate α_{dc} and I_B for a transistor which has $I_C = 2.5$ mA and $I_E = 2.6$ mA . Also determine β_{dc} for the transistor.

Ans: (i) $\alpha_{dc} = 0.96$, (ii) $I_B = 100\ \mu A$, (iii) $\beta_{dc} = 24$.

2. (a) Find α_{dc} for $\beta_{dc} = 50$ and 190; (b) Find β_{dc} for each value of $\alpha_{dc} = 0.995$ and 0.9765 ?

Ans: (i) $\alpha_{dc} = 0.9804$ & 0.9947 (ii) $\beta_{dc} = 199$ & 41.55.

3. If the base current of a transistor is 20 μA and Emitter current is 6.4 mA, what are the values of α_{dc} & $\beta_{dc.}$? Also calculate collector current ?

Ans: $\beta_{dc} = 319$ $\alpha_{dc} = 0.9968$, $I_C = 6.38$ mA

4. If $\alpha_{dc} = 0.967$, $I_E = 10$ mA, what is the base current ?

Ans: $I_C = 9.67$ mA & $I_B = 0.33$ mA.

5. A transistor has $\alpha_{dc} = 0.98$, $I_{CO} = 5\ \mu A$, and $I_B = 100\ \mu A$. Find the value of collector and emitter currents.

Ans: $I_C = 5.15$ mA, $I_E = 5.25$ mA.

6. For a collector feedback bias circuit using a Si transistor with $\beta = 50$, $R_B = 100$ KΩ, $R_C = 1$ KΩ, and $V_{CC} = 5$V, draw the d.c. load line and determine the operating point. *(VTU Jan 2010)*
7. Calculate the values of I_C, I_E, and β_{dc} for a transistor with $\alpha_{dc} = 0.98$ and $I_B = 120$ μA. *(VTU Jan 2009)*
8. Determine the transistor currents in a fixed bias circuit with $V_{BB} = 5$V, $V_{CC} = 12$ V, $R_B = 220$ KΩ, $R_C = 3.3$ KΩ if $\beta = 100$. *(VTU June 2009)*
9. Calculate α_{dc} and β_{dc} for the transistor if I_C is measured as 1 mA and I_B is 25 μA. Also determine new base current to give $I_C = 5$ mA. *(VTU June 2008)*

Answers to Multiple Choice Questions

1. (a)	2. (b)	3. (a)	4. (a)	5. (a)	6. (b)	7. (b)	8. (c)	9. (a)	10. (a)	11. (c)
12 (a)	13. (c)	14. (c)	15. (a)	16. (d)	17. (c)	18. (c)	19. (a)	20. (c)	21. (a)	22. (b)
23. (c)	24. (b)	25. (d).								

UNIT 3

BIASING METHODS

OBJECTIVES

In this Unit we will study how to use Bipolar Junction Transistor in electronic circuits to amplify or to switch the signals by properly energizing the transistor using other active and passive components. The Unit objectives are :

(1) To study and analyze basic biasing circuits like Base bias, Collector to Base bias, and Voltage divider bias.

(2) To compare these basic bias circuits.

(3) To design these basic Bias circuits and analyze the voltage & current levels, and

(4) Qualitative study of thermal stability of bias circuits.

3.1 INTRODUCTION

3.1.1 Definition

The process of energizing the transistor to amplify input a.c. signal such that the fluctuations in ac signal should not drive the transistor to either cut-off or saturation region is called biasing. Hence, biasing is nothing but setting up a Q-point of the transistor near the middle of the dc load line.

3.1.2 Need of Biasing

Proper biasing is required for providing following two conditions :

1. To keep the Emitter-Base junction forward biased and Collector-Base junction reverse biased during the entire cycle of input signal.
2. To stabilize the Q-point against the changes in temperature, variations in transistor parameters, aging of the components etc.

The first condition will ensure the linear operation of transistor and hence flow of proper collector current (I_C), proper value of V_{BE} (0.7 V for S_i transistor and 0.3 V for G_e transistor), and proper value of V_{CE} (1 V for S_i & 0.5 V for Ge transistor).

The second condition will protect the transistor from thermal runaway.

3.1.3 Methods of Biasing

In the transistor amplifier circuits, the biasing can be done with two power supplies V_{BB} and V_{CC}. The V_{BB} supply is used for biasing of the emitter-base junction and V_{CC} supply is used for biasing the collector-base junction as shown in Fig. 3.1 (a). However, in practice, one power supply is used (only V_{CC}) for biasing both the junctions of a transistor as shown in Fig. 3.1 (b). The most commonly used methods for biasing the transistors are:

(1) Base bias (also called fixed bias).

(2) Base bias with collector feedback (also called *collector feedback bias).*

(3) Voltage divider bias (also called *self bias).*

3.2 BASE BIAS

Base bias is a circuit designed to satisfy the above first condition of need of biasing (Section 3.1.2).

3.2.1 Circuit Diagram

Figure 3.1 (a) shows a base bias circuit for a NPN transistor. The base bias circuit is also known as fixed bias circuit. In this case, the circuit uses two d.c. supplies namely V_{BB} and V_{CC}. But a more practical method is to use only one d.c. supply (V_{CC}) as shown in Fig. 3.1 (b). In this case, both the base and collector resistors are connected to the positive side of the V_{CC} supply. To simplify the circuit diagram, we may replace the battery by a line termination with a voltage indicated as shown in Fig. 3.1 (c).

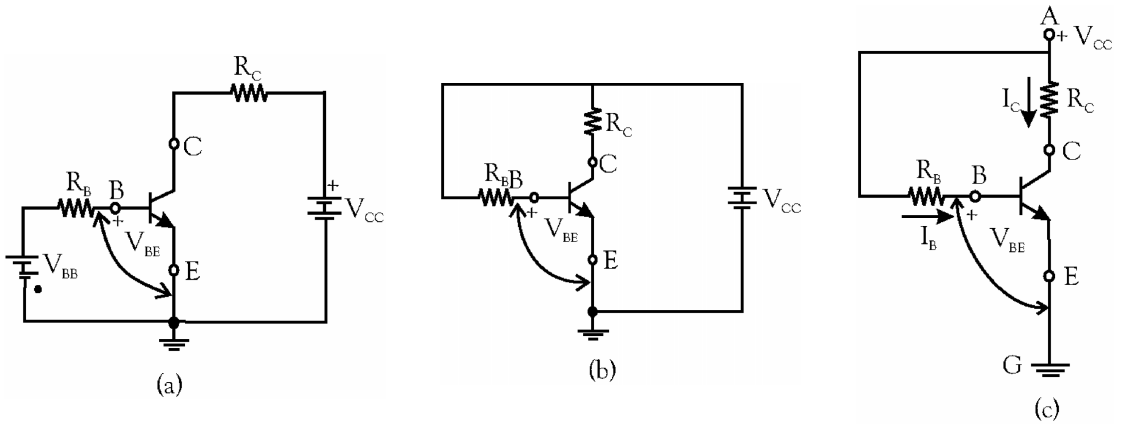


Figure 3.1 *Base bias circuit for a NPN transistor*

3.2.2 Circuit Analysis

To determine the d.c. bias currents and voltages in the base and collector of the Transistor, first consider the base-emitter circuit loop (ABEGA) in Fig. 3.1 (c). Applying Kirchoff's Voltage Law for the given loop,

$$+ V_{CC} - I_B R_B - V_{BE} = 0$$

or the base current,
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \ldots (3.1)$$

Since the supply voltage V_{CC} and the base-emitter voltage V_{BE} have fixed values of voltages, the selection of base bias resistor R_B fixes the value of the base current. The equation (3.1) may be simplified, if we neglect the value of base-emitter voltage, because it is usually very small as compared to the value of V_{CC}. Thus the approximate value of base current,

$$I_B = V_{CC}/R_B \quad \ldots (3.2)$$

Now consider the collector-emitter circuit loop (ACEGA) in Fig. 3.1 (c). Applying Kirchoff's Voltage Law for this loop,

$$+ V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C \quad \ldots (3.3)$$

The above equation gives the voltage drop across the collector-emitter terminals of the transistor. The value of collector current is given by the relation, $I_C = \beta I_B$ or

$$I_C = \beta . \frac{V_{CC}}{R_B} = \frac{V_{CC}}{R_B / \beta} \quad \ldots (3.4)$$

The above relation shows that the collector current is β times greater than the base current and is not at all dependent on the resistance of the collector circuit.

3.2.3 Advantages of Base Bias

(i) This biasing circuit is very simple as only one resistance R_B is required.

(ii) Biasing conditions can easily be set and the calculations are simple.

(iii) There is no loading of the source by the biasing circuit since no external resistor is employed at emitter terminal.

3.2.4 Limitations of Base Bias

(i) The values of collector current (I_C) and collector-to-emitter voltage (V_{CE}) are dependent on current gain β. But we know that β is strongly dependent upon the temperature. It means that collector current and collector-to-emitter voltage of a base bias circuit (which sets the Q-point of a transistor) will vary with the change in value of β due to variation in temperature. Hence, it is impossible to obtain a stable Q-point in a base-bias circuit. As a result the base bias is not used in amplifier circuits.

(ii) The stability factor is very high. Therefore, there are large chances in I_C which leads thermal runaway.

However, it is used in digital circuits, where the transistor is used as a switch between saturation and cut-off-regions.

Example 3.1

Fig. 3.2 shows a fixed bias circuit using an NPN transistor circuit. Determine the values of base current, collector current and the collector-to-emitter voltage ?

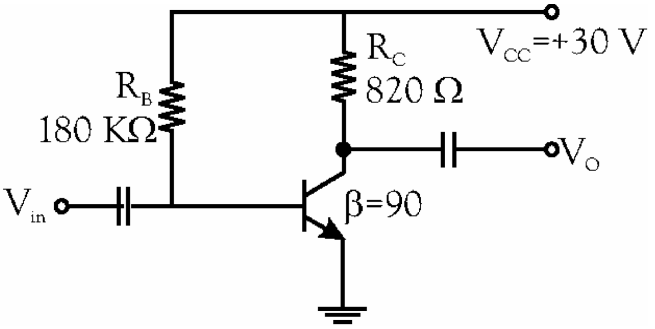


Figure 3.2

Solution:

Given: V_{CC} = 30 V; R_C = 820 Ω; R_B = 180 KΩ = 180 X 10^3 Ω; β = 90.

(i) Value of base current:

We know that the value of base current,

$I_B = V_{CC}/R_B$ = 30 /180 × 10^3 A = **0.166 mA**

(ii) Value of collector current:

We know that the value of collector current,

$I_C = \beta I_B$ = 90 x 0.166 x 10^{-3} = 14.9 x 10^{-3} A = **14.9 mA**

(iii) Value of collector-to-emitter voltage:

We know that the value of collector-to-emitter voltage,

$V_{CE} = V_{CC} - I_C R_C$ = 30 - (14.9 x 10^{-3}).(820) = 30 – 12.22 = **17.78 V**

3.2.5 Stability Factor of Base-Bias Circuit

The basic circuit used in the base bias (or fixed bias) is that of common-emitter configuration. We know that in common emitter configuration, the stability factor is equal to (1+ β). Therefore, for base-bias circuit the stability factor is given by :

$$S = 1+ \beta \quad \ldots (3.5)$$

3.3 COLLECTOR TO BASE BIAS

In order to decrease the stability factor further (ideally S = 1), collector to base bias is used. In collector

to base bias, the collector voltage provides necessary bias voltage to Base-Emitter junction. This circuit tries to decrease thermal runaway problem.

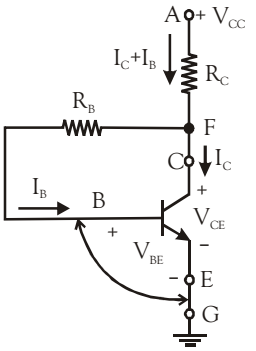


Figure 3.3 *Base bias with collector feedback*

3.3.1 Circuit Diagram

Fig. 3.3 shows a d.c. bias circuit in which the base resistor (R_B) is connected to the collector terminal of a transistor rather than to the V_{CC} supply as in a base bias circuit. Here, the collector voltage provides the bias to base-emitter junction. The resistor R_B acts as a feedback resistor. It provides a very stable Q-point by reducing the effect of variations in current gain (β).

3.3.2 Circuit Analysis

To determine the d.c. bias currents and voltages in the base and collector of the transistor, consider the base-emitter circuit loop (AFBEGA) in the d.c. bias circuit. Applying Kirchoff's Voltage Law to the base-emitter circuit loop.

$$+ V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

Substituting I_C equal to $\beta.I_B$ in the above equation and solving for the base current,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_C} = \frac{V_{CC} - V_{BE}}{R_B + \beta.R_C} \qquad \text{... (Taking } \beta + 1 = \beta)$$

and the collector current,

$$I_C = \beta. I_B = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta} = \frac{V_{CC}}{R_C + R_B / \beta} \qquad \text{... } (\because V_{CC} >> V_{BE}) \qquad ...(3.6)$$

Now applying Kirchoff's Voltage Law to the collector-emitter circuit loop *(i.e.,* AFCEGA) in d.c. bias circuit.

$$+ V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

Substituting $I_C + I_B$ equal to I_C in the above equation and solving it for collector-to-emitter voltage,

$$V_{CE} = V_{CC} - I_C . R_C \qquad ...(3.7)$$

Example 3.2

Calculate the Q-point values i.e., the values of collector current and collector-to-emitter voltage for the d.c. bias circuit shown in Fig. 3.4. Also draw the load line and locate Q-point on it. Assume V_{BE} = 0.7 V.

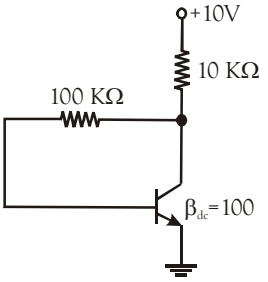


Figure 3.4

Solution:

Given: V_{CC} = 10V; R_C = 10 KΩ = 10 x 10^3 Ω; R_B = 100 KΩ = 100 x 10^3 Ω; β_{dc} = 100 and V_{BE} = 0.7 volt.

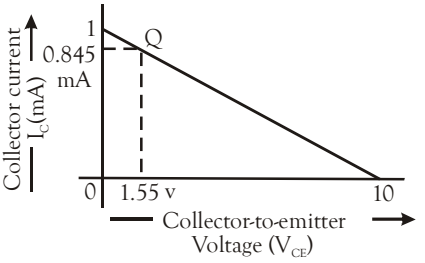


Figure 3.5 *dc load line*

Q-point values

The value of collector current,

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}} = \frac{10 - 0.7}{10 \times 10^3 + \frac{100 \times 10^3}{100}}$$

$$= 0.845 \text{ X } 10^{-3} \text{ A} = 0.845 \text{ mA}$$

and the collector-to-emitter voltage,

$$V_{CE} = V_{CC} - I_C . R_C = 10 - [(0.845 \text{ X } 10^{-3}) \text{ x } (10 \text{ X } 10^3)]$$

$$= 10 - 8.45 = 1.55 \text{ V}$$

D.C load line

We know that upper end of the load line

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10}{10 \times 10^3} = 1 \times 10^{-3} \text{ A} = 1 \text{ mA}$$

and lower end of the load line:-

$$V_{CE\,(cut\text{-}off)} = V_{CC} = 10 \text{ V}$$

Thus the load line may be obtained by joining the upper and lower ends as shown in Fig. 3.5. The Q-point corresponding to the collector current of 0.845 mA and collector-to-emitter voltage of 1.55 V is indicated on the load line.

3.3.3 Stability of Collector to Base Bias

If we apply Kirchoff's Voltage Law to the base-emitter circuit shown in Fig. 3.3, then we get

$$+ V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

Rearranging the above equation and solving for base current,

$$I_B = \frac{V_{CC} - V_{BE} - I_C . R_C}{R_C + R_B}$$

Differentiating the above expression with respect to I_C,

$$\frac{dI_B}{dI_C} = \frac{0 - 0 - 1.R_C}{R_C + R_B} = -\frac{R_C}{R_C + R_B}$$

Substituting the value of dI_B/dI_C in the general expression for stability factor,

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_C+R_B}\right)} = \frac{1+\beta}{1+\beta\times\frac{R_C}{R_C+R_B}} \quad ...(3.8)$$

From the above expression it is evident that the stability factor (S) of a collector feedback bias is smaller than (1 + β). Therefore, the biasing arrangement of collector feedback resistor is certainly an improvement over the fixed bias circuit.

3.3.4 Advantages of Collector to Base Bias

(i) It is a simple method as it requires only two resistors R_B & R_C.

(ii) This circuit provides some stabilization of the operating point as discussed below:

$$V_{CE} = V_{BE} + V_{CB}$$

If there is an increase in collector leakage current due to increase in temperature, the total collector current tends to increase. As a result, V_{CE} tends to decreases due to greater drop across R_C. This will decreases V_{CB} & hence I_B. Such decrease in I_B decreases I_C to original value compensating previous increase.

3.3.5 Limitations of Collector to Base Bias

(i) The circuit does not provide good stabilization and the stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and aging effects.

(ii) This circuit provides a negative feedback which reduces the gain of the amplifier. During the positive half-cycle of the input signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current. This will affect the stability of Q-point.

3.4 VOLTAGE DIVIDER BIAS

In base bias and Collector to base bias, the values of d.c. current (I_C) and voltage (V_{CE}) of the collector depends upon the current gain (β) of the transistor. But we know that the value of current gain (β) is temperature sensitive. Therefore it would be desirable to provide a d.c. bias circuit which is independent of the transistor current gain (β). The d.c. bias circuit shown in Fig. 3.6 (a) meets this condition and is thus a very popular bias circuit. It is commonly known as voltage divider bias or self bias circuit.

3.4.1 Circuit Diagram

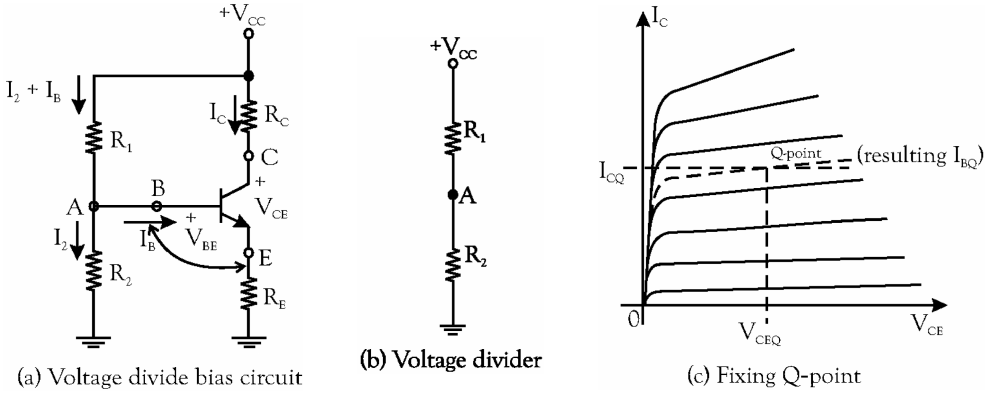


Figure 3.6

The name voltage divider is derived from the fact that resistors R_1 an R_2 form a voltage divider across the V_{CC} supply. The voltage drops across resistor R_2 forward biases the base-emitter junction of a transistor. The emitter resistor (R_E) provides the d.c. stability.

3.4.2 Circuit Analysis

A basic assumption is that the resistance looking into the base is much larger than that of the resistor R_2. If this is so, then the current through resistor R_1 flows almost completely into resistor R_2 and the two resistors may be considered effectively in series as shown in Fig. 3.6 (b). The voltage at the junction of the resistor (i.e., point A), which is also the voltage at the base of the transistor, is then determined simply by the voltage divider network of R_1 and R_2 and the supply voltage. If the current through resistors R_1 and R_2 is of the order of milliamperes and that through the base is of the order of the microamperes, then the base current component can be neglected.

(i) Base Voltage (V_B):

The voltage at the transistor base is voltage drop across R_2, and can be obtained by voltage division rule,

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2} \qquad \text{... (3.9)}$$

Since the voltage drop across the forward baised base-emitter junction (V_{BE}) is very small as compared to the voltage at the base (V_B), therefore the voltage at the emitter is almost equal to the voltage at the base *i.e.*,

$$V_E = V_B \qquad \text{...(Neglecting } V_{BE}\text{)}$$

(ii) Emitter current (I_E):

The emitter current is given by the relation,

$$I_E = \frac{V_E}{R_E} \qquad \text{... (3.10)}$$

(iii) Collector current (I_C):

The collector current is given by the relation,

$$I_C = I_E$$

The voltage drop across the collector resistor,

$$V_{R_C} = I_C . R_C$$

To determine the voltage across R_2, we can apply Kirchhoff's voltage law to the base circuit,

$$V_2 = V_{BE} + V_E$$

or $$V_2 = V_{BE} + I_E R_E \qquad \text{... (3.11)}$$

or $$I_E = \frac{V_2 - V_{BE}}{R_E} \quad \text{since } I_C = I_E, \quad I_C = \frac{V_2 - V_{BE}}{R_E} \qquad \text{... (3.12)}$$

Thus in this circuit, collector current I_C is independent on β.

The voltage at the collector (measured with respect to the ground) is given by the relation

$$V_C = V_{CC} - V_{R_C} = V_{CC} - I_C . R_C \qquad \text{...(3.13)}$$

(iv) Collector-to-emitter voltage (V_{CE}):

Using the circuit, the collector to emitter voltage is given by the relation,

$$V_{CE} = V_C - V_E = V_{CC} - I_C . R_C - I_E . R_E$$

$$= V_{CC} - I_E (R_C + R_E) \qquad (\because \ I_C = I_E)$$

or $$V_{CE} = V_{CC} - I_C(R_C + R_E) \qquad \text{...(3.14)}$$

3.4.3 Stability of Voltage Divider Bias

In this circuit, excellent stabilization is provided by R_E. Consideration of Eqn. (3.11) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will increase the voltage drop across emitter resistance R_E. As voltage drop across R_2 (i.e. V_2) is independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor: It can be shown mathematically that stability factor (S) of the voltage divider bias circuit is given by the relation,

$$S = \frac{(\beta + 1)(R_T + R_E)}{R_T + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \frac{R_T}{R_E}}{\beta + 1 + \frac{R_T}{R_E}} \qquad \text{where } R_T = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio R_T / R_E is very small, then R_T / R_E can be neglected as compared to 1 and the stability factor becomes :

$$S = (\beta + 1) \times \frac{1}{\beta + 1} = 1 \qquad \ldots (3.15)$$

Thus the voltage divider bias provides stability factor close to unity.

3.4.4 Advantages of voltage divider bias

1. Voltage divider bias circuit can successfully provide a d.c. Bias which is independent of the transistor current gain (β).
2. This bias circuit has the smallest possible value of stability factor S and leads to the maximum possible thermal stability. Due to design considerations, R_T/R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Example 3.3

Determine the value of collector current and collector-to-emitter voltage for the voltage divider bias circuit shown in Fig. 3.7. Assume V_{BE} = 0.7 V and β = 100.

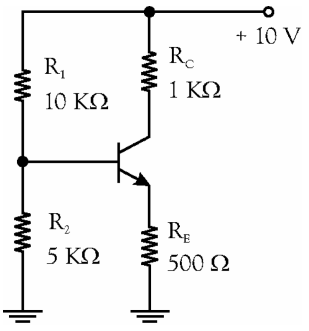


Figure 3.7

Solution:

Given: V_{CC}= 10 V; R_C = 1 KΩ = 1 x 10^3 Ω; R_1 = 10 KΩ; R_2 = 5 KΩ; R_E = 500 Ω; V_{BE} = 0.7V and β = 100.

To determine Collector current:

We know that base voltage

$$V_B = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right) = 10\left(\frac{5}{10 + 4}\right)$$

$$= 3.33 \text{ V}$$

and voltage at the emitter,

$$V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63\,V$$

$\therefore$ Emitter current,

$$I_E = \frac{V_E}{R_E} = \frac{2.63}{500} = 5.26 \times 10^{-3}\ A = 5.26\ mA$$

and collector current,

$$I_C = I_E = 5.26 \text{ mA}$$

To determine Collector-to-emitter voltage :

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right) = 10 - 5.26 \times 10^{-3}\,(1 \times 10^3 + 500)$$

$$= 10 - 7.89 = 2.11 \text{ V} \qquad \textbf{Ans.}$$

Example 3.4

Determine the d.c. bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 3.8.

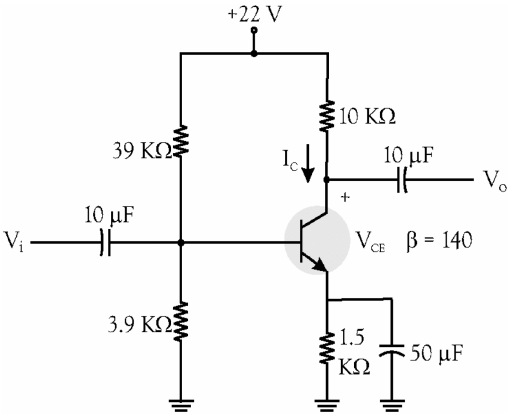


Figure 3.8

Solution:

$$R_{Th} = R_1 \,||\, R_2$$

$$= \frac{(39\,K\Omega)(3.9K\Omega)}{39K\Omega + 3.9K\Omega} = 3.55\,K\Omega$$

$$V_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9K\Omega)(22\,V)}{39\,K\Omega + 3.9K\Omega} = 2V$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2V - 0.7V}{3.55K\Omega + (141)(1.5K\Omega)} = \frac{1.3V}{3.55\,K\Omega + 211.5\,K\Omega} = 6.05\ \mu A$$

$I_C = \beta I_B$

$= (140)\ (6.05\ \mu A)$

$= 0.85\ mA$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$= 22\ V - (0.85\ mA)(10K\Omega + 1.5\ K\Omega)$

$= 22\ V - 9.78\ V$

$= 12.22\ V$

Example 3. 5

Fig. 3.9 (a) shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor is made by silicon.

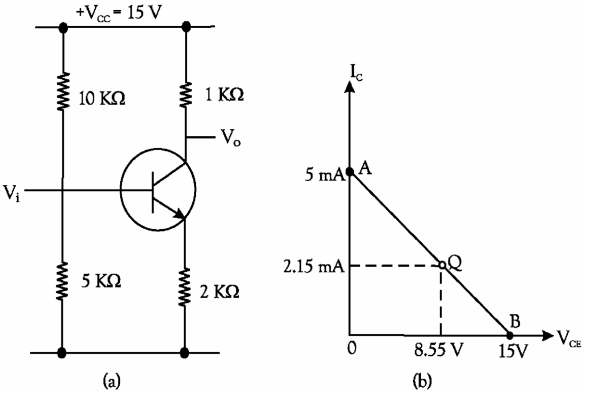


Figure 3.9

Solution:

(i) d.c. load line: The collector-emitter voltage V_{CE} is given by;

$$V_{CE} = V_{CC} - I_C(R_C+R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15$ V. This locates the first point B (OB = 15 V) of the load line on the collector-emitter voltage axis.

When $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15\,V}{(1+2)K\Omega} = 5\,mA$$

This locates the second point A (OA = 5 mA) of the load line on the collector current axis. By joining points A and B, the d.c. load line AB is constructed lis shown in Fig. 3.9 (b).

(ii) Operating point: For silicon transistor, $V_{BE} = 0.7$ V. Voltage across 5 KΩ,

$$V_2 = \frac{V_{CC}}{10+5} \times 5 = \frac{15 \times 5}{10+5} = 5\,V$$

∴ Emitter current is given by,

$$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2\,K\Omega} = \frac{4.3V}{2K\Omega} = 2.15\,mA$$

Then the collector current, $I_C \cong I_E = 2.15$ mA

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C (R_C + R_E) = 15 - 2.15$ mA x 3 KΩ = 15 – 6.45 = 8.55 V

∴ The co-ordinates of Operating point are: (8.55 V, 2.15 mA)

Fig. 3.9 (b) shows the operating point (Q-point) on the load line. Its co-ordinates are:

$I_C = 2.15$ mA, $V_{CE} = 8.55$ V.

3.5 COMPARISON OF BASIC BIAS CIRCUITS

Table 3.2 Comparison of basic bias circuits

S. No.	Base Bias	Collector to Base Bias	Voltage Divider Bias
1	Bias is provided by fixing V_{BE}.	Bias is provided by fixed I_C and V_{BE}.	Bias is provided by voltage division to base using R_1 & R_2 and emitter stabilization resistor (R_E)

S. No.	Base Bias	Collector to Base Bias	Voltage Divider Bias
2	V_{BE} is independent of I_C so that Q-point is unstable.	Because of feedback from collector to base, the variation in I_C is compensated to a small extent which improves the stability of the circuit to some extent.	Voltage divider circuit provides constant V_{BE} and Emitter stabilization resistor R_E provides constant I_C. So that Q-point is more stable than base and collector to base bias.
3	Stability factor is given by $S = (1 + \beta)$ which is far above 1	Stability factor is less than $(1 + \beta)$ which is above 1.	Stability factor can be close to 1 and independent on β.
4	Simple to design	Difficult to design	More difficult to design
5	Not used in amplifier circuits	Not commonly used in amplifiers	Universally used in amplifier circuits

3.6 BIAS CIRCUIT DESIGN

In practice, the following steps are used to design transistor biasing and stabilization circuits:-

Step 1: It is a common practice to take R_E = 500 – 1000 Ω. Greater the value of R_E, better is the stabilization. However, if R_E is very large, higher voltage drop across it leaves reduced voltage drop across the collector load. Consequently, the output is decreased. Therefore, a compromise has to be made in the selection of the value of R_E.

Step 2: The zero signal current I_C is chosen according to the signal swing. However, in the initial stages of most transistor amplifiers, zero signal I_C = 1 mA is sufficient. The major advantages of selecting this value are :

(i) The output impedance of a transistor is very high at 1 mA. This increases the voltage gain.

(ii) There is little danger of overheating as 1 mA is quite a small collector current. It may be noted that working the transistor below zero signal I_C = 1 mA is not advisable because of strongly non-linear transistor characteristics.

Step 3: The values of resistances R_1 and R_2 are so selected that current I_1 flowing through R_1 and R_2 is at least 10 times I_B i.e., $I_1 \geq 10\ I_B$. When this condition is satisfied, good stabilization is achieved.

Step 4: The zero signal I_C should be a little more (say 20%) than the maximum collector current swing due to signal. For example, if collector current change is expected to be 3 mA due to signal, then select zero signal $I_C \cong 3.5$ mA. It is important to note that selecting zero signal I_C below this value may cut off a part of negative half-cycle of the signal. On the other hand, selecting a value much above this value (say 15 mA) may unnecessarily overheat the transistor, resulting in wastage of battery power. Moreover, a higher zero signal I_C will reduce the value of R_C (for same V_{CC}), resulting in reduced voltage gain.

3.6.1 Base Bias Design

To design base bias, following equations are used:

1. $R_B = \dfrac{V_{CC} - V_{BE}}{I_B}$

2. $I_C = \beta I_B$

3. $R_C = \dfrac{V_{CC} - V_{CE}}{I_C}$

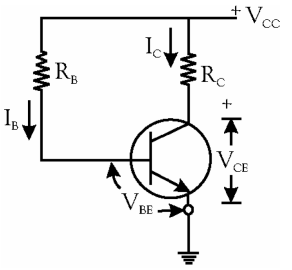


Figure 3. 10

Problem 1: Design a base bias circuit as given in Fig. 3.11 to have V_{CE} = 5 V and I_C = 6 mA. The supply voltage is 20 V and the transistor has β = 100.

Solution:

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{20\ V - 5V}{6\ mA}$$

$$= 2.5\ K\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{6m\ A}{100} = 60\ \mu A$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20V - 0.7V}{60\ \mu A} = 321.6\ K\Omega$$

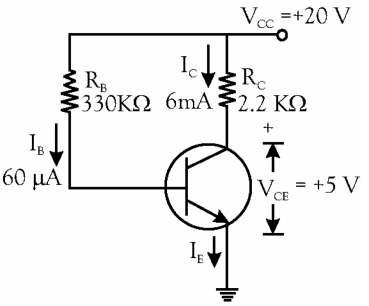


Figure 3. 11

3.6.2 Collector to Base Bias Design

Collector-to-base bias circuit is designed in a similar way as the design of the base bias circuit, except that the voltage across R_B is (V_{CE} – V_{BE}) and the current through R_C is (I_B + I_C). The equations used in the design are as follows:

(a) $I_B = \dfrac{I_C}{\beta}$

(b) $R_C = \dfrac{V_{CC} - V_{CE}}{I_C + I_B}$

(c) $R_B = \dfrac{V_{CE} - V_{BE}}{I_B}$

Problem 2: Design the Collector-to-Base Bias Circuit of Fig. 3.12, so that the supply voltage is 20 V, V_{CE} = 5 V, I_C = 6 mA and the transistor β is 100.

Solution:

(1) $I_B = \frac{I_C}{\beta} = \frac{6mA}{100} = 60\,\mu A$

(2) $R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B} = \frac{20V - 5V}{6m\,A + 60\,\mu A} = 2.48\,K\Omega$

(3) $R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{5V - 0.7V}{60\,\mu A} = 71.6\,K\Omega$

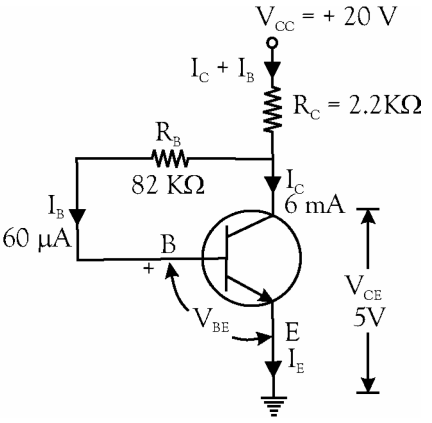


Figure 3.12

3.6.3 Voltage Divider Bias Design

By examining the circuit of voltage divider circuit, the values of the resistors may be found by using the following equations:

(a) $R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$

(b) $R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C}$

(c) $R_1 = \frac{V_{CC} - V_B}{I_2}$

(d) $R_2 = \frac{V_B}{I_2}$

(e) $I_2 = \frac{I_C}{10}$

Problem 3: Design the voltage divider bias for the given circuit in Fig. 3.14, if R_C = 2.2 KΩ, V_{CC} = 9 V and β = 50. Determine the values of R_1, R_2 and R_E. Take V_{BE} = 0.3 V and I_1 = 10 I_B. The operating point is chosen such that I_C= 2 mA, V_{CE} = 3 V.

Solution:

$$R_C = 2.2\,K\Omega,\ V_{CC} = 9\,V,\ \beta = 50$$

$$V_{BE} = 0.3V, \qquad I_1 = 10\, I_B$$

Base current, $$I_B = \frac{I_C}{\beta} = \frac{2mA}{50} = 0.04\ mA$$

Current through R_1 & R_2,

$$I_1 = 10 I_B = 10 \times 0.04 = 0.4\ mA$$

Now,

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$\therefore \qquad R_1 + R_2 = \frac{V_{CC}}{I_1} = \frac{9V}{0.4mA} = 22.5K\Omega$$

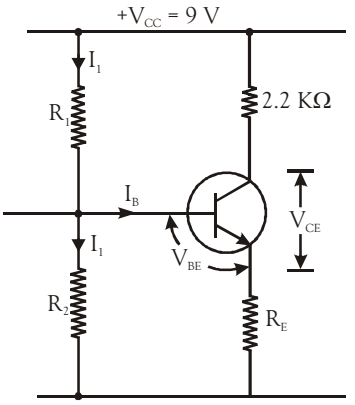


Figure 3.13

Applying Kirchhoff's voltage law to the collector side of the circuit, we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$9 = 2\,mA \times 2.2\,K\Omega + 3 + 2\ mA \times R_E \qquad \text{since } I_C \cong I_E$$

$$\therefore \qquad R_E = \frac{9 - 4.4 - 3}{2} = 0.8\ K\Omega = 800\ \Omega$$

Voltage across R_2, $V_2 = V_{BE} + V_E = 0.3 + 2mA \times 0.8\,K\Omega$

$$= 0.3 + 1.6 = 1.9V$$

$$\therefore \qquad \text{Resistance } R_2 = V_2 / I_1 = 1.9V / 0.4mA = 4.75\,K\Omega$$

and $$R_1 = 22.5 - 4.75 = 17.75\ K\Omega$$

Problem 4: An npn transistor circuit shown in Fig. 3.14, has α = 0.985 and V_{BE} = 0.3 V. If V_{CC} = 16 V, calculate R_1 and R_C to place Q-point at I_C = 2 mA, V_{CE} = 6 V.

Solution:

$$\alpha = 0.985, V_{BE} = 0.3\,V, V_{CC} = 16\,V$$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.985}{1 - 0.985} = 66$$

Base current,

$$I_B = \frac{I_C}{\beta} = \frac{2\,mA}{66} = 0.03\,mA$$

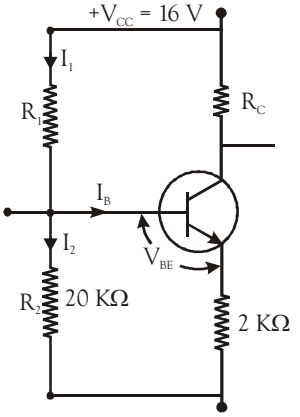


Figure 3.14

Voltage across R_2,

$$V_2 = V_{BE} + V_E = 0.3 + 2\,mA \times 2K\Omega$$

$$= 4.3 \text{ V}$$

$\therefore$ Voltage across $R_1 = V_{CC} - V_2 = 16 - 4.3 = 11.7$ V

Current through R_1 & R_2

$$I_1 = \frac{V_2}{R_2} = \frac{4.3\,V}{20K\Omega} = 0.215\,mA$$

$\therefore$ Resistance $$R_1 = \frac{Voltage\ across\ R_1}{I_1} = \frac{11.7V}{0.215mA} = 54.4\,K\Omega$$

Voltage across $$R_C = V_{CC} - V_{CE} - V_E$$

$$= 16 - 6 - 2 \times 2 = 6V$$

$\therefore$ Collector resistance,

$$R_C = \frac{Voltage\ across\ R_C}{I_C} = \frac{6V}{2\,mA} = 3\,K\Omega$$

3.6.4 How to Bias PNP Transistors?

A PNP transistor is considered as a complement of an NPN transistor. i.e., all voltages and currents in a PNP transistor are opposite to those of the NPN transistor. Thus the d.c. biasing circuit for a PNP transistor may be obtained by the following two modifications :

1. Replace the NPN transistor by a PNP transistor.
2. Reverse all voltages and hence the direction of currents will be reversed.

A positive V_{CC} supply in an NPN transistor biasing circuit will become the negative supply in a PNP transistor biasing circuit with positive terminal of the supply is connected to ground. It is true because to forward bias the base-emitter junction of a PNP transistor, the base-emitter voltage (V_{BE}) has a negative value. Similarly, to reverse bias the collector-base junction, the collector-to-base voltage (V_{CB}) has a negative value.

3.7 THERMAL STABILITY OF BIAS CIRCUITS

3.7.1 Operating Point Stability

In any transistor amplifier which is not properly biased, the collector current in a transistor changes rapidly when:

(i) the temperature changes,

(ii) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (i.e. zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. Such a process makes the operating point independent of these variations. This is known as operating point stabilization.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as stabilization. Once stabilization is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor i.e. the operating point is fixed. A good biasing circuit always ensures the stabilization of operating point.

Need for stabilization:

Stabilization of the operating point is necessary due to the following reasons:-

(i) Temperature dependence of I_C

(ii) Individual component parameter variations

(iii) Thermal runaway.

(i) Temperature dependence of I_C: The collector current I_C is given by following relation,

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1)\, I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 6° C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilize the operating point i.e. to hold I_C constant in spite of temperature variations.

(ii) Individual variations: The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilize the operating point i.e. to hold I_C constant irrespective of individual variations in transistor parameters.

(iii) Thermal runaway: The collector current for a CE configuration is given by;

$$I_C = \beta\, I_B + (\beta + 1)\, I_{CBO} \qquad \ldots (3.16)$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilization is done, the collector leakage current I_{CBO} also increases. It is clear from Eqn. (3.16) that if I_{CBO} increases, the collector current I_c increases by $(\beta + 1)\ I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out. The self-destruction of an un-stabilized transistor is known as **thermal runaway**.

3.7.2 Relative Performance of Si & Ge Transistors

1. Why Si transistor is commonly used in electronic circuits?

Si transistor is commonly used in electronic circuits due to following reasons:

(i) **Smaller collector leakage current I_{CO}**: At room temperature, a silicon crystal has fewer free electrons than a germanium crystal. Hence silicon will have much smaller collector leakage current (I_{CO}) than that of germanium. In general, with germanium I_{CO} is 10 to 100 times greater than with silicon.

(ii) **Smaller variation of I_{CO} with temperature:** The variation of I_{CO} with temperature is less in silicon as compared to germanium. A rough rule of thumb for germanium is that I_{CO} approximately doubles with each 6°C rise while in case of silicon, it approximately doubles with each 10°C rise.

(iii) **Greater range of working temperature:** The structure of germanium will be destroyed at a temperature of approximately 100°C. The maximum normal working temperature of germanium is 70°C but silicon can be operated upto 150°C. Therefore, silicon devices are not easily damaged by excess heat.

EXERCISES

I. Descriptive Type Questions

1. What is biasing in transistor amplifiers ? Explain the conditions to be fulfilled to achieve faithful amplification in a transistor amplifier.
2. What is transistor biasing ? Why it is needed ?
3. What do you mean by stabilization of operating point?
4. Mention the essentials of a biasing circuit.
5. Describe the various methods used for transistor biasing. State their advantages and disadvantages.
6. Describe the voltage divider bias method in detail. How stabilization of operating point is achieved by this method ?
7. Mention the steps that are taken to design the transistor biasing and stabilization circuits.
8. Write short notes on the following:
   (i) Operating point (ii) Stabilization of operating point.
9. Why Si transistor is commonly used in electronic circuits ?
10. How to bias PNP transistors ?
11. Compare base bias, collector to base bias and voltage divider bias with regard to stability of the transistor collector voltage with spread in h_{FE} value. *(VTU Jan 2010)*
12. What is the meaning of transistor biasing ? Draw a neat sketch to explain the base biasing of a transistor in CE mode. What is its stability factor ? *(VTU June 2009)*
13. List the transistor biasing circuits. Explain with neat circuit the operation of Base-bias. *(VTU Jan 2009)*
14. Define biasing of a transistor ? Compare the base bias, collector to base bias and voltage divider bias and discuss the advantages and disadvantages of the three types of bias circuits. *(VTU June 2008)*
15. Define biasing of Transistor. Explain with neat circuit the operation of voltage divider bias circuit. *(VTU Jan 2008)*
16. Discuss the thermal stability of transistor bias circuit with respect to I_{CBO} and V_{BE}. *(VTU Jan 2008)*
17. With a circuit diagram, explain the operation of collector to base bias circuit. Explain how this circuit significantly improves the bias stability for h_{FE} changes compared to base bias. *(VTU June 2007)*

II. Multiple Choice Questions

1. For an emitter follower, the voltage gain is _____
   (a) Unity (b) Greater than unity
   (c) Less than unity (d) Zero
2. The self bias arrangement gives a better Q-point stability when _____
   (a) R_C is small (b) β is small but R_C is large
   (c) Both β and R_C are large (d) None of these
3. The load line moves parallel to itself on the CE output characteristics of a transistor when _____
   (a) R_L changes (b) V_{CC} changes
   (c) Both R_L and V_{CC} change (d) None of these
4. To work as a linear amplifier a transistor must operate in _____
   (a) Active region (b) Saturation region
   (c) Nonlinear region (d) Cut-off region
5. When used as a switch the transistor operates in _____
   (a) Active region (b) Saturation and cut-off region
   (c) Active and saturation region (d) Cut-off region
6. Even with sinusoidal base current we get non-sinusoidal collector current in common emitter configuration because of _____
   (a) Noise introduced in base current (b) Large resistance of the signal source
   (c) Large input resistance of transistor (d) Non parallel output characteristics
7. The stability factor S is the rate of change of collector current with
   (a) Base current (b) Reverse Saturation current
   (c) Emitter current (d) V_{CC}
8. The interaction of DC load line and the output characteristics of a transistor is called _____
   (a) Q-Point (b) Quiescent point
   (c) Operating point (d) All of these
9. The biasing circuit, which gives most stable operating point is _____
   (a) Base Bias (b) Collector to base bias
   (c) Voltage divider bias (d) None of these
10. Reverse saturation current doubles for every _____ ^{O}C rise in temperature.
    (a) 50 (b) 40
    (c) 30 (d) 10

11. Which of the following bias is universally used in amplifier circuits _____
    (a) Base Bias (b) Collector to base bias
    (c) Voltage divider bias (d) None of these
12. Base bias is used in _____
    (a) Amplifiers (b) Digital Switches
    (c) Both (a) & (b) (d) None of these
13. Base bias is also called _____
    (a) Fixed bias (b) Self bias
    (c) Both (a) & (b) (d) None of these
14. Stability factor of Voltage divider bias is _____
    (a) Close to 1 (b) Independent on β
    (c) Both (a) & (b) (d) None of these
15. In an unbiased transistor amplifier, the collector current changes due to _____
    (a) Changes in Temperature (b) Changes in device parameters
    (c) Changes in the value of dc supply (d) All of these

III. Numerical Problems

1. Design a base bias circuit with V_{CE} = 5 V and I_C = 6 mA. The supply voltage is 20 V and the transistor has β = 100.

   Ans: R_C = 2.5 KΩ, I_B = 60 μA, R_B = 321.6 KΩ
2. For a base bias circuit with silicon transistor, V_{CC} = 12 V, V_{CE} = 6 V, I_C = 5 mA, β_{dc} = 100. Determine I_B, R_C and R_B.

   Ans: I_B = 50 μA, R_B = 226 KΩ, R_C = 1.188 KΩ
3. Design the Collector-to-Base Bias Circuit so that the V_{CC} = 20 V, V_{CE}= 5 V, I_C = 6 mA and the transistor β is 100.
4. Design the Collector-to-Base Bias Circuit so that the supply voltage is 20 V, V_{CE}= 5 V, I_C = 6 mA and the transistor β is 100.

   Ans: I_B = 60 μA, R_C = 2.48 KΩ, R_B = 71. 6 KΩ.
5. Design a voltage divider bias circuit to have V_{CE}=V_E = 6 V and I_C =1.5 mA. The circuit operates from a 20 V supply, and the transistor β is 100.

   Ans: R_E = 4 KΩ, R_C = 5.43 KΩ, R_2 = 43.6 KΩ, R_1 = 96.5 KΩ
6. Design a voltage divider bias circuit with V_{CC} = 12 V, V_{CE} = 6 V, I_C = 5 mA, and β = 100.

   Ans: R_C = 600 Ω, R_E = 600 Ω, R_1 = 16.6 KΩ, R_2 = 7.4 KΩ

7. Design a voltage divider bias circuit with V_{CC} = 16 V, V_{BE} = 0.7 V, I_C = 3 mA, R_2 = 2.2 KΩ, R_E = 330 Ω, R_C = 3.3 KΩ and α = 0.98. Also determine stability factor.

   Ans: R_1 = 11.22 KΩ, S = 5.916

8. Design a collector to base bias circuit with the following specifications V_{CE} = 5 V, I_C = 5 mA, V_{CC} = 15 V and h_{FE} = 100, V_{BE} = 0.7V. *(VTU Jan 2010)*

9. Draw the dc load line for the voltage divider biasing circuit which has V_{CC} = 30 V, R_1 = 6.8 KΩ, R_2 = 1 KΩ, R_E = 750 Ω and R_C = 3 KΩ. Find the collector current and Q-point. *(VTU June 2009)*

10. Design a collector to base bias circuit to have V_{CE} = 5 V and I_C = 5 mA, the supply voltage is 15 V and β_{dc} = 100, assume silicon transistor. *(VTU Jan 2009).*

11. Transistor is biased in voltage divider bias circuit with R_1 = 47 KΩ, R_2 = 15 KΩ, R_C = 1.5 KΩ, R_E = 1 KΩ, V_{CC} = 15 V. Compare Emitter voltage (V_E), Collector Voltage (V_C) and Collector-emitter voltage (V_{CE}). *(VTU Jan 2008).*

12. A collector to–base bias circuit has V_{CC} = 5 V, R_C = 5.6 KΩ, R_B = 82 KΩ, and V_{CE} = 5 V. Determine the transistor h_{FE} value. Calculate new V_{CE} level when a transistor with h_{FE} = 50 is substituted. *(VTU June 2007).*

13. For the base bias circuit for a NPN transistor, find I_B, I_C, and V_{CE}, if R_C = 2.2 KΩ, R_B = 470 KΩ, V_{CC} = 18 V, h_{FE} = 100, V_{BE} = 0.7 V. Draw the DC load line and indicate the Q-point. *(VTU Jan 2007).*

Answers to Multiple Choice Questions

1. (c) 2. (d) 3. (c) 4. (a) 5. (b) 6. (d) 7. (b) 8. (d) 9. (c) 10. (d) 11. (c)
12 (b) 13. (a) 14. (c) 15. (d)

UNIT 4

OTHER DEVICES

OBJECTIVES

In this Unit we will study some of other electronic active components used in electronic circuits either to amplify or to regulate and control the current or voltage. The Unit objectives are:

(1) To study the structure and characteristics of Silicon Controlled Rectifier (S.C.R), SCR Control Circuits, and S.C.R applications.

(2) To study the structure and characteristics of Unijunction transistor (UJT) and to study various applications of UJT.

(3) To study the structure and characteristics of Junction Field Effect Transistor (JFET), its characteristics and amplification properties.

4.1 SILICON CONTROLLED RECTIFIER (S.C.R)

Silicon Controlled Rectifier is a three terminal electronic device manufactured using silicon. The device is invented in the year 1957, and used as a controlled switch to perform various functions such as rectification, inversion and regulation of power flow. The SCR is an important electronic device because it can be fabricated to handle currents upto several thousand amperes and voltages more than 1 Kilovolts. It is a unidirectional power switch and is being extensively used in switching d.c. and a.c., rectifying a.c. to give controlled d.c. output, converting d.c. into a.c. *etc.*

A silicon controlled rectifier acts as a true electronic switch. It can change alternating current into direct current and at the same time can control the amount of power fed to the load. Thus SCR combines the features of a rectifier and a transistor.

4.1.1 SCR Construction

When a *p-n* junction is added to a n-p-n transistor, the resulting three *p-n* junction device is called a silicon controlled rectifier. Fig. 4.1 (a) shows its construction. Hence SCR is essentially an ordinary diode (pn) and a junction transistor (npn) combined in one unit to form pnpn device. Three terminals are taken, one from the outer *p-type* material called *anode A*, second from the outer *n-type* material called *cathode K* and the third from the base of transistor section and is called *gate* G. In the normal operating conditions of SCR, anode is held at high positive potential *w.r.t.* cathode and gate at small positive potential w.r.t. cathode. Fig. 4.1 *(b)* shows the symbol of *SCR.*

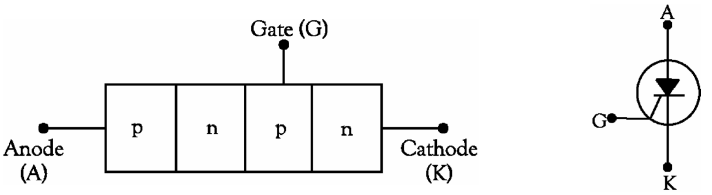


Figure 4.1 *(a) SCR structure* *(b) SCR symbol*

The silicon controlled rectifier is a solid state equivalent of vacuum tube thyratron. The gate, anode and cathode of SCR correspond to the grid, plate and cathode of thyratron. For this reason, SCR is sometimes called *thyristor.*

4.1.2 SCR Basic Operation

In a silicon controlled rectifier, load is connected in series with anode. The anode is always kept at positive potential w.r.t. cathode.

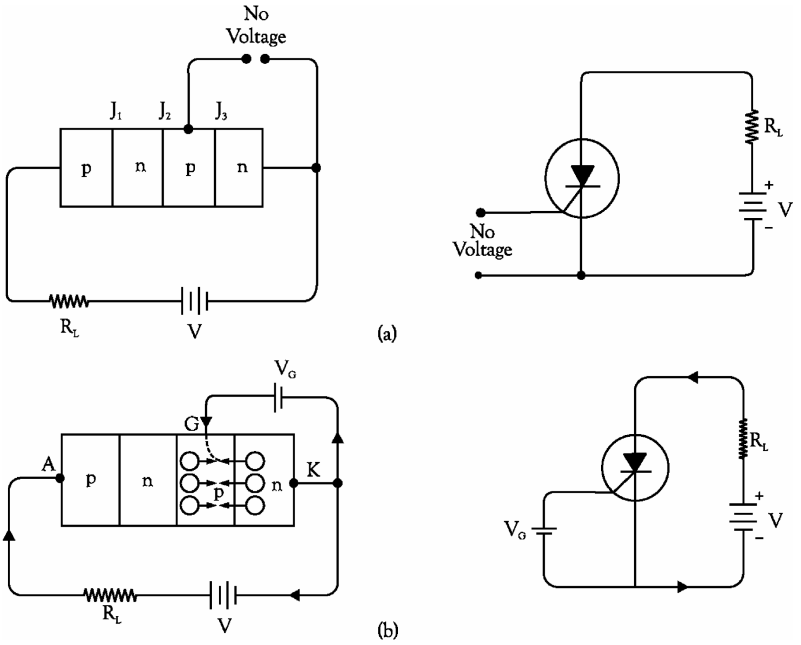


Figure 4.2 *SCR operation*

The working of SCR can be studied under the following two conditions.

(i) When gate is open: Fig. 4.2 shows the SCR circuit with gate is open i.e. no voltage applied to the gate. Under this condition, junction J_2 is reverse biased while junctions J_1 and J_3 are forward biased. Hence, the situation in the junctions J_1 and J_3 is just as in a npn transistor with base open. Consequently, no current flows through the load R_L and the SCR becomes cut-off.

However, if the applied voltage is gradually increased, a stage is reached when reverse biased junction J_2 breaks down. The SCR now conducts heavily and is said to be in the ON state. The applied voltage at which SCR conducts heavily without gate voltage is called *Breakover voltage*.

(ii) When gate is positive w.r.t. cathode: The SCR can be made to conduct heavily at smaller applied voltage by applying a small positive potential to the gate as shown in Fig. 4.2. (b). Now junction J_3 is forward biased and junction J_2 is reverse biased. The electrons from n-type material start moving across junction J_3 towards left whereas holes from p-type meterial towards the right. Consequently, the electrons from junction J_3 are attracted across junction J_2 and gate current starts flowing. As soon as the gate current flows, anode current increases. The increased anode current in turn makes more electrons available at junction J_2. This process continues and within an extremely small time, junction J_2 breaks down and the SCR starts conducting heavily. Once SCR starts conducting, the gate terminal loses all control. Even if gate voltage is removed, the anode current does not decrease at all. The only way to stop conduction (i.e. bring SCR in to OFF condition) is to reduce the applied voltage to zero.

Conclusion: The following conclusions are drawn from the working of SCR:

(i) An SCR has two states i.e. either it does not conduct or it conducts heavily. There is no intermediate state in between. Therefore, SCR behaves like a switch.

(ii) There are two ways to turn ON the SCR. The first method is to keep the gate open and make the supply voltage equal to the breakover voltage. The second method is to operate SCR with supply voltage less than breakover voltage and then turn it ON by means of a small voltage (typically 1.5 V, 30 mA) applied to the gate.

(iii) Applying small positive voltage to the gate is the normal way to turn ON an SCR because the breakover voltage is usually much greater than supply voltage.

(iv) To switch-off the SCR (i.e. to make it non-conducting), reduce the supply voltage to zero.

4.1.3 SCR Equivalent Circuit

The SCR shown in Fig. 4.3 (i) can be visualized as separated into two transistors as shown in Fig. 4.3 (ii). Thus, the equivalent circuit of SCR is composed of one pnp transistor and one npn transistor connected as shown in Fig. 4.3. (iii). It is clear that the collector of each transistor is coupled to the base of the other, thereby making a positive feedback loop.

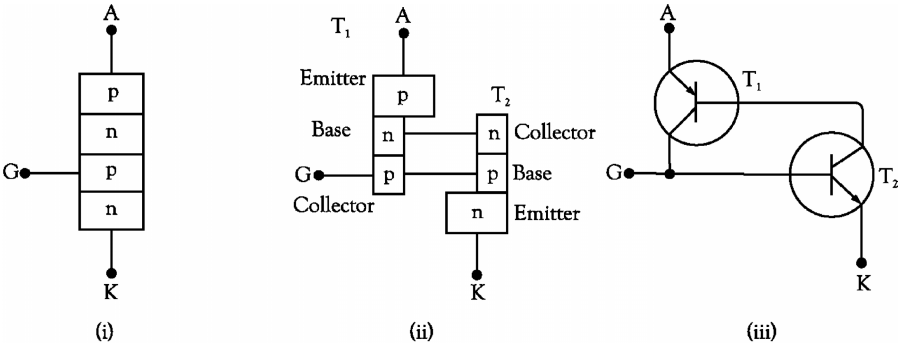


Figure 4.3 *Equivalent circuits of SCR*

The working of SCR can be easily explained from its equivalent circuit. Fig. 4.4. shows the equivalent circuit of SCR with supply voltage V and load resistance R_L. Assume the supply voltage V is less than breakover voltage as is usually the case.

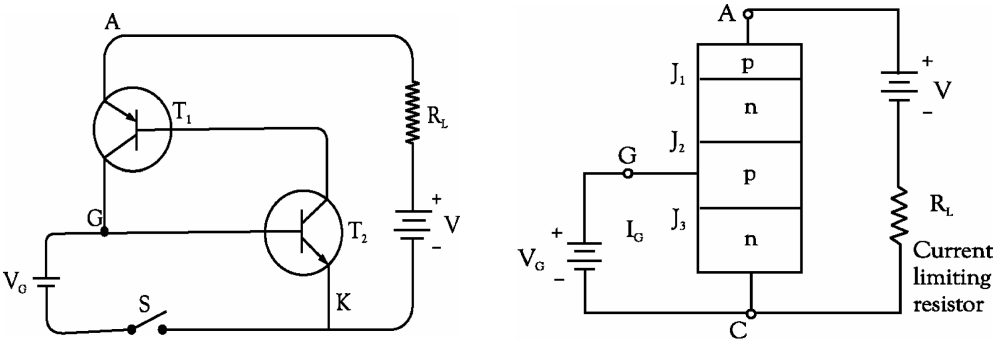


Figure 4.4 *Equivalent circuit of SCR with biasing*

With gate is open (i.e. switch S is open), there is no base current in transistor T_2. Therefore, no current flows in the collector of T_2 and hence that of T_1. Under such conditions, the SCR switches OFF. However, if switch S is closed, a small gate current will flow through the base of T_2 which increases its collector current. The collector current of T_2 is the base current of T_1. Therefore, collector current of T_1 increases, which increases the base current of T_2. This action is accumulative since an increase of current in one transistor causes an increase of current in the other transistor. As a result of this action, both transistors (Fig. 4.4) are driven to saturation, and heavy current flows through the load R_L. Under such conditions, the SCR is said to be switched ON.

4.1.4 SCR Characteristics

The V-I characteristics of an SCR is the curve between anode-cathode voltage *(V)* and anode current *(I)*, at constant gate current. Fig. 4.5 shows the V-I characteristics of a typical SCR.

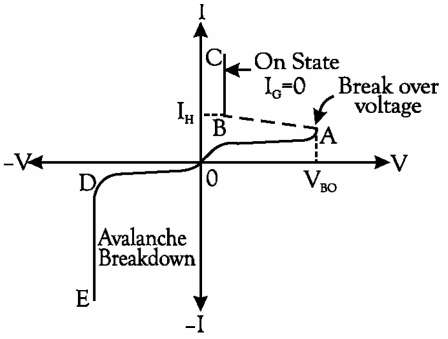


Figure 4.5 *SCR characteristics*

(i) Forward characteristics: When anode is positive w.r.t. cathode, the curve between V and I is called the forward characteristic. In Fig. 4.5, OABC is the forward characteristic of SCR at gate current I_g = 0. If the supply voltage is increased from zero, a point is reached (point A) when the SCR starts conducting. Under this condition, the voltage across SCR suddenly drops as shown by dotted curve AB and most of supply voltage appears across the load resistance R_L. If proper gate current is made to flow, SCR can **switch ON** at much smaller supply voltage. In SCR forward characteristic curve, the region OA is called **forward blocking region** or cut-off region, AB is called negative resistance region, and BC is called saturation region or ON state. The forward voltage corresponding to point A is called breakover voltage (V_{BO}) and the corresponding current is called breakover current (I_{BO}). The current corresponding to point B is called **Holding current** (I_H) and corresponding voltage is called Holding voltage (V_H). If the forward current I falls below than holding current level, then depletion region begins to develop around J_2 and the SCR goes forward blocking region. When SCR turned ON from OFF state, the resulting forward current is called **latching current**. The latching current is always slightly higher than holding current.

(ii) Reverse characteristics: When anode is negative w.r.t. cathode, the curve between V and I is known as reverse characteristic. If the reverse voltage is gradually increased, at first the anode current remains small (i.e. leakage current) and at some reverse voltage, avalanche breakdown occurs and the SCR starts conducting heavily in the reverse direction as shown by the curve DE. This maximum reverse voltage at which SCR starts conducting heavily is known as reverse breakdown voltage.

4.1.5 SCR Control Circuits: SCR Switch & Rectifier Circuits

(1) SCR as a Switch:

Fig. 4.6 shows the circuit for SCR as a switch. The SCR has only two states, namely : ON state and OFF state and there is no other state in between. When appropriate gate current is passed, the SCR starts conducting heavily and remains in this position indefinitely even if gate voltage is removed. This corresponds to the ON condition. However, when the anode current is reduced to the holding current, the SCR is turned OFF. This behaviour of SCR is allowed it to use as electronic switch.

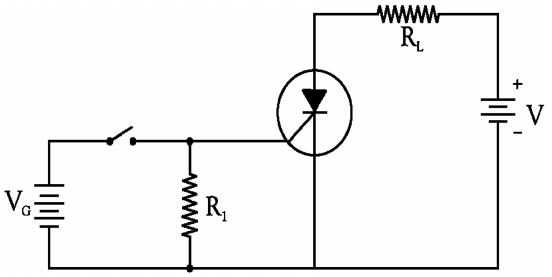


Figure 4.6 *SCR as a switch*

Advantages of SCR as a switch: An SCR has the following advantages over a mechanical or electromechanical switch (relay):

(i) It has no moving parts. Consequently, it gives noiseless operation at high efficiency.

(ii) The switching speed is very high up to 10^9 operations per second.

(iii) It permits control over large current (30-100 A) in the load by means of a small gate current (a few mA).

(iv) It has small size and gives trouble free service.

(2) SCR as a Rectifier:

(a) SCR as Half-wave rectifier: An SCR can be used as controlled half-wave rectifier as shown in Fig. 4.7. To distinguish between an ordinary half-wave rectifier using diode and SCR half-wave rectifier, an ordinary half-wave rectifier will conduct full positive half-cycle, where as an SCR half-wave rectifier can be made to conduct full or part of a positive half-cycle by proper adjustment of the gate current. Therefore, an SCR can control power fed to the load and hence is called controlled rectifier.

In SCR half-wave rectifier, the a.c. supply to be rectified is supplied through the transformer. The load resistance R_L is connected in series with the anode. A variable resistance 'r' is inserted in the gate circuit to control the gate current.

Operation: The a.c. supply to be converted into d.c. supply is applied to the primary of the transformer. Suppose the peak inverse voltage appearing across secondary is less than the reverse breakdown voltage of the SCR, then this condition ensures that SCR will not breakdown during negative half-cycles of a.c. supply. The circuit action is as follows:

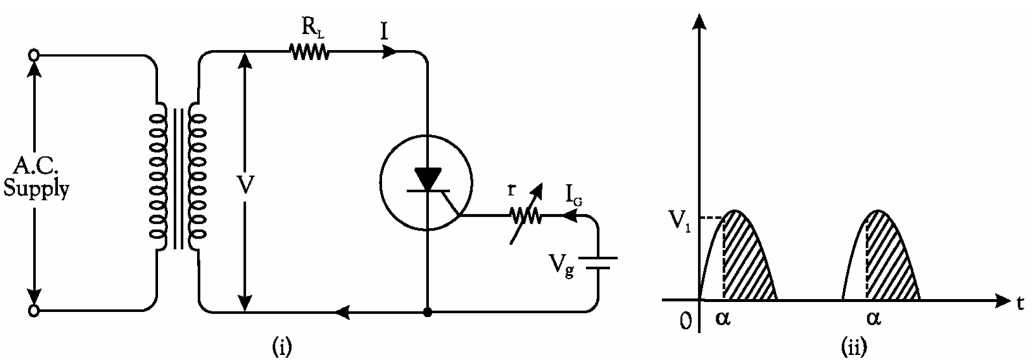


Figure 4.7 *Half-wave rectifier using SCR : (i) Circuit, (ii) output waveform*

(i) During the negative half-cycles of a.c. voltage appearing across secondary, the SCR does not conduct regardless of the gate voltage. It is because in this condition, anode is negative w.r.t. cathode and also peak inverse voltage (PIV) is less than the reverse breakdown voltage.

(ii) The SCR will conduct during the positive half-cycles provided proper gate current is made to flow. The greater the gate current, the lesser the supply voltage at which SCR is turned ON. The gate current can be changed by the variable resistance r as shown in Fig. 4.7 (i).

(iii) Suppose that gate current is adjusted to such a value that SCR switches ON at a positive voltage V_1 which is less than the peak voltage V_p. Referring to Fig. 4.7 (ii), it is clear that SCR will start conducting when secondary a.c. voltage becomes V_1 in the positive half-cycle. Beyond this, the SCR will continue to conduct till voltage becomes zero at which point it is turned OFF. Again at the start of the next positive half-cycle, SCR will start conducting when secondary voltage becomes V_1.

(iv) Referring to Fig. 4.7 (ii), it is clear that firing angle is α, i.e. at this angle in the positive half-cycle, SCR starts conduction. The conduction angle is ϕ (= $180^\circ - \alpha$).

(b) SCR Full-wave Rectifier: Fig. 4.8 (i) shows the circuit of SCR full-wave rectifier. It is exactly like an ordinary centre-taped rectifier circuit except that the two diodes have been replaced by two SCRs. The gates of both SCRs get their supply from two gate controls. One SCR conducts during the positive half-cycle and the other during the negative-half-cycle. Consequently, full-wave rectified output is obtained across the load.

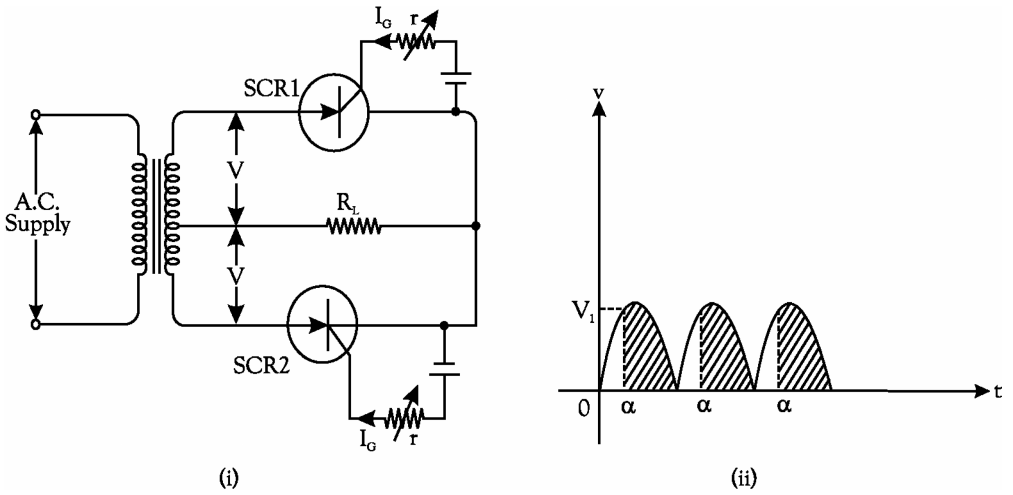


Figure 4.8 *Full-wave rectifier using SCR : (i) Circuit , (ii) output waveform*

Operation: The angle of conduction can be changed by adjusting the gate currents. Suppose the gate currents are so adjusted that SCRs conduct as the secondary voltage (across half winding) becomes V_1.

(i) During the positive half-cycle of a.c. across secondary, the upper end of secondary is positive and the lower end is negative. This will cause SCR1 to conduct. However, the conduction will start only when the voltage across the upper half of secondary becomes V_1 as shown in Fig. 4.8

(ii) In this way only shaded portion of positive half-cycle will pass through the load.

(iii) During the negative half-cycle of a.c. input, the upper end of secondary becomes negative and the lower end becomes positive. This will cause SCR2 to conduct when the voltage across the lower half of secondary becomes V_1. It may be seen that current through the load is in the same direction (d.c.) on both half-cycles of input a.c. The advantage of this circuit over ordinary full-wave rectifier circuit is that by adjusting the gate currents, we can change the conduction angle and hence the output voltage.

4.1.6 Other Applications of SCR

(1) SCR as Light Detector:

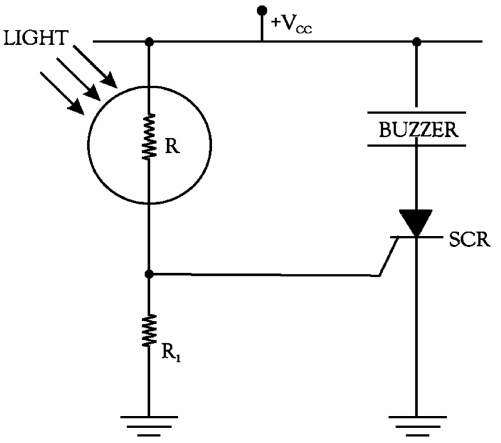


Figure 4.9 *Circuit diagram of SCR light detector*

Fig. 4.9 shows the use of SCR for overlight detection. The resistor R is a photo-resistor, a device whose resistance decreases with the increase in light intensity. When the light falling on R has normal intensity, the value of R is high enough and the voltage across R_1 is insufficient to trigger the SCR. However, when R is in strong light, its resistance decreases and the voltage drop across R_1 becomes high enough to trigger the SCR. Consequently, the buzzer sounds the alarm. It may be noted that even if the strong light disappears, the buzzer continues to sound the alarm. It is because once the SCR is fired, the gate loses all control.

(2) Crowbar Circuit using SCR:

SCR is used as crowbar circuit to protect a load against an overvoltage from a power supply. The Fig. 4.10 shows the crowbar circuit using SCR. In the circuit, a positive supply of 20 V is connected to a Zener diode in series with a resistor. The voltage across the resistor drives the gate of an SCR, which is in parallel with the load. The Zener voltage is 21 V. As long as the supply voltage is 20 V, the Zener diode is open and the SCR gate voltage is zero. Since the SCR is open, 20 V appears across the load resistor.

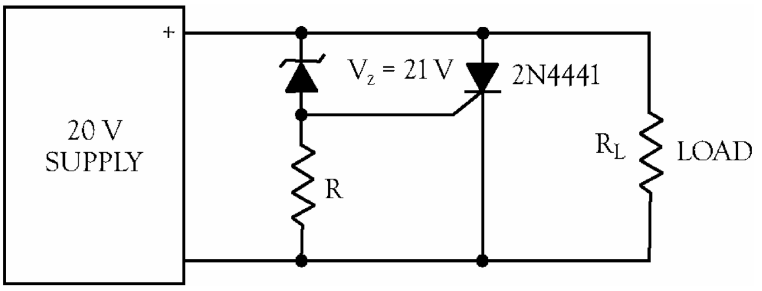


Figure 4.10 *SCR crowbar circuit*

If some thing goes wrong with the power supply and the voltage tries to rise above 21 V, the Zener diode breaks down, and a voltage appears at the gate of the SCR. When this voltage exceeds approximately 0.7 V, the SCR latches (switchs ON) and shorts out the load voltage. The action is similar to throwing a crowbar across the load terminals. Because the turn ON time of SCR is very fast (t ≈1μs), the load is quickly protected against the damaging effects of a large overvoltage. Crowbar circuit using SCR protects many digital ICs from the overvoltage.

4.2 UNIJUNCTION TRANSISTOR (UJT)

A unijunction transistor (abbreviated as UJT) is a three terminal semiconductor switching device. This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply. Due to this characteristic, the unijunction transistor can be employed in a variety of applications like switching, pulse generator, saw-tooth generator etc.

4.2.1 UJT Construction

A UJT consists of an *n-type* silicon bar with an electrical connection on each end. The leads to these connections are called base leads, base-one B_1 and base-two B_2. Along the bar, closer to B_2, a p-n junction is formed between a p-type emitter and the n-type bar. The lead to this junction is called the *emitter lead E* (as shown in Fig. 4.11 (i)). Fig. 4.11 (ii) shows the symbol of unijunction transistor. Note that emitter is shown closer to B_2 than B_1. The following points are worth considering:

(i) Since the device has one *p-n* junction and three leads, it is commonly called a unijunction transistor (*uni* means single).

(ii) With only one *p-n junction,* the device is a new form of diode. Because the two base terminals are taken from one section of the diode, this device is also called *double-based diode.*

(iii) The emitter region is heavily doped having many holes as charge carriers. The *n* region (n-type bar), is lightly doped. For this reason, the resistance between the base terminals is very high (5 to 10 KΩ) when emitter lead is open.

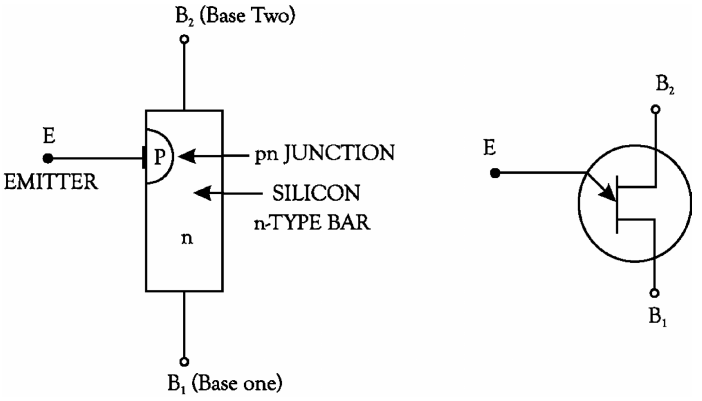


Figure 4.11 *Unijunction Transistor (i) Construction (ii) Symbol*

4.2.2 UJT Operation

Fig. 4.12 shows the basic circuit for the operation of a unijunction transistor. Normally the terminal B_2 is kept positive w.r.t. B_1 by means of a battery V_{BB}.

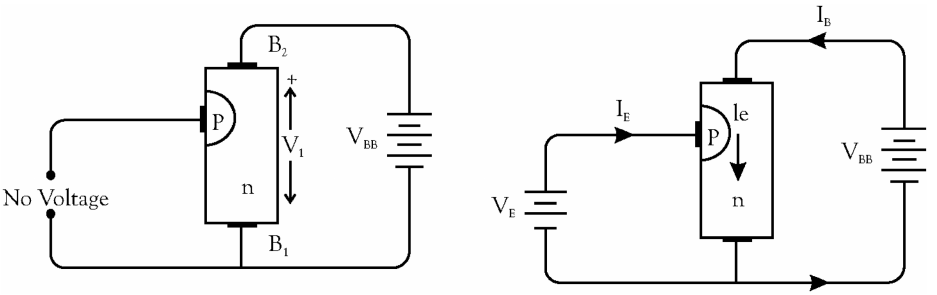


Figure 4.12 *UJT operation (i) Without emitter voltage, (ii) With emitter voltage*

(i) If voltage V_{BB} is applied between B_2 and B_1 with emitter open as shown in Fig. 4.12 (i), a voltage gradient is established along the n-type bar. Since the emitter is located nearer to B_2, more than half of V_{BB} appears between the emitter and B_1. The voltage V_1 between emitter and B_1 establishes a reverse bias on the p-n junction and the emitter current is cut off. Of course, a small amount of leakage current flows from B_2 to emitter due to minority charge carriers.

(ii) If a positive voltage is applied at the emitter as shown in Fig. 4.12 (ii), the p-n junction will remain reverse biased so long as the input voltage is less than V_1. If the input voltage to the emitter exceeds V_1, the p-n junction becomes forward biased. Under these conditions, holes are injected from p-type material into the n-type bar. These holes are repelled by positive B_2 terminal and they are attracted towards B_1 terminal of the bar. This accumulation of holes in the emitter to B_1 region results in the decrease of resistance in this section of the bar. The

result is that internal voltage drop from emitter to B_1 decreased and hence the emitter current I_E increases. As more holes are injected, a condition of saturation will eventually be reached. At this point, the emitter current is limited by emitter power supply only. The device is now in the ON state.

(iii) If a negative pulse is applied to the emitter, the p-n junction is reverse biased and the emitter current is cut off. The device is then said to be in the OFF state.

Equivalent Circuit of a UJT

Fig. 4.13 shows the equivalent circuit of a UJT. The resistance of the silicon bar is called the inter-base resistance R_{BB}. The inter-base resistance is represented by two resistors in series:

(a) R_{B2} is the resistance of silicon bar between B_2 and the point at which the emitter junction lies.

(b) R_{B1} is the resistance of the bar between B_1 and emitter junction. This resistance is shown variable because its value depends upon the bias voltage across the p-n junction. The p-n junction is represented by a diode D.

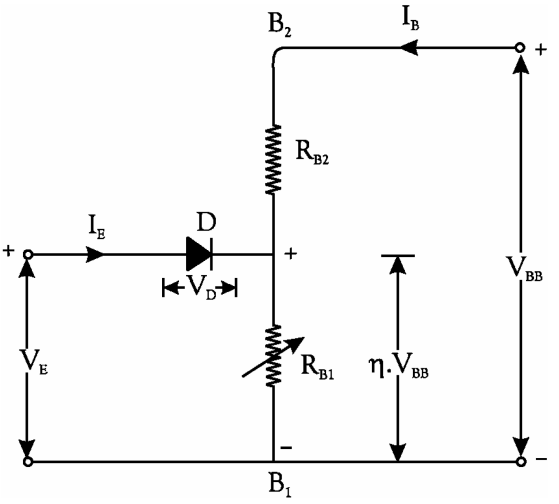


Figure 4.13 *Equivalent circuit of UJT*

The circuit action of a UJT can be explained more clearly from its equivalent circuit.

(i) With no voltage applied to the UJT, the inter-base resistance is given by :

$$R_{BB} = R_{B1} + R_{B2}$$

The value of R_{BB} generally lies between 4 KΩ and 10 KΩ,

(ii) If a voltage V_{BB} is applied between the bases B_1 and B_2 with emitter open, the voltage will divide up across R_{B1} and R_{B2}.

Voltage across R_{B1} is obtained by voltage division rule,

$$V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB}$$

$$V_1 / V_{BB} = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

The ratio V_1/V_{BB} is called intrinsic stand-off ratio and is represented by Greek letter η.

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} \quad ...(4.1)$$

The value of η usually lies between 0.51 and 0.82.

$\therefore$ Voltage across $R_{B1} = \eta V_{BB}$

The voltage ηV_{BB} appearing across R_{B1} reverse biases the diode. Therefore, the emitter current is zero.

(iii) If now a progressively rising positive voltage is applied to the emitter, the diode will become forward biased when input voltage exceeds ηV_{BB} by V_D, the forward voltage drop across the silicon diode i.e.

$$V_P = \eta V_{BB} + V_D \quad ...(4.2)$$

Where V_P = peak point voltage & V_D = forward voltage drop across silicon diode ($\approx$ 0.7V)

When the diode D starts conducting, holes are injected from p-type material to the n-type bar. These holes are swept down towards the terminal B_1. This decreases the resistance between emitter and B_1 (indicated by variable resistance symbol for R_{B1}) and hence the internal drop from emitter to B_1. The emitter current now increases regeneratively until it is limited by the emitter power supply.

4.2.3 UJT Characteristics

Fig. 4.14 shows the curve between emitter voltage (V_E) and emitter current (I_E) of a UJT at a given voltage V_{BB} between the bases. This is known as the emitter characteristic of UJT.

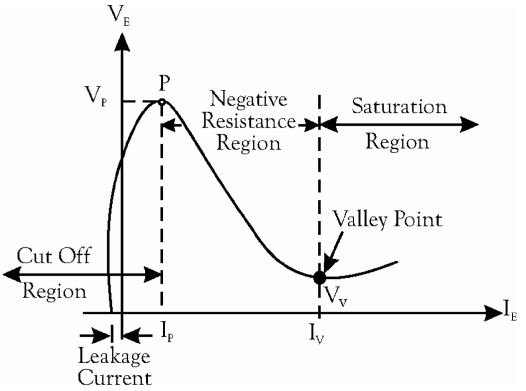


Figure 4.14 *UJT characteristics*

The following points may be noted from the characteristics:

(i) Initially, in the cut-off region, as V_E increases from zero, slight leakage current flows from terminal B_2 to the emitter. This current is due to the minority charge carriers in the reverse biased diode.

(ii) Above a certain value of V_E forward current I_E begins to flow, increasing until the peak voltage V_P and current I_P are reached at point P and the point P is called peak point.

(iii) After the peak point P, any attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This is a negative resistance portion of the curve because with increase in I_E, V_E decreases. The device, therefore, has a negative resistance region which is stable enough to be used with a great deal of reliability in many areas e.g., trigger circuits, sawtooth generators, timing circuits etc.

(iv) The negative portion of the curve lasts until the valley point V is reached with valley – point voltage V_V and valley-point current I_v. After the valley point, the device is driven to saturation.

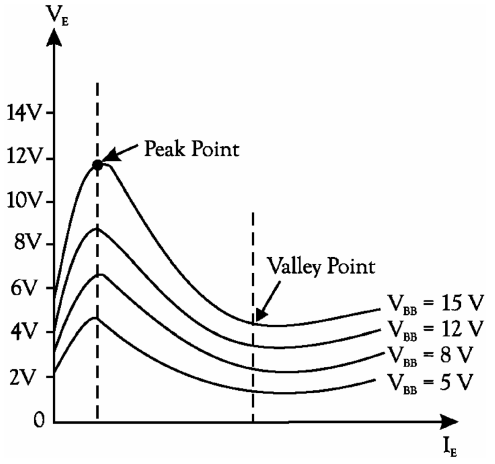


Figure 4.15 *UJT characteristics at different I_{BB}*

Fig. 4.15 shows the typical family of V_E/I_E characteristics of a UJT at different voltages between the bases. It is clear that peak - point voltage (= ηV_{BB}+ V_D) falls steadily with reducing V_{BB} and so does the valley point voltage V_V. The difference V_P - V_V is a measure of the switching efficiency of UJT and can be seen to fall off as V_{BB} decreases. For a general purpose UJT, the peak - point current is of the order of 1μA at V_{BB} =20 V with a valley - point voltage of about 2.5 V at 6 mA.

Advantages of UJT

The UJT was invented in 1948 but did not become commercially available until 1952. Since then, the device has achieved great popularity due to the following reasons:

(i) It is a low cost device.

(ii) It has excellent characteristics with negative resistance region.

(iii) It is a low-power absorbing device under normal operating conditions.

Due to above reasons, this device is being used in a variety of applications, which include oscillators, trigger circuits, saw-tooth generators, bistable network etc.

4.2.4 UJT Applications

Unijunction transistors are used extensively in oscillator, pulse and voltage sensing circuits.

UJT Saw Tooth generator

Fig. 4.16 shows UJT relaxation oscillator where the discharging of a capacitor through UJT can develop a saw-tooth output voltage as shown.

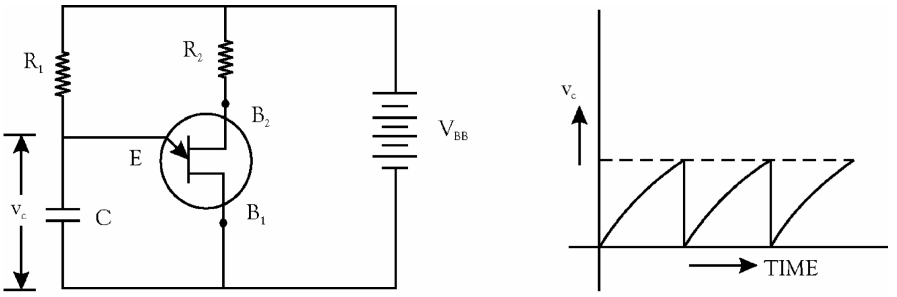


Figure 4.16 *UJT saw tooth generator*

When battery V_{BB} is turned on, the capacitor C charges through resistor R_1. During the charging period, the voltage across the capacitor rises in an exponential manner until it reaches the peak -point voltage(V_p). At this instant of time, the UJT switches ON and the capacitor is discharged through low resistance path between E and B_1. As the capacitor voltage decreases to zero, the emitter ceases to conduct and the UJT is switched OFF. The next cycle then begins, allowing the capacitor C to charge again. The frequency of the output saw-tooth wave can be varied by changing the value of R_1 since this controls the time constant R_1C of the capacitor charging circuit.

Frequency of Oscillation: The time period and hence the frequency of the saw-tooth wave can be calculated as follows : Assuming that the capacitor is initially uncharged, the voltage V_C across the capacitor prior to breakdown is given by

$$V_C = V_{BB}\left(1 - e^{-t/R_1C}\right) \qquad ...(4.3)$$

where R_1C = charging time constant of resistor-capacitor circuit, t = time from the commencement of wave form.

The discharge of the capacitor occurs when V_C is equal to the peak-point voltage ($V_P = \eta\ V_{BB}$).

$$\eta V_{BB} = V_{BB}\left(1 - e^{-t/R_1C}\right)$$

$$\eta = 1 - e^{-t/R_1C}$$

$$e^{-t/R_1C} = 1 - \eta$$

$$t = R_1C \log_e \frac{1}{1 - \eta}$$

$\therefore$ Time period, $$T = 2.303\, R_1C \log_{10} \frac{1}{1 - \eta} \quad \text{...(4.4)}$$

The expression for output frequency is f = 1/T.

UJT Overvoltage Indicator

Fig. 4.17 shows a simple d.c. over-voltage indicator. A warning pilot - lamp L is connected to the emitter and B_1 path as shown in Fig. 4.17. So long as the input voltage is less than the peak-point voltage (V_p) of the UJT, the device remains switched OFF. However, when the input voltage exceeds V_p, the UJT is switched ON and the capacitor discharges through the low resistance path between terminals E and B_1. The current flowing in the pilot lamp L lights it, thereby indicating the overvoltage in the circuit.

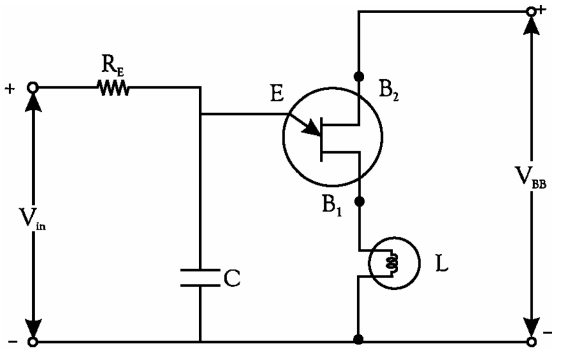


Figure 4.17 *UJT overvoltage indicator*

4.3 JUNCTION FIELD EFFECT TRANSISTORS

Field Effect Transistor (FET) is a three terminal unipolar semiconductor device in which current is controlled by externally applied voltage. Hence FET is a **voltage controlled device** unlike BJT, which is a current controlled device. In the FET, the operation depends on the flow of majority carriers only and hence FET is a **uni-polar** device. There are two types of FETs. They are:

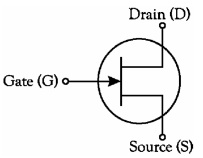
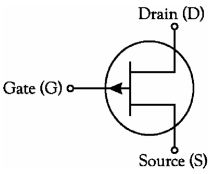
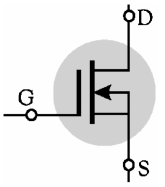
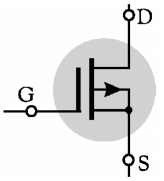
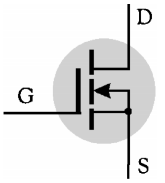
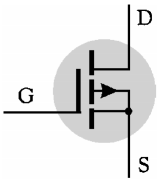
(a) Junction Field Effect Transistor (JFET)

(b) Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)

JFETs are further divided in to two types as P-channel JFET and N-channel JFET

MOSFETs are further divided in to Depletion-Enhancement MOSFET (D-E MOSFET) and Enhancement only MOSFET (E-MOSFET). Each type is further divided into N-channel and P-channel device as in JFET.

Symbol:

S. No.	Device	Symbol
1	N-type JFET	
2	P-Type JFET	
3	N-type DE MOSFET	
4	P-type DE MOSFET	
5	N-type E MOSFET	
6	P-type E MOSFET	

4.3.1 JFET Construction

(a) N-type JFET Construction

The structure of N-type FET is shown in Fig. 4.18 (a). It consists of an N-type semiconductor bar sandwiched between two heavily doped P-type regions formed by alloying or diffusion. These P-regions forms two P-N junctions and are internally connected and a single lead is brought out which is called **Gate** terminal. Ohmic contacts are made at the two ends of the N-type semiconductor bar. Thus the n-type bar forms a sort of **channel** through which the current flows from one end to other end on application of potential difference between the ends. One end of the channel is called **Source** terminal and the other is called the **Drain** terminal as shown in the Fig. 4.18 (a). In N-type JFET, the channel is N-type and hence during the applied potential difference, the current flowing between Drain and Source is due to electrons. In JFET, the Source and Drain terminals can be interchanged.

The Source Terminal: The source S is the terminal through which the majority carriers enters the bar. The current flowing through channel at Source S is denoted as I_S.

The Drain Terminal: The drain is a terminal through which the majority carriers leave the bar. The current flowing through channel at drain D is denoted as I_D. The voltage applied between drain and source is denoted as V_{DS}.

The Gate Terminal: The heavily doped P-region on both sides of the channel form the control electrode called Gate G. A negative voltage V_{GS} is applied between Gate and Source to reverse bias the P-N junction. The Source, Gate and Drain works like a controlled water tap as shown in Fig. 4.18. (b).

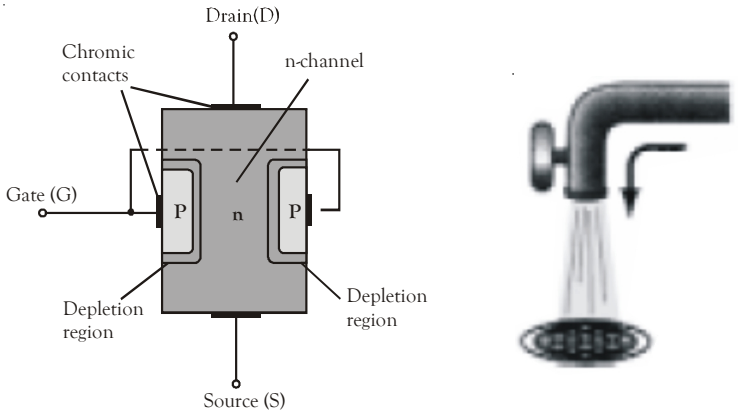


Figure 4.18 *(a) N-type junction field-effect transistor (N-JFET)*
(b) Water tap equivalent model of JFET

(b) P-type JFET Construction:

The structure of P-type FET is shown in Fig. 4.19. It consists of a P-type semiconductor bar sandwiched between two heavily doped N-type regions formed by alloying or diffusion. These N-regions form two N-P junctions and are internally connected and a single lead is brought out which is called

Gate terminal. Ohmic contacts are made at the two ends of the P-type semiconductor bar. Thus the P-type bar forms a sort of **channel** through which the current flows from one end to other on application of potential difference between the ends. One end of the channel is called **Source** terminal and the other is called the **Drain** terminal as shown in the Fig. 4.19.

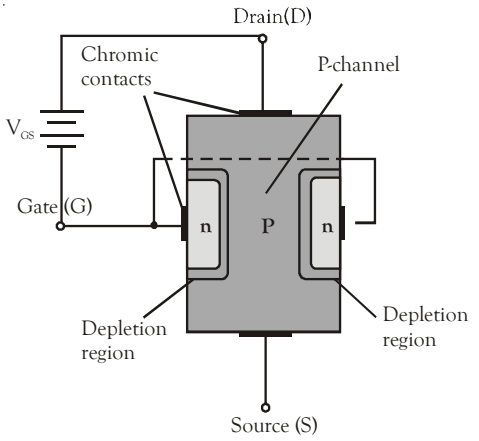


Figure 4.19 *p-type junction field-effect transistor (p-JFET)*

4.3.2 Theory of Operation

The p-n junction between Gate and Source is always reverse biased by means of V_{GS} so that the current flowing through Gate terminal is extremely low and practically considered as zero. If we apply some voltage (V_{DD}) between Drain and Source, the Drain current I_D passes through the channel between Drain and Source. If we increase the negative voltage on Gate with respect to Source (V_{GS}), the reverse bias increases and hence the width of depletion region (also called space charge region) within the channel increases. Thus in JFET, by varying reverse voltage on P-N junction we can vary the width of semiconductor channel and hence the Drain current I_D can be controlled.

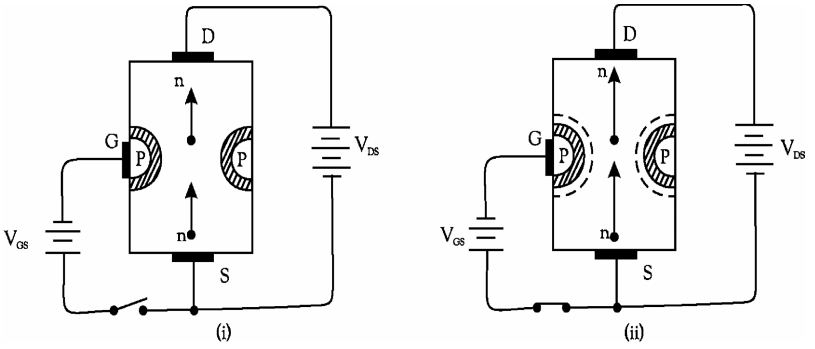


Figure 4.20 *Operation of JFET*

Fig. 4.20 shows the circuit of n-channel JFET with normal polarities. The circuit action is as follows:

(i) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero as shown in Fig. 4.20 (i), the two p-n junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(ii) When a reverse voltage V_{GS} is applied between the gate and source as shown in Fig. 4.20 (ii), the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain.

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate. For this reason, the device is called field effect transistor. It may be noted that a p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

4.3.3 JFET Characteristics

Output Characteristics:

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate-source voltage (V_{GS}) is known as Output characteristics of JFET. Fig. 4.21 shows the circuit for determining the output characteristics of JFET.

Keeping V_{GS} fixed at some value, say V_{GS} = 0 V using V_{GG}, the drain-source voltage (V_{DD}) is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of JFET at V_{GS} = 0V. Repeating similar procedure, output characteristics at various gate-source voltages say V_{GS} = –1 V, V_{GS} = – 2 V, V_{GS} = – 3 V, and V_{GS} = – 4 V can be drawn. Fig. 4.22(a) shows a family of output characteristics.

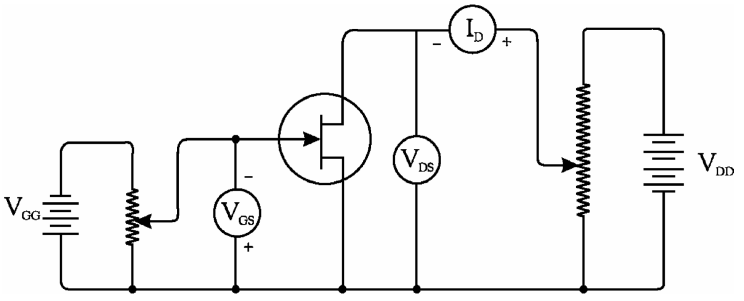


Figure 4. 21 *Circuit for determining the output characteristics of JFET*

The following points may be noted from the characteristics :

(i) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as pinch-off voltage.

(ii) After pinch-off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch-off voltage. Consequently, drain current remains constant.

(iii) When the V_{DS} is increased further, the reverse biased gate-channel (P–N junction) undergoes avalanche breakdown and small changes in V_{DS} produces very large change in I_D.

(iv) The characteristics resemble that of a pentode valve.

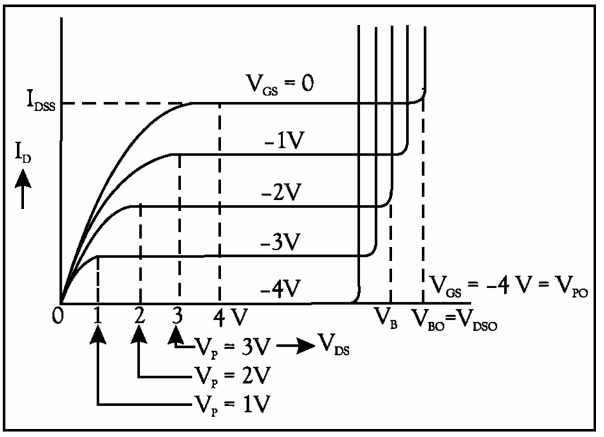


Figure 4.22 *(a) shows the drain characteristics*

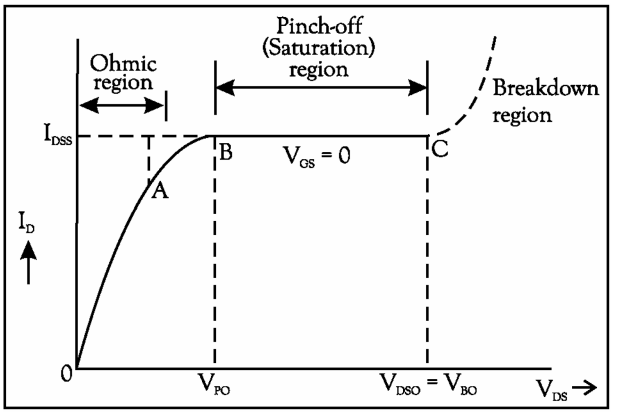


Figure 4.22 *(b) JFET characteristics when V_{GS} = 0*

The JFET characteristics when V_{GS} = 0 is shown in detail in Fig. 4.22(b). The output characteristic curve can be divided into following four regions:

(1) Ohmic Region OA:

This part of characteristic is linear. The drain current increases linearly with the increase in drain- to-source voltage, obeying Ohm's law. The resistance from drain to source $R_{DS} = V_{DS}/I_D$ is related to the gate voltage (V_{GS}). Thus JFET acts like **voltage dependent resistor** till point A called Knee point is reached.

(2) Curve AB:

In this region, the drain current increases at **reverse square law rate** upto point B which is called pinch-off point. This slow reduction in drain current from previous linear increase is due to growth of depletion region to a size thereby reducing the effective width of channel. The drain to source voltage V_{DS} corresponding to point B is known as **pinch-off voltage, V_P**.

(3) Pinch–off Region BC:

It is also called saturation region. In this region, the drain current remains constant at maximum value (I_{DSS}). Here, JFET operates as a **constant current source** because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases, the channel resistance R_{DS}, also increases thereby keeping I_D practically constant at I_{DSS}. The drain current in the pinch-off region depends upon the gate-to-source voltage and is given by Shockley's equation,

$$I_D = I_{DSS} (1 - (V_{GS}/V_P))^2 \qquad ...(4.5)$$

(4) Breakdown Region CD:

In this region, the drain current (I_D) increases rapidly as the drain-to-source voltage (V_{DS}) is increased due to avalanche breakdown of reverse biased gate-channel P-N junction. Hence in this region, JFET acts like **constant voltage source**.

Transfer Characteristics:

The transfer characteristic of JFET shown in Fig. 4.23. The expression for drain current is given by the Shockeley's relation,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \qquad ...(4.6)$$

where

I_D = drain current at given V_{GS}

I_{DSS} = shorted-gate drain current

V_{GS} = gate-source voltage

$V_{GS\,(off)}$ = gate-source cut-off voltage

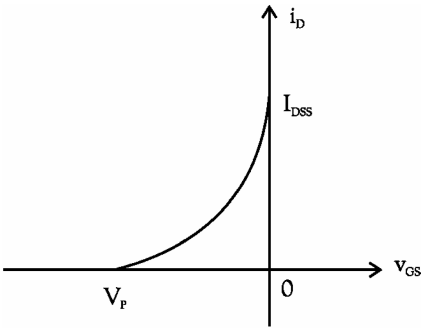


Figure 4.23 *Transfer characteristics of JFET*

Transfer curve from the drain characteristics

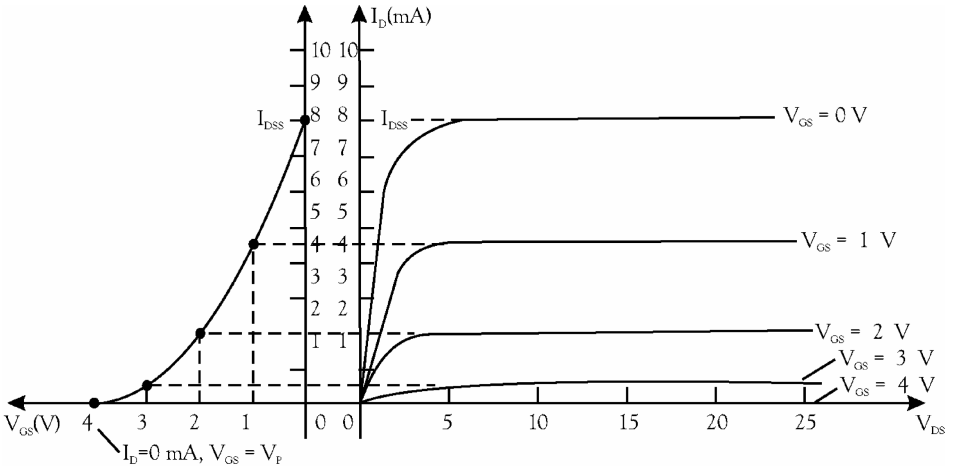


Figure 4.24 *Obtaining the transfer curve from the drain characteristics*

In the above Fig. 4.24,

When V_{GS} = 0 V, I_D = I_{DSS}.

When V_{GS} = V_P = -4 V, the drain current is zero milliamperes, defining another point on the transfer curve. That is:

When V_{GS} = V_P, I_D = 0 mA.

Using Shockley's Eqn, when V_{GS} = 0,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1-0)^2$$

$$\boxed{I_D = I_{DSS} \mid V_{GS} = 0V} \qquad ...(4.7)$$

Substituting $V_{GS} = V_P$ yields $\boxed{I_D = 0 \mid V_{GS} = V_P}$ ...(4.8)

4.3.4 JFET Parameters

(1) Drain resistance (r_d): It is the AC resistance between Drain and Source when the FET is operating in Pinch-off region. Drain resistance (r_d) is defined as the ratio between changes in V_{DS} to corresponding changes in I_D for constant V_{GS}.

$$r_d = \Delta V_{DS}/\Delta I_D \text{ when } \Delta V_{GS} = 0.$$

The drain resistance is also called output resistance of JFET.

(2) Transconductance (g_m): It is the ratio of the change in drain current (I_D) to the corresponding change in gate source voltage (V_{GS}) at constant drain-source voltage (V_{DS}).

$$g_m = \Delta I_D/\Delta V_{GS} \text{ when } \Delta V_{DS} = 0.$$

It is also called mutual conductance.

(3) Amplification factor (μ) : It is the ratio of the change in Drain-Source voltage (V_{DS}) to the corresponding Gate-Source voltage (V_{GS}) when Drain current I_D is constant.

$$\mu = \Delta V_{DS}/\Delta V_{GS} \text{ when } \Delta I_D = 0.$$

Relationship between μ, g_m, and r_d:

$$\mu = \Delta V_{DS}/\Delta V_{GS} \text{ when } \Delta I_D = 0.$$
$$= (\Delta V_{DS}/\Delta I_D) \cdot (\Delta I_D/\Delta V_{GS}) = r_d \cdot g_m$$

Thus $\mu = r_d \cdot g_m$ ...(4.9)

4.3.5 JFET Amplifications

Fig. 4.25 shows JFET amplifier circuit. The weak signal to be amplified is applied between gate and source and amplified output is obtained from the drain-source circuit. For the proper operation of JFET, the gate must be negative w.r.t. source i.e., input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by means a circuit known as Voltage divider biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

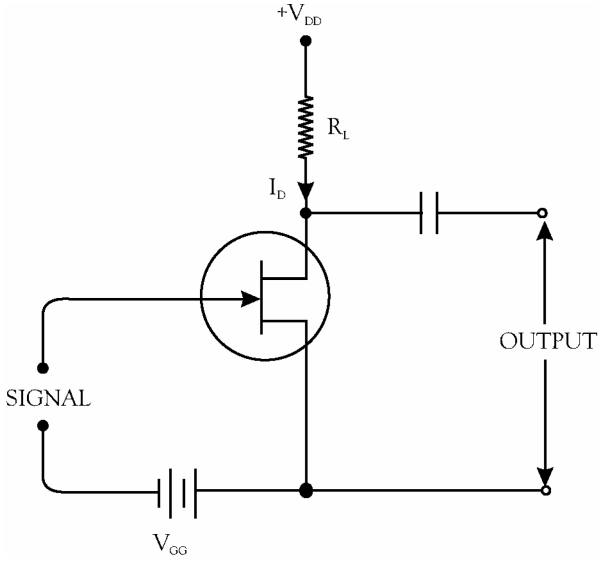


Figure 4.25 *JFET amplifier*

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes JFET capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is the small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output voltage across the load R_L. In this way, JFET acts as an amplifier.

4.3.6 JFET AC Equivalent Circuit

The ac equivalent circuit of JFET is shown in Fig. 4.26. The control of drain current I_d by Vgs is included as a current source $g_m V_{gs}$ connected from drain to source. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages.

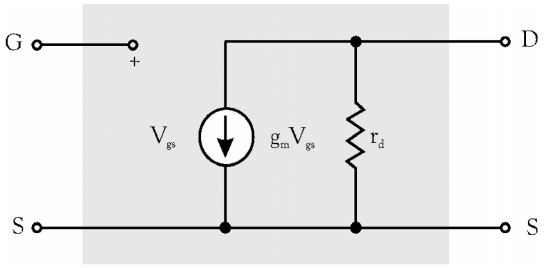


Figure 4.26 *AC equivalent circuit of JFET*

4.3.7 Advantages of FET over BJT

During 1960s, the electronics industry shifted many electronic applications from the junction transistor to the field-effect transistor (FET), which is easier to manufacture and uses much less power than the junction transistor. Some of the advantages of FET are:

(i) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(ii) The operation of a JFET depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of vacuum tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a JFET.

(iii) A JFET has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(iv) A JFET has a very high power gain. This eliminates the necessity of using driver stages.

(v) A JFET has a smaller size, longer life and high efficiency.

4.3.8 Comparison of JFET and BJT

The JFET differs from an ordinary or bipolar transistor in the following ways:

(i) In a JFET, there is only one type of charge carrier, i.e., holes in p-type channel and electrons in n-type channel are responsible for conduction. For this reason, it is also called a unipolar transistor. However, in BJT, both holes and electrons are responsible for conduction. Therefore, an ordinary transistor is called a bipolar transistor (BJT).

(ii) As the input circuit (i.e., gate to source) of a JFET is reverse biased, it has high input impedance. However, the input circuit of BJT is forward biased and hence has low input impedance.

(iii) As the gate is reverse biased, it carries very small current. Obviously, JFET is just like a vacuum tube where control grid (corresponding to gate in JFET) carries extremely small current and input voltage controls the output current. Hence, JFET is also called a **voltage-controlled** device. However, BJT is a current controlled device i.e., input current controls the output current.

(iv) A BJT uses base current to control a large current between collector and emitter whereas a JFET uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterized by current gain whereas the JFET gain is characterized as a transconductance i.e., the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In JFET, there are no junctions along the channel between drain and gate, as in BJT. The conduction is through an n- type or p-type semi-conductor material. For this reason, noise level in JFET is very small.

(vi) The JFET is relatively immune to radiation where as BJT is very sensitive to radiation due to the fact that β is practically affected.

(vii) JFET has greater thermal stability than BJT.

(viii) The power gain of JFET is much larger than that of BJT at audio frequencies.

(ix) JFET has negative temperature co-efficient at high current levels. It means that the current decreases as temperature increases. This characteristic prevents the JFET from thermal breakdown. BJT, on other hand, has positive temperature co-efficient at high current levels. Hence collector current increases with increase in temperature, which leads thermal breakdown.

(x) Some of the device parameters of JFET and BJT are given below:

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\,A$	$\Leftrightarrow$	$V_{BE} \cong 0.7\,V$

4.3.9 FET Applications

The high input impedance and low output impedance and low noise level make JFET far superior to the bipolar transistor. Some of the circuit applications of JFET are:

(i) **As a buffer amplifier:** A buffer amplifier is a stage of amplification that isolates the preceding stage from the succeeding stage. Because of the high input impedance and low output impedance, a JFET can act as an excellent buffer amplifier (See Fig. 4.27). The high input impedance of JFET means light loading of the preceding stage. This permits almost the entire output from first stage to appear at the Buffer input. The low output impedance of JFET can drive heavy loads (or small load resistances). This ensures that all the output from the buffer reaches the input of the second stage.

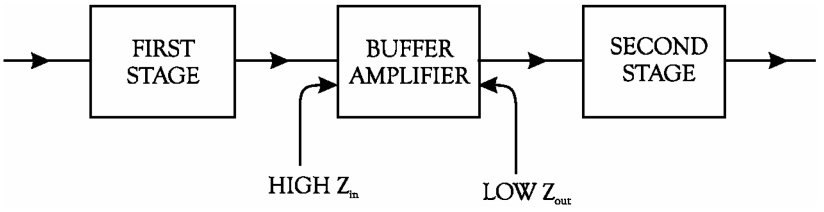


Figure 4.27 *Buffer amplifier*

(ii) **Phase-shift oscillators:** JFETs can be used to construct Phase-shift oscillator. The high input impedance of JFET minimize the loading effect in Phase-shift oscillator.

(iii) As RF amplifier: In communication electronics, we have to use JFET RF amplifier in a receiver instead of BJT amplifier for the following reasons:

(a) The noise level of JFET is very low. The JFET will not generate significant amount of noise and is thus useful as an RF amplifier.

(b) The antenna of the receiver receives a very weak signal that has an extremely low amount of current. Since JFET is a voltage controlled device, it will well respond to low current signal provided by the antenna.

SOLVED PROBLEMS

1. *The intrinsic stand-off ratio for a UJT is determined to be 0.6. If the inter-base resistance is 10 KΩ, what are the values of R_{B1} and R_{B2} ?*

Solution:

Given, $R_{BB} = 10\ K\Omega, \quad \eta = 0.6$

Now, $R_{BB} = R_{B1} + R_{B2}$

Or $10 = R_{B1} + R_{B2}$

Also $\eta = [R_{B1} / (R_{B1} + R_{B2})]$

$0.6 = R_{B1}/10$

Therefore, $R_{B1} = 10 \times 0.6 = 6\ K\Omega$ and $R_{B2} = (10 - 6)\ K\Omega = 4\ K\Omega$

2. *A unijunction transistor has 10 V between the bases. If the intrinsic stand off ratio is 0.65, find the value of stand off voltage. What will be the peak-point voltage if the forward voltage drop in the p-n-junction is 0.7 V ?*

Solution:

$V_{BB} = 10\ V, \quad \eta = 0.65, \quad V_D = 0.7\ V$

Stand off voltage $= \eta V_{BB} = 0.65 \times 10 = 6.5\ V$

Peak-point voltage $= V_P = \eta V_{BB} + V_D = 6.5 + 0.7 = 7.2\ V$

3. *A JFET has the following parameters: $I_{DSS} = 32$ mA. $V_{GS}((off) = -8$ V. $V_{GS} = -4.5$ V. Find the value of drain current.*

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 mA$$

$= 6.12$ mA

4. *A JFET has a drain current of 5 mA. If I_{DSS} = l0 mA and $V_{GS}(off)$ = - 6 V, find the value of (i) V_{GS} and (ii) V_p.*

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

or $$5 = 10\left[1 0 + \frac{V_{GS}}{6}\right]^2$$

or $$10 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707 \text{ mA}$$

$\therefore$ $$V_{GS} = -1.76\ V$$

and $$V_P = -V_{GS(off)} = 6\ V$$

5. *When V_{GS} of a JFET changes from -3.1 V to -3 V, the drain current changes from l mA to 1.3 mA. What is the value of transconductance?*

Solution:

ΔV_{GS} = 3.1 – 3 = 0.1 V, ΔI_D = 1.3 – 1 = 0.3 mA

Then Transconductance,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3\ mA}{0.1V} = 3 \text{ mA}/1\text{V} = 3000\ \mu \text{ mhos}$$

6. *The following readings were obtained experimentally from a JFET:*

V_{GS}	0 V	0 V	–0.2 V
V_{DS}	7 V	15 V	15 V
I_D	10 mA	10.25 mA	9.65 mA

Determine (i) a. c. drain resistance (ii) transconductance and (iii) amplification factor.

Solution:

(i) With V_{GS} constant at 0 V, the increase in V_{DS} from 7 V to 15 V increases the drain current From 10 mA to 10.25 mA. i.e.

Change in drain-source voltage, ΔV_{DS} = 15 - 7 = 8 V

Change in drain current, ΔI_D = 10.25 - 10 = 0.25 mA

EXERCISES

I. Descriptive Type Questions

1. Explain the construction and working of an SCR.
2. Draw the equivalent circuit of an SCR and explain its working from this equivalent circuit. *(VTU Jan 2009)*
3. Explain the terms breakover voltage, holding current and forward current rating as used in connection with SCR analysis.
4. Draw the V-I characteristics of an SCR and explain? *(VTU June 2009)*
5. Explain the action of an SCR as a switch. What are the advantages of SCR switch over a mechanical or electro-mechanical switch?
6. Discuss some important applications of SCR.
7. Explain the construction and working of a UJT. *(VTU June 2009)*
8. Draw the equivalent circuit of a UJT and discuss its working from the circuit. *(VTU Jan 2009)*
9. Describe some important applications of a UJT.
10. Write short notes on the following:
    (i) UJT Saw Tooth generator
    (ii) UJT Overvoltage Indicator
11. Explain the construction and working of a n-channel JFET. *(VTU June 2008)*
12. What is the difference between a JFET and a bipolar transistor ?
13. How will you determine the drain characteristics of JFET? What do they indicate?
14. Define the JFET parameters and establish the relationship between them.
15. Briefly describe advantages and applications of JFET.
16. Draw a circuit diagram to obtain the drain characteristics for an n-channel JFET. Thus draw drain characteristics and explain them. *(VTU Jan 2010)*
17. Sketch typical SCR forward and reverse characteristics. Identify all regions of characteristicsa and all important current and voltage levels. *(VTU Jan 2010)*

II. Multiple Choice Questions

1. SCR is a solid state equivalent of Vacuum tube _____
   (a) Tetrode (b) Triode
   (c) Pentode (d) Thyratron
2. SCR is also called _____
   (a) Unijunction Transistor (b) Triode
   (c) Thyristor (d) MOSFET

3. Which of the following devices is expected to have the highest input impedance?
   (a) MOSFET (b) BJT
   (c) JFET (d) Diode
4. The SCR is used as a _____
   (a) Ordinary rectifier (b) Controlled rectifier
   (c) Amplifier (d) None of these
5. SCR has _____ P-N junctions in it.
   (a) One (b) Two
   (c) Three (d) Four
6. UJT is commonly used in construction of _____ electronic circuits
   (a) Amplifiers (b) Oscillators
   (c) Saw tooth generators (d) Rectifiers
7. The internal resistance between two base terminals of UJT is called _____
   (a) Intrinsic stand-off resistance, (b) Inter-base resistance
   (c) Reverse resistance (d) Peak-point resistance
8. The ac equivalent circuit of an FET contains _____
   (a) A voltage source g_m. V_{GS} (b) A current source of value $g_m.V_{GS}$
   (c) A voltage source of value $\mu.V_{GS}$ (d) A current source of value $\mu.V_{GS}$
9. An initial saturated drain current can be attained in an n-channel JFET when V_{GS} is equal to ____
   (a) Pinch off voltage (b) Zero volts
   (c) –4 V (d) Vally voltage
10. The input impedance of a JFET is _____ that of an ordinary transistor.
    (a) More (b) Less
    (c) Equal (d) None of these
11. An FET has _____ regions in its I-V characteristic curve
    (a) 2 (b) 3
    (c) 4 (d) 5
12. A JFET is a _____ transistor.
    (a) Unipolar (b) Bipolar
    (c) Bi-junction (d) None of these
13. A JFET is characterized by _____ gain.
    (a) Current (b) Voltage
    (c) Resistance (d) None of these

14. The voltage gain of a JFET is usually _____ than the ordinary transistor.
    (a) More (b) Equal
    (c) Less (d) Not comparable
15. Input impedance of MOSFET is _____ than that of JFET.
    (a) More (b) Less
    (c) Equal (d) None of these
16. A JFET is _____ sensitive to changes in input voltage than an ordinary transistor.
    (a) More (b) Less
    (c) Equal (d) Not comparable
17. The drain and source terminals of a JFET are _____
    (a) Interchangeable (b) Not interchangeable
    (c) Separated by one pn junction (d) Separated by two pn junctions
18. The output characteristics of a JFET are similar to that of _____ valve.
    (a) Triode (b) Tetrode
    (c) Pentode (d) Diode
19. The noise level in JFET is _____ as compared to ordinary transistor.
    (a) Less (b) More
    (c) Equal (d) Zero
20. SCR can be analyzed using _____ transistors
    (a) Two transistors (b) Three transistors
    (c) Four transistors (d) One transistors and one diode
21. In UJT, the region of characteristics between peak point and valley point is called _____ region.
    (a) Negative resistance (b) Positive resistance
    (c) Active (d) All the above
22. Latching current in SCR is _____ than holding current
    (a) Less (b) More
    (c) Equal (d) None of these
23. The SCR is a _____ Device.
    (a) NPN (b) PNP
    (c) PNPN (d) PNN
24. A relaxation oscillator uses _____
    (a) MOSFET (b) SCR
    (c) UJT (d) BJT

25. The gate current of a JFET is

(a) Very large (b) Very small

(c) Significant (d) Depends on input voltage

III. Numerical Problems

1. In a UJT relaxation oscillator, R_T = 5 KΩ, C_T = 0.1 μF and η = 0.58. Find the frequency of the oscillations ?

   Ans: f_O = 2.305 KHz.

2. In a UJT relaxation Oscillator, R_T = 10 KΩ and C_T = 0.1 μF. The vally potential is 1.5 V and V_{BB} = 20 V. The cut-in voltage of diode is 0.7 V and the stand-off ratio is 0.6. Calculate the frequency of oscillations.

   Ans: f_O = 1.218 KHz.

3. Find the range of R_T for the UJT oscillator that will ensure proper turn ON and OFF of the UJT used. Given: η = 0.33, V_V = 0.8 V, I_V = 15 mA, I_P = 35 μA, and V_P = 18 V. Assume V_{BB} = 30 V.

   Ans: R_T is in between 1.94 KΩ to 342.85 KΩ

4. For a JFET, given that I_{DSS} = 10 mA, $V_{GS(off)}$ = –4V. Determine drain current for V_{GS} = 0 V, -1 V and –4 V.

   Ans: (i) When V_{GS} = 0 V, I_D = 10 mA; (ii) When V_{GS} = –1 V, I_D = 5.625 mA; (iii) When V_{GS} = –4 V, I_D = 0 mA.

5. The trans-conductance of a JFET used in a voltage-amplifier circuit is 3000 μmhos and the load resistance is 10 KΩ. Calculate the voltage amplification of the circuit assuming that $r_d >> R_L$.

   Ans: $A_V = g_m \times R_L$ = 30Ω.

6. When V_{GS} of a JFET changes from –3.1 V to –3 V, the drain current changes from l mA to 1.3 mA. What is the value of trans-conductance ?

   Ans: 3000 μΩ mho.

7. A JFET has a drain current of 5 mA. If I_{DSS} = l0 mA and $V_{GS(off)}$ = –6 V, find the value of (i) V_{GS} and (ii) V_P.

   Ans: (i) V_{GS} = –1.76 V, and (ii) $V_P = V_{GS(off)}$ = –6 V.

8. Sketch the transfer curve for a p-channel JFET with I_{DSS} = 4 mA and V_P = 3 V.

9. A JFET has an I_{DSS} of 9 mA and a $V_{GS(off)}$ of –3 V. Find the value of drain current when V_{GS} = –1.5 V

   Ans: I_D = 2.25 mA.

Answers to Multiple Choice Questions

1. (d)	2. (c)	3. (a)	4. (b)	5. (c)	6. (c)	7. (b)	8. (b)	9. (a)	10. (a)	11. (c)
12 (a)	13. (b)	14. (c)	15. (a)	16. (b)	17. (a)	18. (c)	19. (a)	20. (a)	21. (a)	22. (b)
23. (c)	24. (c)	25. (b).								

UNIT 5

AMPLIFIERS AND OSCILLATORS

OBJECTIVES

In this Unit we will study the details of use of Bipolar Junction Transistor to amplify the input signal in the form of single stage and two stage configuration. The Unit also focuses on various types of feedback circuits and use of feedback to design various oscillator circuits. The Unit objectives are:

(1) To study Decibel–a Unit to compare power levels, and Half power points.

(2) To design and analyze Single Stage CE Amplifier and Capacitor coupled two stage CE amplifier.

(3) To study Series voltage negative feedback and effects of Negative feed back.

(4) To study the Barkhausen Criterion for Oscillations.

(5) To construct and analyze BJT RC phase shift oscillator, Hartley, Colpitts and crystal oscillator Circuits.

5.1 INTRODUCTION TO AMPLIFIER

Amplifier is an electronic circuit/system used to amplify an input signal to increase the current or voltage, or power of the signal at the output. The process of increasing these parameters of an a.c. signal is called **amplification**.

An amplifier increases the magnitude of input current or input voltage by means of energy drawn from an external source (a battery or d.c. source) using an active component like transistor or electron tube (triode). Basically, the active component converts the energy from the d.c. source in to energy at the output of the amplifier which is proportional to the input signal.

5.1.1 Classification

1. **Based on type of output**
   (a) Linier amplifier
   (b) Nonlinear amplifier

A Linear amplifier amplifies all the frequencies of input signal equally. A nonlinear amplifier amplifies different input frequency signals to different extent.

2. Based on the input

(a) Small signal amplifier

(b) Large signal amplifier

A small amplifier amplifies the input signal of the order of certain millivolts and a large signal amplifier amplifies the input signal of the order of several volts.

3. Based on the output

(a) Voltage amplifier

(b) Power amplifier

In voltage amplifier only input voltage gets amplified where as in power amplifier both input current and input voltage gets amplified at output.

4. Based on Transistor configuration

(a Common Base amplifier

(b) Common Emitter amplifier

(c) Common Collector amplifier

In common base amplifier, base terminal of transistor is common between input and output. In common emitter amplifier, emitter terminal is common between input and output. In common collector amplifier, collector terminal is common between input and output.

5. Based on biasing conditions

(a) Class A

(b) Class B

(c) Class AB

(d) Class C

In class A amplifier, the output appears during entire cycle of the input signal (360°). In class B amplifier, the output appears during half cycle of the input signal (180°). In class AB amplifier, the output appears during more than half cycle but less than full cycle of input signal (<360° & >180°). In class C amplifier, the output appears during less than half cycle of input signal (<180°).

6. Based on Frequency response

(a) Audio amplifier

(b) Intermediate Frequency (IF) amplifier

(c) Radio Frequency (RF) amplifier

(d) Ultra High Frequency (UHF) amplifier

(e) Microwave amplifier

7. Based on number of stages

(a) Single Stage amplifier

(b) Multi Stage amplifier

5.2 DECIBELS AND HALF POWER POINTS

5.2.1 Power Gain

While comparing two powers say P_i and P_o, it is common practice to choose the log base of 10.

Decibel is a unit of power change (power gain) or amplification factor. When the output power of an amplifier changes from P_i to P_o, the power level change is

$$\Delta P = \log_{10}\left(\frac{P_o}{P_i}\right) bel \quad \text{or} \quad \Delta P = 10\log_{10}\left(\frac{P_o}{P_i}\right) decibel\ (dB) \qquad ...(5.1)$$

Note that 1 bel = 10 decibel

Example 1

If an amplifier has its power output increased from 4 watts to 8 watts, the increase is measured in decibel (dB) as

$10 \log_{10} (8/4) = 10 \log_{10} 2 = 10 \times 0.3010 = 3.01$ dB $= +3$ dB

Example 2

If an amplifier has its power output increased from 8 W to 16 W, the increase is measured in decibel (dB) as

$10 \log_{10} (16/8) = 10 \log_{10} 2 = 10 \times 0.3010 = 3.01$ dB $= +3$ dB

Example 1 & 2 shows that there is same change in hearing response regardless of level.

Example 3

Determine the power gain in decibels of a power amplifier that has an input voltage V_i of 15 V peak-to-peak and an output voltage V_o of 8 V peak-to-peak across a load resistance R_o of 4 Ω. The amplifier input resistance is 470 KΩ ?

Solution:

$P_i = (V_i^2/R_i) = [(V_{ip\text{-}p}/2\sqrt{2})^2 / R_i] = 60\ \mu W$

$P_o = (V_o^2/R_o) = [(V_{op\text{-}p}/2\sqrt{2})^2 / R_o] = 2$ W

Therefore the power gain ratio is $A_p = P_o/P_i = 33.3 \times 10^3$

To present this on linear scale, this would be a decibel gain of $10 \log_{10} (P_o/P_i) = 10 \log_{10} (33.3 \times 10^3) = 10\ (4.523) = 45.23$ dB.

Other expressions for Power Gain

The power dissipated in a resistance is (V^2/R). So,

$$A_p = 10 \log_{10}\left[\frac{(v_0)^2/R_L}{(v_i)^2/R_i}\right] \text{dB}$$

$$= 10 \log_{10}\left[\frac{v_o}{v_i}\right]^2 \text{dB} \quad (\text{when } R_i = R_L)$$

or.

$$A_p = 20 \log_{10} \left[\frac{v_o}{v_i} \right] dB \quad ...(5.2)$$

Also. $P_o = i_o^2 R_L$ and $P_i = i^2 R_i$ and if $R_L = R_i$

then,

$$A_p = 20 \log_{10} \left[\frac{i_o}{i_i} \right] dB \quad ...(5.3)$$

Amplifier *output power level changes* (ΔP_o) are also measured in decibels, and in this case the equations become:

$$\Delta P_0 = 10 \log_{10} \left[\frac{P_2}{P_1} \right] dB \quad ...(5.4)$$

where P_1 is the initial output power level. and P_2 is the new level.

Also in terms of voltages

$$\Delta P_0 = 20 \log_{10} \left[\frac{v_2}{v_1} \right] dB \quad ...(5.5)$$

and in terms of currents

$$\Delta P_0 = 20 \log_{10} \left[\frac{i_2}{i_1} \right] dB \quad ...(5.6)$$

where v_1 and i_1 are the initial output voltage and current levels and v_2 and i_2 are the new levels.

Example 4

The output power from an amplifier is 50 mW when the signal frequency is 5 KHz. The power output falls to 25 mW when the frequency is increased to 20 KHz. Calculate the output power change in decibels.

Solution:

$$\Delta P_0 = 10 \log_{10} \left[\frac{P_2}{P_1} \right] = 10 \log_{10} \left[\frac{25\ mW}{50\ mW} \right]$$

$$= -3 \text{ dB}$$

Example 5

The output voltage of an amplifier is measured as 1 V at 5 KHz, and as 0.707 V at 20 KHz. Calculate the output power change.

Solution:

$$\Delta P_0 = 20 \log_{10} \left[\frac{v_2}{v_1} \right] = 20 \log_{10} \left[\frac{0.707V}{1\ V} \right]$$

$$= -3 \text{ dB}$$

Examples 4 and 5 demonstrate that the output power of an amplifier is reduced by 3 dB when the measured power falls to half of its normal level or when the measured voltage falls to 0.707 of its normal level.

5.2.2 Characteristics of Decibel System

1. A decibel is a measure of **ratio** and not of **an amount.** It tells us how many times one quantity is greater or lesser with respect to another or the reference quantity. It does not measure the actual (or absolute) voltage or power but only their changes.
2. D*ecibel is non-linear i.e.,* 20 dB is not twice as much power or voltage as 10 dB.
3. This log-based system allows a tremendous range of power ratios to be encompassed by using only two-digit numbers. For example : 1 dB = (1.26 : 1) power ratio and 50 dB = 1,00,000: 1 power ratio.
4. Total dB of a cascaded amplifier can be found by simply adding each stage dBs.
5. It can be proved that 1 dB represents the log of two powers which have a ratio of 1.26.

1 dB = 10 $\log_{10} P_2/P_1$

$$\log_{10}{}^{P_2/P_1} = \frac{1}{10} = 0.1 \qquad \text{or} \qquad \frac{P_2}{P_1} = 10^{0.1} = 1.26$$

Hence, +1dB represents an increase in power of 26%.

5.2.3 Variation of Amplifier Gain with Frequency

Fig. 5.1 shows a typical graph of an amplifier output voltage or power plotted versus frequency. Note that the frequency scale is logarithmic. The output normally remains constant over a middle range of frequencies and falls off at low and high frequencies. The gain over this middle range is termed the *mid-band gain*. The low frequency and high frequency at which the gain falls by 3 dB are designated f_1 and f_2 respectively. This range is normally considered as useful range of operating frequency for the amplifier, and the frequency difference ($f_2 - f_1$) is termed the *amplifier bandwidth* (BW).

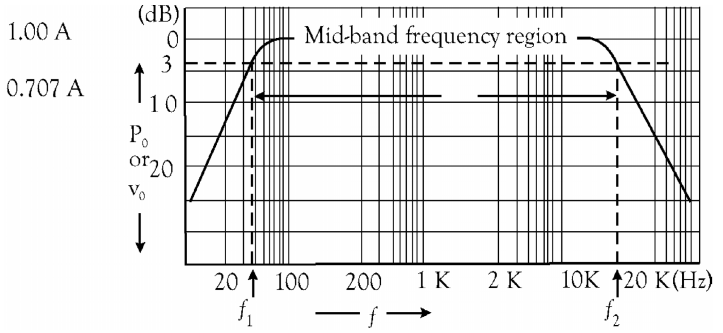


Figure 5.1 *Frequency response of an amplifier*

If the input voltage of an amplifier is kept constant but its frequency is varied, it is found that the amplifier gain,

1. Remains practically constant over a sizable range of mid-frequencies,
2. Decreases at low as well as high frequencies.

While analyzing the above curve shown in Fig. 5.1, three va1ues of frequencies are important:

1. Mid-frequency range
2. Lower cut-off frequency, f_1
3. Upper cut-off frequency, f_2.

The lower and upper cut-off frequencies are defined as those frequencies where voltage gain of the amplifier decreases to 0.707 times the mid-band gain (3 dB point).

5.2.4 3-dB & Half Power Points

Frequencies f_1 and f_2 are termed as the *half-power* points or the 3 dB points. This is because the power output is 3-*dB* from its normal level when P_2 is half P_1. When the amplifier output is expressed as a voltage on the graph of frequency response, then 3 dB points (corresponding to f_1 and f_2) occur when V_2 is 0.707 V_1.

5.2.5 Cut-off Frequencies of Amplifiers

Alpha Cut-off Frequency

It is found that at high frequencies, the value of current gain of CB–connected transistor, α begins to fall. This decrease in α is related to the transit time effect of the charge carriers as they move from the emitter to collector. The alpha cut-off frequency f_α is that high frequency at which the α of a *CB-connected* transistor becomes 0.707 of its low-frequency value (say, 1 KHz.).

Beta Cut-off Frequency

The beta cut-off frequency f_β is that high frequency at which the β of a *CE*-connected transistor drops to 0.707 of its low-frequency (say, 1 KHz) value.

5.3 SINGLE STAGE CE AMPLIFIER

A single stage transistor amplifier consists of one transistor, biasing circuit and other auxiliary components, used to amplify weak signals. Although a practical amplifier consists of a number of stages, such a complex circuit can be conveniently split up into separate single stages. By analyzing only a single stage and using this single stage analysis repeatedly, we can effectively analyze the complex circuit. It follows that single stage amplifier analysis is of great value in understanding the practical amplifier circuits.

5.3.1 How Transistor Amplifies?

Fig. 5.2 shows a single stage transistor amplifier. When a weak a.c. signal is applied to the base of transistor, a small base current (which is a.c.) starts flowing through it. Due to transistor action, a much larger (β times the base current) a.c. current flows through the collector load R_c. As the value of R_c is

quite high (usually 4–10 KΩ), a large voltage appears across R_c. Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

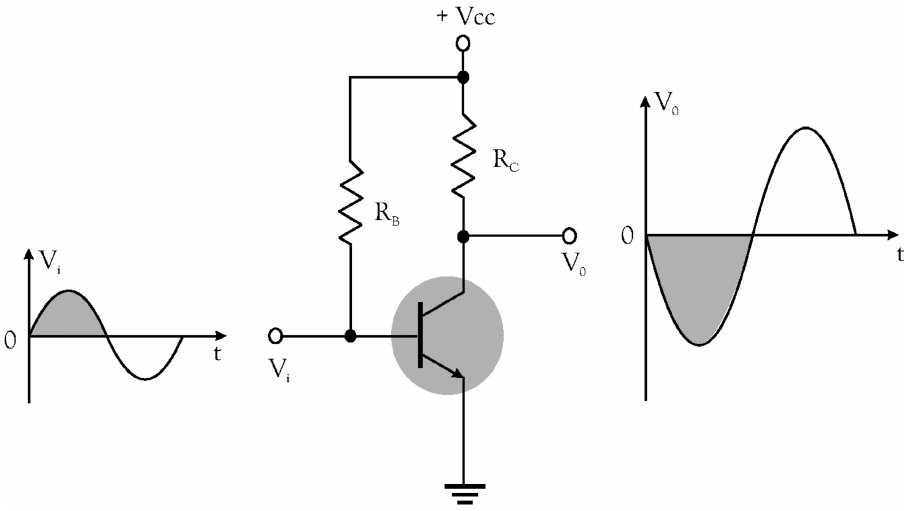


Figure 5.2 *Single stage CE amplifier*

5.3.2 Practical Circuit of Transistor Amplifier

A practical version of RC coupled single stage CE amplifier with voltage divider bias and various controlling capacitors is shown in Fig. 5.3. The various circuit elements and their functions are described below:

(i) **Biasing circuit**: The resistances R_1, R_2 and R_E used for biasing and stabilization. The biasing circuit must establish a proper operating point otherwise a part of the negative half cycle of the signal may be clipped in the output.

(ii) **Input capacitor C_1:** An electrolytic capacitor C_1 (≈ 10 μF) is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance will come across R_2 and thus change the bias. The capacitor C_1 allows only a.c. signal to flow but isolates the signal source from R_2.

(iii) **Emitter bypass capacitor C_E:** An emitter bypass capacitor C_E (≈ 100 μF) is used in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, there by reducing the output voltage.

(iv) **Coupling capacitor C_2:** The coupling capacitor C_2 (≈ 10 μF), couples one stage of amplification to the next stage. If it is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C. This is because R_C will come in

parallel with the resistance R_1 of the biasing network of the next stage, thereby altering the bias conditions of the latter. In short, the coupling capacitor C_2 isolates the d.c. of one stage from the next stage, but allows the flow of a.c. signal.

The input signal is injected into the base-emitter circuit whereas output signal is taken out from the collector-emitter circuit. The E/B junction is forward-biased by V_{CC} and C/B junction is reversed-biased by V_{CC}.

$$I_C = \beta I_B \quad \text{and} \quad V_{CE} = V_{CC} - I_C R_C \qquad ...(5.7)$$

Circuit Operation

When positive half-cycle of the signal is applied:

1. V_{BE} is increases because it is already positive w.r.t. the ground as per biasing condition.
2. This leads to increase in forward bias of base-emitter junction.
3. I_B increases according to increase in forward bias.
4. I_C is increases by β times of the increase in I_B.
5. Voltage Drop $I_C R_C$ across R_C increases considerably.
6. Consequently V_{CE} is decreased as $V_{CE} = V_{CC} - I_C R_C$.

Hence the negative half-cycle of the amplified output signal appears at output. This means that a positive half-cycle of input signal becomes negative half-cycle output signal. Similarly, during negative half-cycle of the input signal, the reverse action takes place and an amplified positive half-cycle signal appears at the output.

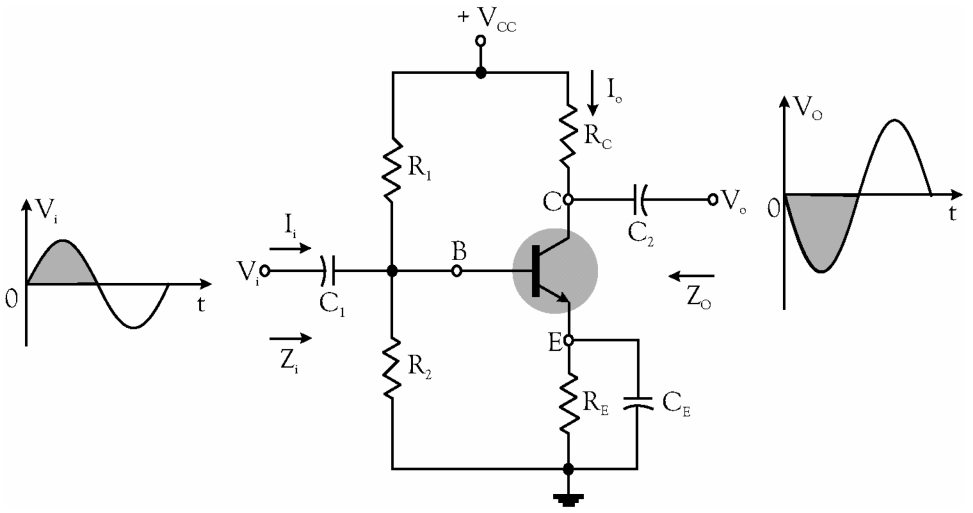


Figure 5.3 *RC coupled single stage CE amplifier with voltage divider bias*

5.3.3 Various Circuit Currents

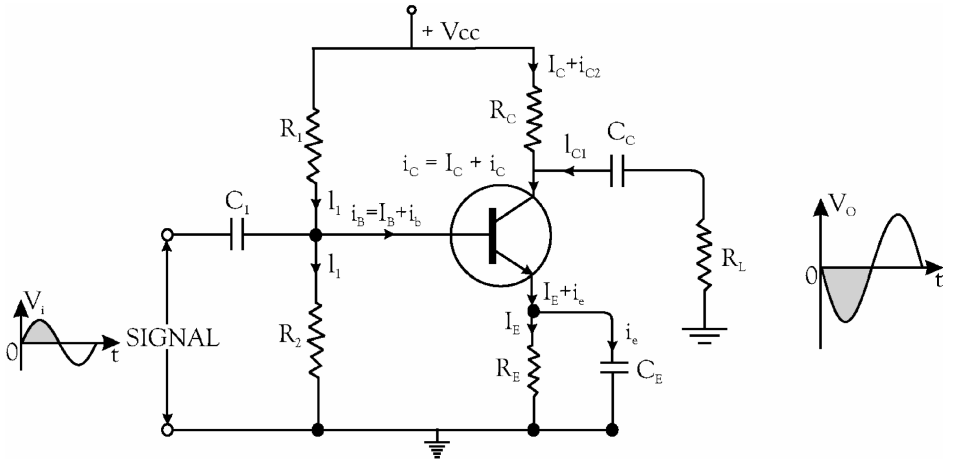


Figure 5.4 *RC coupled single stage CE amplifier with voltage divider bias and currents*

It is useful to mention the various currents in the complete amplifier circuit. These are shown in the circuit of Fig. 5.4.

(i) Base current: When no signal is applied in the base circuit, d.c. base current I_B flows due to biasing circuit. When a.c. signal is applied, a.c. base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by :

$$i_B = I_B + i_b$$

(ii) Collector current: When no signal is applied, a d.c. collector current I_C flows due to biasing circuit. When a.c. signal is applied, a.c. collector current i_c also flows. Therefore, the total collector current i_C is given by;

$$i_C = I_C + i_c$$

where $I_C = \beta I_B$ = zero signal collector current

$i_c = \beta i_b$ = collector current due to signal.

(iii) Emitter current: When no signal is applied, a d.c. emitter current I_E flows. With the application of signal, total emitter current i_E is given by;

$$i_E = I_E + i_e$$

It is useful to keep in mind that:

$$I_E = I_B + I_c$$

$$i_e = i_b + i_c$$

Now base current is usually very small, therefore, as a reasonable approximation,

$$I_E \cong I_c \text{ and } i_e \cong i_c$$

Phase Reversal

In common emitter connection, when the input signal voltage increases in the positive direction, the output voltage increases in the negative direction and *vice-versa.* In other words, in CE amplifier, there is a phase difference of 180° between the input and output voltage. This is called phase reversal.

5.3.4 Graphical Representation

Fig. 5.5 shows the output characteristics of the practical circuit of Transistor Amplifier in CE configuration.

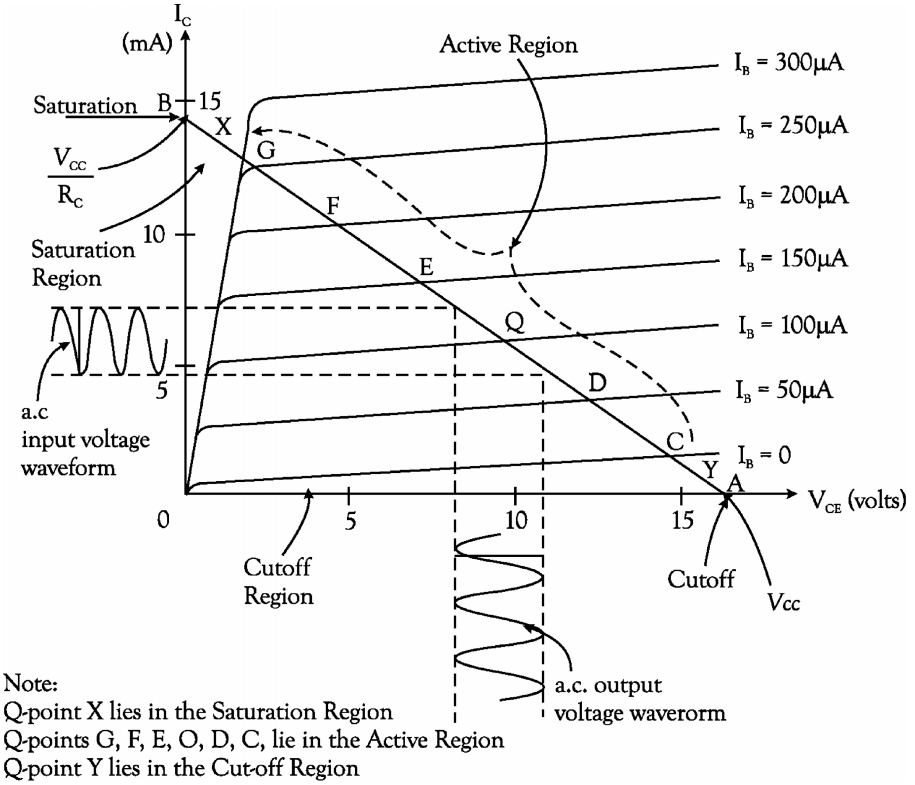


Figure 5.5 *Graphical representation of output of CE amplifier*

While analyzing a transistor amplifier circuit, it is required to find out the collector current for different collector-emitter *voltages.* At first we have analyzed the *d.c.* conditions of the circuit and drawn d.c. load line, without applying a.c. signal.

D.C. Load Line

For drawing the *d.c.* load line of a transistor amplifier, one must know its cut-off and saturation points. lt is a straight line joining these two points. The *voltage* equation of the collector emitter circuit of Fig. 5.4 is:

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \quad I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

We deal with the following two specific cases:

(i) When $I_C = 0$, $V_{CE} = V_{CC} \rightarrow$ Cut-off point A

(ii) When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} \rightarrow$ Saturation point B

The *d.c.* load line is constructed by joining these two points A and B, as shown in Fig. 5.5

A.C. Load line

Now, if we apply *a.c.* input signal, it produces sinusoidal variations in base current. This results in sinusoidal variations in the Q-point. (also called operating point). All the operating points like C, D, E, F and G lying between cut-off and saturation points, form the Active Region of the transistor. Quiescent *(Q)* points X and Y lie in the Saturation and Cut-off Regions respectively.

In Fig. 5.5, the Q-point lies at point Q which is at the intersection of the load line and the output characteristic of I_C *vs.* V_{CE} at a particular value of I_B (100 μA). Because of the a.c. fluctuations in collector current, the output voltage swings sinusoidally above and below the quiescent voltage. The a.c. output voltage is inverted with respect to the *a.c.* input voltage, meaning that it is 180° out of phase with the input. During the positive half-cycle of input voltage, the base current increases, causing the collector current to increase. This produces a larger voltage drop across the collector resistor therefore, the collector voltage decreases, and we get the first negative half-cycle of output voltage. Conversely, during the negative half-cycle of input voltage, less collector current flows and the voltage drop across the collector resistor decreases, Consequently the collector to ground voltage rises and we get the positive half-cycle of output voltage.

5.3.5 AC Analysis of CE Amplifier

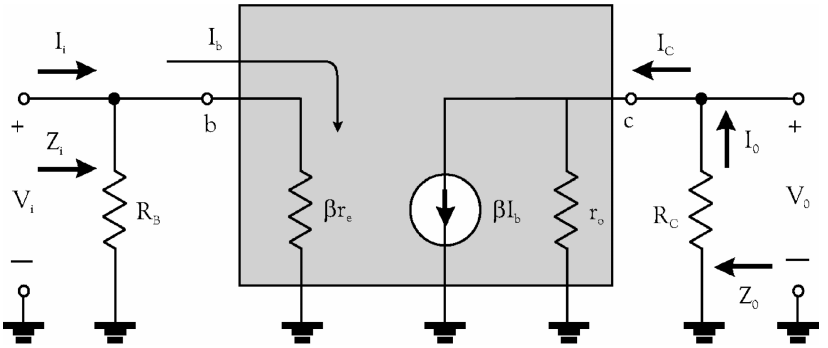


Figure 5.6 *AC equivalent circuit of CE amplifier*

1. Input Impedance : Z_i

When viewed from base, ac resistance of the emitter junction is βr_e. As seen from Fig. 5.6, circuit input resistance is

$$\boxed{Z_i = R_B \| \beta r_e} \text{ ohms}$$

For the majority of situations R_B is greater than βr_e by more than a factor of 10, permitting the following approximation:

$$Z_i \cong \beta r_e \text{ ohms when } R_B \geq 10\beta r_e \quad ...(5.8)$$

For voltage divider bias $R_B = R_1 \| R_2 = R_1R_2/(R_1 + R_2)$

2. Output Impedance : Z_o

The output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$.

For Fig. 5.6, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source.

$$\boxed{Z_o = R_C \| r_o} \text{ ohms}$$

If $r_o = 10\ R_C$, the approximation $R_C \| r_o$, R_C becomes

$$\boxed{Z_0 \cong R_C}_{r_o \geq 10R_C} \quad ...(5.9)$$

3. Voltage Gain : A_V

The resistors r_O and R_C are in parallel,

and $V_0 = -\beta I_b (R_C \| r_o)$

but $I_b = \dfrac{V_i}{\beta r_C}$

so that $V_0 = -\beta\left(\dfrac{V_i}{\beta r_e}\right)\left(R_C \| r_o\right)$

and $\boxed{A_v = \dfrac{V_0}{V_i} = -\dfrac{\left(R_C \| r_o\right)}{r_e}}$

If $r_0 \geq 10R_C$, then

$$\boxed{A_v = -\frac{R_C}{r_e}}_{r_o \geq 10\ R_C} \quad ...(5.10)$$

4. Current Gain : A_i

Applying the current-divider rule to the input and output circuits,

$$I_0 = \frac{(r_0)(\beta I_b)}{r_0 + R_C} \text{ and } \frac{I_0}{I_b} = \frac{r_0\beta}{r_0 + R_C}$$

with $$I_b = \frac{(R_B)(I_i)}{R_B + \beta r_e} \text{ or } \frac{I_b}{I_i} = \frac{R_B}{R_B + \beta r_e}$$

The result is

$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_b}\right)\left(\frac{I_b}{I_i}\right) = \left(\frac{r_0\beta}{r_0 + R_C}\right)\left(\frac{R_B}{R_B + \beta r_e}\right)$$

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_0}{(r_o + R_C)(R_B + \beta r_e)}}$$

However, if $r_0 \geq 10R_C$ and $R_B \geq 10\beta r_e$, which is often the case,

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_B r_0}{(r_o)(R_B)}$$

Hence,

$$\boxed{A_i \cong \beta}_{r_o \geq 10R_C,\ R_B \geq 10\beta r_e} \quad ...(5.11)$$

Using above equations we can write,

$$\boxed{A_i = - A_v \frac{Z_i}{R_C}} \quad ...(5.12)$$

5. Phase Relationship:

The negative sign in the resulting Eqn. 5.12 for A_V reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 5.4.

5.3.6 Characteristics of a CE Amplifier

A CE transistor amplifier has the following characteristics:

1. It has moderately low input resistance (l KΩ to 2 KΩ).

2. Its output resistance is moderately large (50 KΩ or so),
3. Its current gain (β) is high,
4. It has very high voltage gain of the order of 1500 or so,
5. It produces very high power gain of the order of 10,000 times or 40 dB,
6. It produces *phase reversal* of input signal *i.e.*, input and output signals are 180^0 out of phase with each other.

5.3.7 Uses of CE Amplifier

Most of the transistor amplifiers are of CE type because of large gains in voltage, current and hence power. Moreover, their input and output impedance characteristics are suitable for many applications.

5.4 CAPACITOR COUPLED TWO STAGE CE AMPLIFIER

5.4.1 Circuit

The Fig. 5.7 shows the capacitor coupled two stage CE amplifier. As shown in the figure, the output signal of first-stage with transistor Q_1 is coupled to the input of the next stage with transistor Q_2 through coupling capacitor and resistive load at the output terminal of first stage. Due to the use of capacitor and resistor in the coupling of stages, such an amplifier is also called **RC coupled amplifier.**

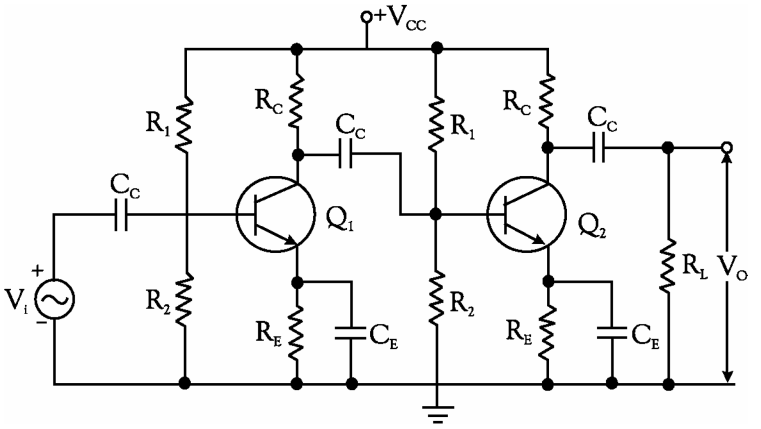


Figure 5.7 *Two stage RC coupled amplifier using transistors*

The coupling does not affect the quiescent point of the next stage since the coupling capacitor CC blocks the dc voltage of the first stage from reaching the base of the second stage.

5.4.2 Operation

The a.c. input signal V_i is applied to the base of transistor Q_1 which amplifies the signal. Its phase is reversed, and the amplified output appears across its collector load R_{C1}. The output of the first stage across R_{C1} is given to the base of the second stage transistor Q_2 through the capacitor Cc. Further amplification is done by Q_2 and the amplified output is available across R_{C2} in the collector of Q_2, with further phase reversal. The output signal V_O is the twice-amplified replica of the input signal V_i. It is in-phase with V_i because its phase has been reversed twice. The total gain is lesser than the product of the gains of individual stages because, when a second stage is made to follow the first stage, the effective load resistance of the first stage is reduced due to the shunting effect of the input resistance of the second stage. This reduces the gain of the stage which is loaded by the second stage. But in general, If A_1 is the gain of first stage of the amplifier and A_2 is the gain of second stage of the amplifier, then the total gain of multi-stage amplifier is $A = A_1 \times A_2$.

5.4.3 Frequency Response

The frequency response characteristic for an *R*-C coupled amplifier is given in Fig. 5.8. It is apparent that the voltage gain drops off at low (less than 50 Hz) and high (more than 20 KHz) frequencies, whereas it is uniform over the mid-band range of 50 Hz to 20 KHz. The bandwidth of the circuit is $(f_2 - f_1)$.

The RC network gives a wideband frequency response without peak at any frequency and hence used to cover a complete audio frequency (AF) amplifier band. However, its frequency response drops off at very low frequencies due to coupling capacitors and also at high frequencies due to shunt capacitors such as stray capacitance. This is illustrated in Fig. 5.8.

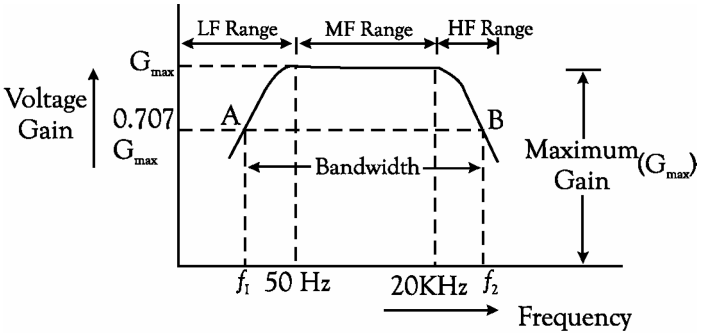


Figure 5.8 *Frequency response of RC coupled two stage amplifier*

5.4.4 Advantages of RC coupling

1. It requires resistors and capacitors which are very cheap, light in weight and small in size.
2. Its frequency response is excellent in the audio frequency range.
3. The nonlinear distortion due to RC coupling is minimum because it does not employ any inductive component such as coil or transformer.
4. Its overall amplification is greater than the amplification provided by other types of couplings like inductive coupling.

5.4.5 Disadvantages of RC Coupling

1. Impedance matching is not possible with RC coupling due to the fact that the output impedance of the amplifier is several hundred ohms whereas the input impedance of Speaker is of few ohms. (normally 8 – 16 ohms).
2. Amplifier becomes noisy with age of components and in the humid environment.

5.4.6 Difference between RC-coupled and Single Stage Amplifier

S. No.	RC-Coupled Amplifier	Single Stage Amplifier
1	Its frequency response is much better in the audio frequency range.	Its frequency response is poor in the audio frequency range.
2	It has better fidelity over a wide range of frequency.	It has low fidelity.
3	Non-linear distortion is less.	Non-linear distortion is more.
4	Overall amplification is higher.	Overall amplification is low.

5.4.7 Applications

RC coupled amplifiers are used in audio small signal amplifiers, especially in record players, tape recorders, public address systems, radio receivers and television receivers as pre-amplifier. Since impedance matching is poor, reduced power is passed to the speaker and hence can not be used for power amplification.

5.5 SERIES VOLTAGE NEGATIVE FEEDBACK

A feedback amplifier is a modified amplifier in which a *fraction of the amplifier output is fed back to the input circuit.* This partial dependence of amplifier input on its output helps to control the output. A feedback amplifier consists of two parts: an amplifier and a feedback circuit. There are two types of feedback systems. They are:

(i) Positive feedback

If the feedback voltage (or current) is so applied as to *increase the input voltage* (*i.e.,* output is in phase with input), then it is called *positive feedback.* Other names for it are: *regenerative* or *direct* feedback.

Since positive feedback produces excessive distortion, it is seldom used in amplifiers. However, because it increases the power of the original signal, it is used in oscillator circuits.

(ii) Negative feedback

If the feedback voltage (or current) is so applied as to reduce the amplifier input (*i.e.,* outpur is 180° out of phase with input); then it is called negative feedback. Other names for it are : *degenerative* or *inverse* feedback. Negative feedback is frequently used in amplifier circuits.

5.5.1 Principles of Negative Feedback

Consider an inverting amplifier, where the output voltage is 180° out of phase w.r.t the input voltage as shown in Fig. 5.9.

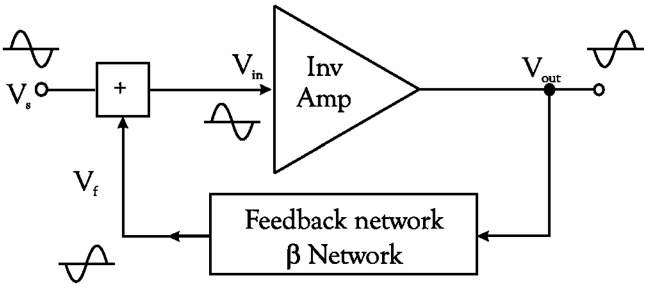


Figure 5. 9 *Amplifier with negative feedback*

A part of output voltage is taken as feedback voltage (V_f) using the feedback or β-network and fed back to input. Let the feedback factor be β.

Then $V_f = \beta V_{out}$

or $$\boxed{\beta = \frac{V_f}{V_{out}}} \quad ...(5.13)$$

The value of β lies between 0 and 1. When β is zero, no feedback is applied, and when β is one, whole of the output voltage is applied as a feedback voltage, i.e. $V_f = V_{out}$. Assuming that the feedback network is purely resistive, then the voltages V_f and V_{out} will be in phase. But for inverting amplifier, V_{out} and V_s will be out of phase by 180°. Thus the signal voltages V_s and feedback voltage V_f will be out of phase, as illustrated in the Fig. 5.9. Therefore, net input voltage V_{in} to the amplifier will be difference between V_s and V_f. Hence this type of feedback is known as "negative feedback". Thus

$$V_{in} = V_s - V_f \quad \text{or} \quad V_s = V_{in} + V_f$$

Then, the gain with feedback is

$$A_f = \frac{V_{out}}{V_s} \quad \text{or} \quad A_f = \frac{V_{out}}{V_{in} + V_f}$$

But $V_f = \beta V_{out}$ Hence

$$A_f = \frac{V_{out}}{V_{in} + \beta V_{out}} = \frac{V_{out} / V_{in}}{1 + \beta \frac{V_{out}}{V_{in}}}$$

Since $\frac{V_{out}}{V_{in}}$ = A which is the gain without feedback

$$\boxed{A_f = \frac{A}{1 + A\beta}} \quad ...(5.14)$$

Eqn. 5.14 is the general feedback equation. A_f is called the closed-loop gain since the gain is measured with the feedback loop. In negative feedback system, the feedback voltage V_f is subtracted from the signal input voltage V_S. As a result, the magnitude of gain with voltage feedback is always less than the magnitude of gain without feedback.

$$|A_f| < |A|$$

5.5.2 Advantages of Negative Feedback

The numerous advantages of negative feedback outweigh its only disadvantage of reduced gain. Some of the advantages of negative feedback are:

1. Higher fidelity *i.e.,* more linear operation,
2. Highly stabilized gain,
3. Increased bandwidth *i.e.,* improved frequency response,
4. Less amplitude distortion,
5. Less harmonic distortion,
6. Less frequency distortion,
7. Less phase distortion,
8. Reduced noise,
9. Input and output impedances can be modified as desired.

5.5.3 Types of Negative Feedback

The feedback voltage applied to input can be proportional to either output load voltage or output load current and is applied to input either in series or in shunt. Accordingly there are four basic feedback configurations:

(a) **Voltage series feedback:** Here, output voltage is applied to feedback network and the feedback voltage is applied in series with input voltage of the amplifier.

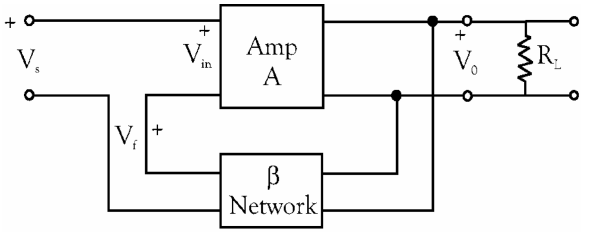


Figure 5.10 (a) *Voltage series feedback*

(b) **Voltage shunt feedback:** Here, output voltage is applied to feedback network and the feedback voltage is applied in shunt with input voltage of the amplifier.

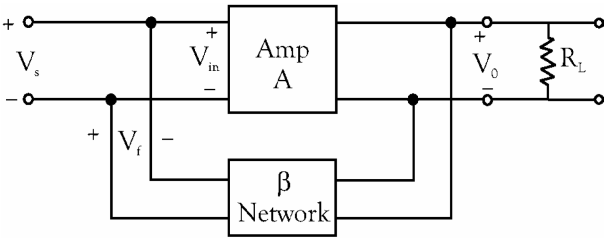


Figure 5.10 (b) *Voltage shunt feedback*

(c) **Current Series Feedback:** Here, output load current is applied to feedback network and the feedback voltage is applied in series with input voltage of the amplifier.

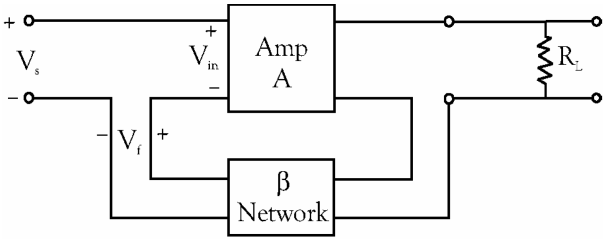


Figure 5.10 (c) *Current series feedback*

(d) **Current Shunt Feedback:** Here, output load current is applied to feedback network and the feedback voltage is applied in parallel with input voltage of the amplifier.

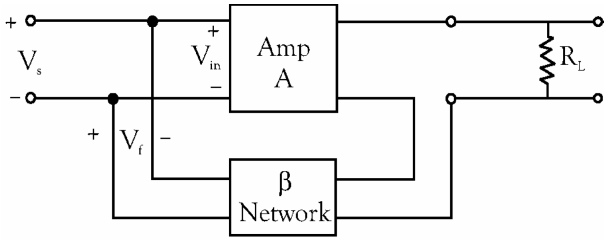


Figure 5.10 (d) *Current shunt feedback*

5.6 EFFECT OF NEGATIVE FEEDBACK

5.6.1 Gain Stability

The gain A of the amplifier without feedback is not stable, but it changes with changes in operating conditions of the device, changes in temperature etc. The application of negative feedback stabilizes the gain A_f. We know that,

$$A_f = \frac{A}{1+A\beta}$$

Differentiating both sides we get,

$$\frac{dA_f}{dA} = \frac{(1+A\beta) - (A\beta)}{(1+A\beta)^2} = \frac{1}{(1+A\beta)^2}$$

$$\frac{dA_f}{A_f} = \frac{dA}{(1+A\beta)^2} \times \frac{1}{A_f} = \frac{dA}{(1+A\beta)^2} \times \frac{1}{\frac{A}{(1+A\beta)}}$$

$$= \frac{dA}{(1+A\beta)^2} \times \frac{1+A\beta}{A}$$

Therefore, $$\boxed{\frac{dA_f}{A_f} = \frac{1}{1+A\beta} \times \frac{dA}{A}} \quad \text{...(a)}$$

Thus changes in the gain with feedback are less than the changes in the gain without feedback. As changes in the gain are reduced, the gain with feedback is stabilized and remains almost constant.

5.6.2 Gain Control

Gain of an amplifier with feedback can be written as

$$A_f = \frac{A}{1+A\beta} = \frac{1}{\beta + \frac{1}{A}}$$

If A is very large, then $1/A \approx 0$, hence $\mathbf{A_f \approx 1/\beta}$

Thus the gain of the feedback amplifier depends only on the feeback network.

It can be shown that, for non-inverting amplifier,

$$\beta = \frac{R_1}{R_1 + R_F}$$

where R_1 = Input resistance and

R_F = Feedback resistance of an amplifier.

The gain with feedback is $1/\beta$ and is depends on R_F and R_1 only

$$\frac{1}{\beta} = \frac{R_1 + R_F}{R_1} = 1 + \frac{R_F}{R_1} \quad \text{...(b)}$$

Hence, the gain of the amplifier with feedback can be controlled by the feedback network and is extremely stable.

5.6.3 Constant Gain for all Frequencies

When the gain A, of the amplifier is very large, the gain with feedback A_f, is dependent only on the β factor, as seen above. If the β network is made up of pure resistance which are stable and constant then the gain A_f will also remain stable and will remain the same for all frequencies, temperature and variations in transistor parameters at least theoretically. Thus, the voltage gain of the amplifier with feedback is independent of signal frequency.

5.6.4 Increase in Bandwidth

The bandwidth of an amplifier without feedback is equal to the separation between the 3 dB frequencies f_1 and f_2.

$$\therefore \quad BW = f_2 - f_1$$

where f_1 =lower 3 dB frequency, and f_2 = upper 3 dB frequency

If **A** is its gain, then the gain-bandwidth product is **A x BW** and for any amplifier, the gain-bandwidth product is always constant, i.e.,

$$\boxed{Gain \times Bandwidth = constant}$$

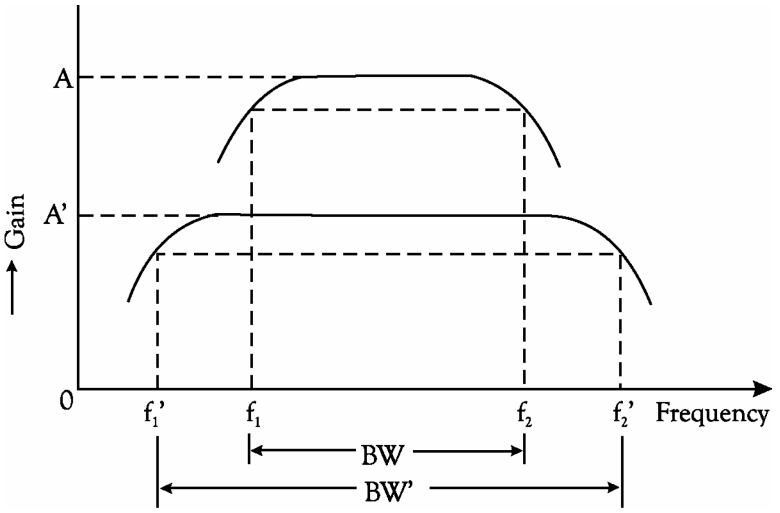


Figure 5.11 *Plot of amplifier gain with frequency*

Now, when negative feedback is applied, the amplifier gain is reduced. Since the gain bandwidth product has to remain the same in both cases, it is obvious that the bandwidth must increase to compensate for the decrease in gain (Fig. 5.11). It can be proved that with negative feedback, the lower and upper 3 dB frequencies of an amplifier become

$$f_1' = \frac{f_1}{(1+\beta A)} \text{ and } f_2' = f_2 (1 + \beta A) \quad \text{...(c)}$$

Hence as a result of negative feedback, f_1' has decreased whereas f_2' has increased thereby giving a wider separation or bandwidth.

5.6.5 Effect on Input Impedance

The Equivalent circuit to study input impedance with feedback is shown in Fig. 5.12.

Let, Z_i = Input impedance without feedback

Z_{if} = Input impedance with feedback

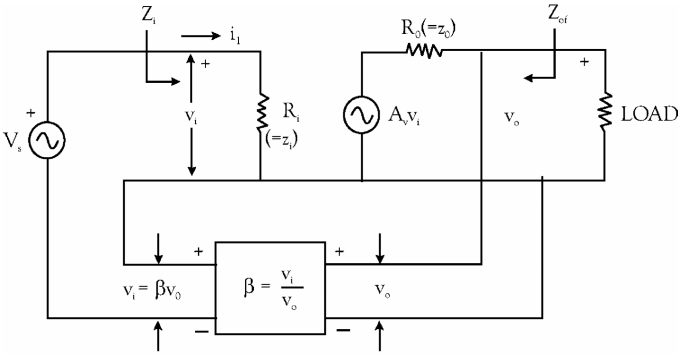


Figure 5.12 *Equivalent circuit to study input impedance*

Voltage gain without feedback, $A_V = \frac{v_0}{v_i}$

$$A_f = \frac{A}{1 + A\beta}$$

Input current $i_i = \frac{v_i}{Z_i}$, where v_i = input voltage

But $v_i = v_s - v_f$, where v_f = feedback voltage

$$\therefore \quad i_i = \frac{v_s - v_f}{Z_i} = \frac{v_s - \beta v_o}{Z_i}, \text{ putting } v_f = \beta v_o$$

But $v_0 = A_v v_i$, where A_v = open loop voltage gain

$$\therefore \quad i_i = \frac{v_s - \beta A_v v_i}{Z_i}$$

or $i_i Z_i = v_S - \beta A_v v_i$

or $v_S = i_i Z_i + A_v \beta v_i$

As $v_i = i_i Z_i$,

$v_S = i_i Z_i + A_v \beta i_i Z_i$

or $\frac{v_S}{i_i} = Z_i (1+A_v\beta)$

But $\frac{v_S}{i_i} = Z_{if}$, the input impedance with feedback

$\therefore$ $Z_{if} = Z_i (1+A_v\beta)$ ...(d)

Hence, the input impedance with feedback is $(1+A_v\beta)$ times the input impedance without feedback. Thus the effect of negative feedback is to increase the input impedance of a series-voltage negative feedback amplifier by a factor $(1+ A_v\beta)$.

5.6.6 Effect on Output Impedance

Let the source signal voltage v_S be set equal to zero, and let an arbitrary voltage v be applied to the output port. The resulting current in the output circuit be i.

We have, $A_v v_i + iZ_0 = v$, putting $R_0 = Z_0$

In general, $v_i = v_S - v_f$, where v_f = feedback voltage

when $v_S = 0$, $v_i = - v_f$

$\therefore$

$v = - A_v v_f + iZ_o$

or $v = iZ_0 - A_v (\beta v)$, putting $v_f = \beta v$ $\left[\because \quad \beta = \frac{v_f}{v}\right]$

or $v + A_v\beta v = iZ_0$

i.e., $v(1 + A_v\beta) = iZ_0$

or $\frac{v}{i} = \frac{Z_0}{1 + A_v\beta}$

But $\frac{v}{i} = Z_{of}$, the output impedance with feedback.

$\therefore$ $Z_{of} = \frac{Z_0}{1 + A_v\beta}$ ...(e)

Hence, due to negative feedback, the output impedance gets reduced by the factor $(1 + A_v\beta)$.

The following table gives an idea on effect of various feedback systems on input and output impedances.

Table 5.1 Effect of negative feedback

Sl. No.	Type of feedback system	Effect of negative feedback on input impedance	Effect of negative feedback on output impedance
1.	Voltage-series	Increases	Decreases
2.	Voltate-shunt	Decreases	Decreases
3.	Current-series	Increases	Increases
4.	Current-shunt	Decreases	Increases

5.7 ADDITIONAL EFFECTS OF NEGATIVE FEEDBACK

5.7.1 Decibels of Feedback

Negative feedback can be measured in decibels. A 40 dB negative feedback for an amplifier means that the amplifier gain will reduce by 40 dB on application of feedback. Thus, $A_{Vf} = A_v - 40\ dB = A_v/100$

5.7.2 Harmonic Distortion on Feedback

In practical amplifiers, due to nonlinearity of the transistor characteristics, the output contains a harmonic frequency terms i.e., along with input frequency f, there will be other frequency components like 2f, 3f, 4f, ... etc., at the output and are called harmonic components. These additional frequencies produces distortion at output called harmonic distortion.

Let the harmonic distortion voltage generated within the amplifier change from D to D' when negative feedback is applied to the amplifier.

Suppose $D' = x\ D$ ...(g)

The fraction of the output distortion voltage which is fed back to the input is

$$= \beta D' = x\beta D$$

After amplification, it becomes βxDA and is out-of-phase with original distortion voltage D.

Hence, the new distortion voltage D' which appears in the output is $D' = D - \beta x\ DA$ ...(h)

From (g) and (h), we get

$$x\ D = D - x\beta DA$$

or $$x = \frac{1}{1 + \beta A}$$

Substituting this value of x in Eq. (g) above, we have

$$D' = \frac{D}{1 + \beta A} \qquad ...(i)$$

It is obvious from the above equation that D' < D. In fact, negative feedback reduces the amplifier distortion by the amount of loop gain *i.e.*, by a factor of $(1 + \beta A)$.

5.7.3 Attenuation Distortion on Feedback

Attenuation distortion occurs when different frequencies are amplified by different amounts. This is illustrated in Fig. 5.13. The negative feedback reduces attenuation distortion by factor $(1 + \beta A_v)$.

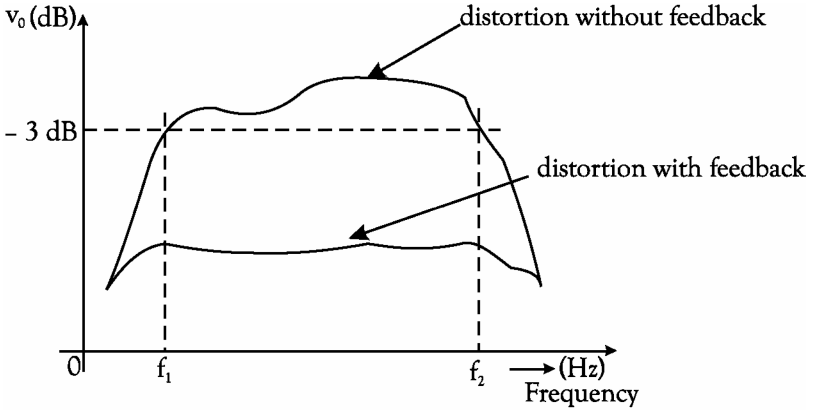


Figure 5.13 *Attenuation distortion*

5.7.4 Phase Shift on Feedback

In order to determine the effect of negative feedback on amplifier phase shift, let us assume that the open-loop gain has a phase shift angle of ϕ and that the closed-loop phase shift is ϕ_{CL}. Then,

Open-loop gain = $A_v \angle\phi$

and $$A_{CL} \angle\phi_{CL} = \frac{A_v \angle\phi}{1 + A_v\beta\angle\phi} = \frac{A_v\beta \sin\phi}{1 + A_v\beta \cos\phi + j A_v \beta \sin\phi}$$

or $$\phi_{CL} = \phi - \tan^{-1} \frac{A_v\beta \sin\phi}{1 + A_v \beta \cos\phi}$$

Thus negative feedback reduces amplifier phase shift by an angle

$$\tan^{-1} \frac{A_v\beta \sin\phi}{1 + A_v \beta \cos\phi} \qquad ...(j)$$

5.7.5 Circuit Noise

The term noise in amplifiers is used broadly to describe any spurious electrical disturbance that causes an output from an amplifier when the applied input signal is zero. Noise may be produced by causes which may be either external to the system or internal to the system. Hence, the noise N can be decreased by a factor of $(1 + \beta A_V)$ as in the case of non-linear distortion. It is noted that the only noise generated by the circuit elements in the feedback loop is decreased by the feedback. Noise produced by the elements external to the feedback loop (e.g., bias resistors) will not be reduced by negative feedback. Thus negative feedback reduces circuit noise.

5.8 THE BARKHAUSEN CRITERION FOR OSCILLATIONS

5.8.1 What is an Oscillator ?

An oscillator is an amplifier, which uses a positive feedback and without any external input signal generates an output signal at a desired frequency.

5.8.2 Comparison between an Amplifier & Oscillator

An amplifier produces an output signal whose waveform is similar to the input signal but whose power level is generally high. This additional power is supplied by the external dc source. Hence, an amplifier is essentially an energy converter *i.e.,* it takes energy from the de power source and converts it into ac energy at signal frequency. The process of energy conversion is controlled by the input signal. If there is no input signal, there is no energy conversion and hence there is no output signal.

An oscillator *does not require an external signal* either to start *or* maintain energy conversion process. It keeps producing an output signal *so* long as the dc power source is connected. Moreover, the frequency of the output signal is determined by the passive components used in the oscillator and can be varied as desired.

5.8.3 Classification of Oscillators

Electronic oscillators may be broadly divided into following two groups:

(i) Sinusoidal (or harmonic) oscillators-which produce sinusoidal output signal.

(ii) Non-sinusoidal (or relaxation) oscillators-which produce square, rectangular or sawtooth waveform signal or of pulse shape signal at the output.

Sinusoidal oscillators may be further subdivided into:

(a) Tuned-circuits or LC feedback oscillators such as Hartley, Colpitt's and Clapp etc.

(b) RC phase-shift oscillators such as Wien-bridge oscillator.

(c) Negative-resistance oscillators such as tunnel diode oscillator.

(d) Crystal oscillators such as Pierce oscillator.

(e) Heterodyne or beat-frequency oscillator (BFO).

5.8.4 Barkhausen Criterion

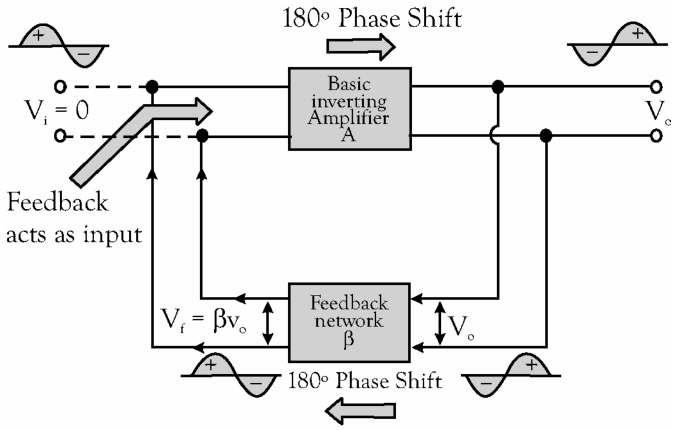


Figure 5.14 *Basic block diagram of oscillator circuit*

Consider an amplifier circuit with a feedback network connected between output and input as shown in Fig. 5.14. The feedback is selected in such a way that the voltage derived from output V_f using feedback network is in phase with input voltage V_i. Since the inverting amplifier introduces 180° phase shift, the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input. This ensures positive inphase which is the first condition feedback.

Consider a fictitious voltage V_i applied at the input of the amplifier. The output voltages is

$$\boxed{V_o = A\,V_i} \qquad ...(5.15)$$

The feedback factor β decides the feedback voltage to be given to input,

$$\boxed{V_f = \beta\,V_o} \qquad ...(5.16)$$

Substituting (5.15) in (5.16) we get,

$$\boxed{V_f = A\,\beta\,V_i} \qquad ...(5.17)$$

For the oscillator, the feedback voltage should drive the amplifier and hence V_f must act as V_i. From equation (5.17) we can write that, V_f is sufficient to act as V_i when the product of open loop gain and feedback factor is units. i.e.,

$$\boxed{|A\,\beta| = 1} \qquad ...(5.18)$$

Eqn. 5.18 gives the second condition in sustained oscillation.

The above two conditions required to produce oscillation in an oscillator are called Barkhausen Criterion for oscillation. They are summarized below:

1. The total phase shift around the amplifier and feedback network should be 0° or 360°.
2. The magnitude of the product of the open loop gain of the amplifier (A) and feedback factor β must be unity. i.e., $|A\beta| = 1$

As per first criterion, the phase of V_f is same as V_i. i.e. feedback network should introduce 180° phase shift in addition to 180° phase shift introduced by inverting amplifier. This ensures positive feedback. So total phase shift around a loop is 360°/0°. In this condition, V_f drives the circuit and without external input circuit works as an oscillator.

5.9 BJT RC PHASE SHIFT OSCILLATOR

RC phase shift oscillator is used to produce sinusoidal signal of any frequency. It consists of an inverting amplifier and a feedback network consisting of resistors and capacitors (RC) arranged in ladder fashion. Hence such an oscillator is also called ladder type RC phase shift oscillator.

5.9.1 Principle

In an oscillator, the amplifier circuit produces 180° phase shift. Hence, the feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. Thus if one RC network produces phase shift of θ = 60° then to produce phase shift of 180° such three RC networks must be connected in cascade. Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60°, thus total phase shift due to feedback is 180° (3x 60°). Such a feedback network is shown in following Fig. 5.15.

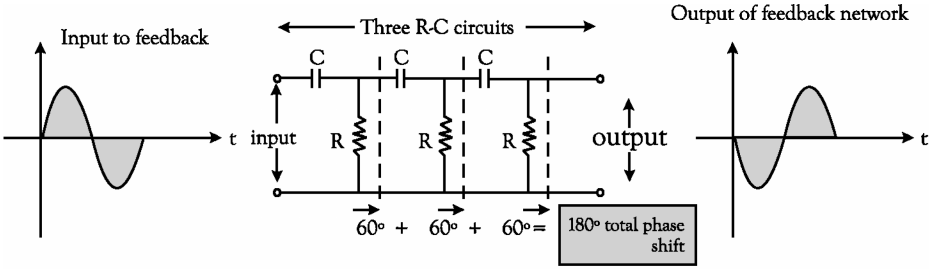


Figure 5.15 *Feedback network in RC phase shift oscillator*

In the above ladder circuit, all the resistance values and all the capacitance values are same, and by properly selecting them, for a particular frequency, each section of R and C produces a phase shift of 60°.

5.9.2 Circuit

As shown in Fig. 5.16, in a practical RC phase shift oscillator, a common emitter (CE) single stage amplifier is used as a basic amplifier. This produces 180° phase shift. The feedback network consists of 3 RC sections each producing 60° phase shift.

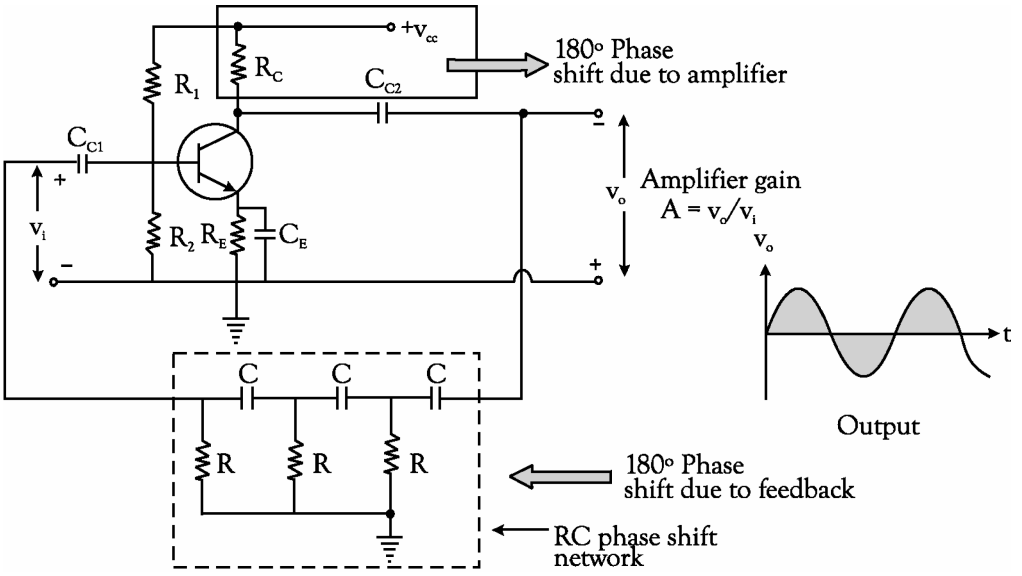


Figure 5.16 *RC phase shift oscillator using BJT*

5.9.3 Working

The output of amplifier is connected to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC sections, thus 360°. This satisfies the required Barkhausen condition for positive feedback and circuit works as an oscillator.

5.9.4 Frequency of Oscillation

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{6}\,R\,C}} \qquad \text{...(5.19)}$$

Actually to satisfy the Barkhausen condition, the expression for the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi R\,C} \cdot \frac{1}{\sqrt{6 + 4K}}} \qquad \text{...(5.20)}$$

where $K = \frac{R_C}{R}$

In practice, R_c/R is small and hence K is neglected,

The condition of h_{fe} for the transistor to obtain the oscillations is given by,

$$\boxed{h_{fe} > 4K + 23 + \frac{29}{K}} \quad \text{...(5.21)}$$

And value of K for minimum h_{fe} is 2.7 hence minimum h_{fe} = 44.5. So transistor with h_{fe} less than 44.5 cannot be used in phase shift oscillator.

5.9.5 Advantages of RC Oscillator

The advantages of R-C phase shift oscillator are :

1. The circuit is simple to design.
2. The circuit can produce output over audio frequency range.
3. The circuit can produces sinusoidal output waveform.
4. It is a fixed frequency oscillator.

5.9.6 Disadvantages of RC Oscillator

1. By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.
2. The frequency stability is poor due to the changes in the values of various components, due to effect of temperature, aging etc.

5.10 HARTLEY OSCILLATOR

Hartley Oscillator is an electronic circuit, produces sinusoidal signal. It consists two parts as (1) an amplifier and (2) a tank or tuned circuit with positive feedback.

5.10.1 Principle

In Hartley oscillator, the transistor inverting amplifier produces 180° phase difference and the tank circuit consisting of two series centre tapped inductors L_1 & L_2 in parallel with a capacitor C provides another 180° phase difference, so that there is 360°/0° phase difference along the loop with positive feedback.

5.10.2 Circuit

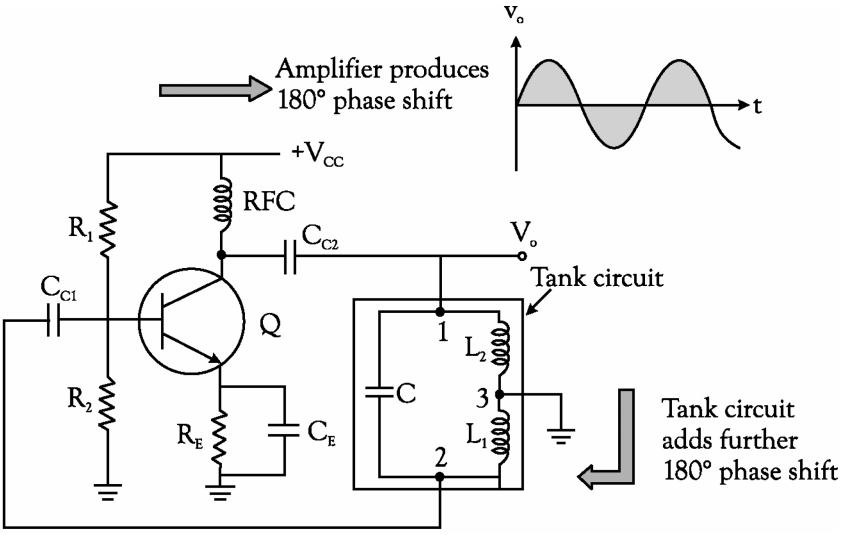


Figure 5.17 *Hartley oscillator using BJT*

The basic circuit of BJT Hartley oscillator is shown in Fig. 5.17. The resistances R_1, R_2 and R_E provide necessary bias to the circuit. The capacitors C_{C1} and C_{C2} are coupling capacitors. The feedback network consists of a tank circuit made up of two inductors L_1 and L_2 and capacitor C. The radio frequency choke (RFC) is used to achieve isolation between a.c. and d.c. operations.

5.10.3 Working

The transistor CE amplifier provides a phase shift of 180°. When V_{CC} is switched on, the capacitor C gets charged and oscillatory current is set up in the tank circuit. As the point 3 is earthed, when point 1 is positive then at the same instant point 2 is negative with respect to point 3 and vice versa. Thus there exists a phase difference of 180° between points 1 and 2. This is additional 180° phase shift introduced by tank circuit to satisfy oscillator condition. Thus when feedback is adjusted such that $A\beta = 1$, the circuit works as an oscillator. The oscillating frequency is decided by the tank circuit elements L_1, L_2 and C.

5.10.4 Frequency of Oscillation

The frequency of oscillations produced by LC tank circuit is,

$$\boxed{f = \frac{1}{2\pi\sqrt{LC}}} \qquad ...(5.22)$$

There are two inductors L_1 and L_2 in series hence equivalent inductance of the tank circuit is,

$$\boxed{L_{eq} = L_1 + L_2}$$

It should be noted that if there exists a mutual inductance M between two inductors, it must be considered while calculating equivalent inductor.

$$\boxed{L_{eq} = L_1 + L_2 + 2\,M \quad if\ M\ exists}$$

Hence the frequency of oscillations produced by Hartley oscillator is given by,

$$\boxed{f = \frac{1}{2\,\pi\sqrt{L_{eq}C}}} \qquad ...(5.23)$$

The feedback fraction = $\beta = V_f / V_o = XL_2/XL_1 = L_2/L_1$ ...(5.24)

The value of L_1 and L_2 is chosen in such a way that $A\beta = 1$ to satisfy Barkhausen second criteria.

5.10.5 Applications

The Hartley oscillators are widely used in the radio receivers as local oscillators

5.11 COLPITTS OSCILLATOR

Colpitts Oscillator is an electronic circuit, produces sinusoidal signal. It consists two parts as (1) an amplifier and (2) a tank or tuned circuit with positive feedback.

5.11.1 Principle

In Colpitt's oscillator, the transistor CE amplifier produces 180° phase difference and the tank circuit consisting of two series centre tapped Capacitors C_1 & C_2 in parallel with an inductor L provides another 180° phase difference, so that there is 360°/0° phase difference along the loop with positive feedback.

5.11.2 Circuit

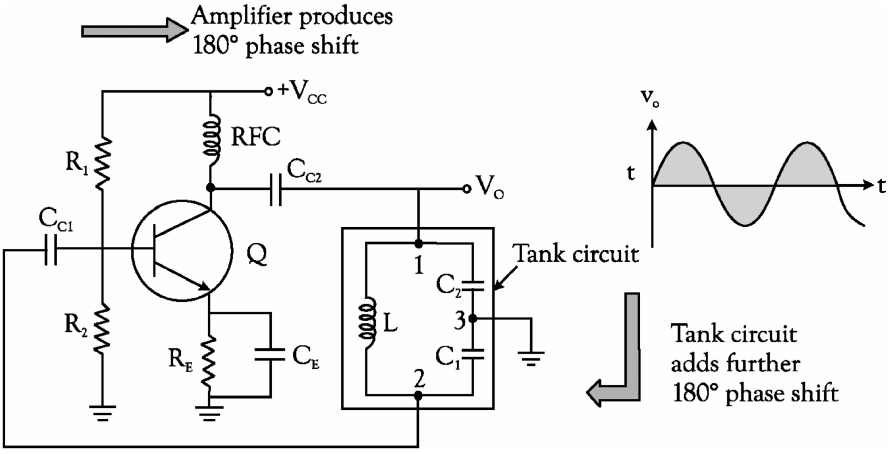


Figure 5.18 *Colpitt's oscillator using BJT*

The amplifier stage uses an active device as a transistor in common emitter (CE) configuration as shown in Fig. 5.18. The R_1 and R_2 are the biasing resistances. The resistance R_E is the stabilization resistance. The Cc_1 and Cc_2 are the coupling capacitors. The capacitive divider, C_1 and C_2 in the tank circuit provides the necessary feedback for oscillations. The RFC is radio frequency choke due to which the isolation between a.c. and d.c. operation is achieved.

5.11.3 Working

When the supply V_{CC} is switched on, the oscillatory current is set up in the tank circuit. It produces a.c. voltages across C_1 and C_2. The terminal 3 is grounded hence it is at zero potential. Thus with respect to terminal 3, when terminal 1 is positive, the terminal 2 is negative and vice versa. Hence, at any instant there exists a phase difference of 180^o between terminals 1 and 2. The amplifier produces a phase shift of 180^0 between input and output. The tank circuit adds further 180^0 phase shift between output and feedback input so that there is $360°/0°$ phase difference between output and input. This satisfies the required oscillating conditions.

5.11.4 Frequency of Oscillation

The frequency of oscillations produced by LC tank circuit is,

$$\boxed{f = \frac{1}{2\pi\sqrt{LC}}} \qquad ...(5.25)$$

But in Colpitt's oscillator there are two capacitors connected in series in tank circuit. The equivalent capacitance C_{eq} of C_1 and C_2 in series decides the frequency of oscillations.

$$\boxed{C_{eq} = \frac{C_1 C_2}{C_1 + C_2}}$$

Hence the frequency of oscillations produced by Colpitt's oscillator is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{LC_{eq}}}} \qquad ...(5.26)$$

The feedback factor = $\beta = V_f / V_o = X_{C2}/X_{C1} = C_1/C_2$ ...(5.27)

The value of C_1 and C_2 is chosen in such a way that $A\beta = 1$ to satisfy Barkhausen second criteria.

5.11.5 Applications

The Colpitt's oscillator is very commonly used as local oscillator in superheterodyne radio receiver.

5.12 CRYSTAL OSCILLATOR

A crystal oscillator generates electrical oscillations of constant frequency, based on Piezoelectric property of the crystal used in the circuit. The frequency of the oscillation is exactly equal to the resonant frequency of the crystal.

5.12.1 Principle

Some crystals in nature, like quartz, exhibit the Piezo-electric effect. The Piezo-electric effect is an effect in which the application of pressure on the faces of a crystal results in an electric charge on these faces. In such crystals, if we apply some potential, the crystal wafer gets contract by reducing the distance between the two faces. Also when the potential is reversed, the wafer expands by increasing the distance between the faces. If an alternating voltage is applied to the crystal wafer, it will vibrate at a frequency called **resonant frequency** of the crystal. The resonant frequency depends on the cut of the crystal with respect to the mechanical axis of it.

When an ac voltage is applied across the crystal, it starts vibrating in its fundamental resonant frequency, and it looks like an equivalent tuned circuit as shown in Fig. 5.19

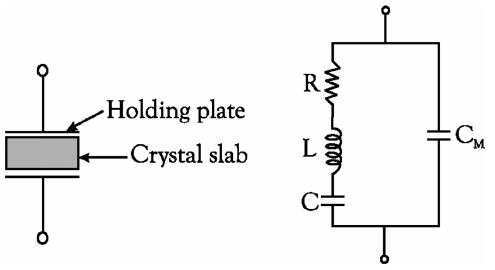


Figure 5.19 *(a) Piezoelectric crystal and (b) its equivalent circuit*

When the crystal is not vibrating, it is equivalent to a capacitance due to the mechanical mounting of the crystal. Such a capacitance existing due to the two metal plates separated by a dielectric like crystal slab, is called **mounting capacitance** denoted as C_M (Fig 5.19 (a)).

When the crystal is vibrating, there are internal frictional losses which are denoted by a resistance R and the mass of the crystal, which is the indication of its inertia is represented by an inductance L. In vibrating condition, it is having some stiffness, which is represented by a capacitor C. The mounting capacitance is a shunt capacitance. Hence, the overall equivalent circuit of a crystal can be shown as in the Fig. 5.19 (b).

5.12.2 Circuit

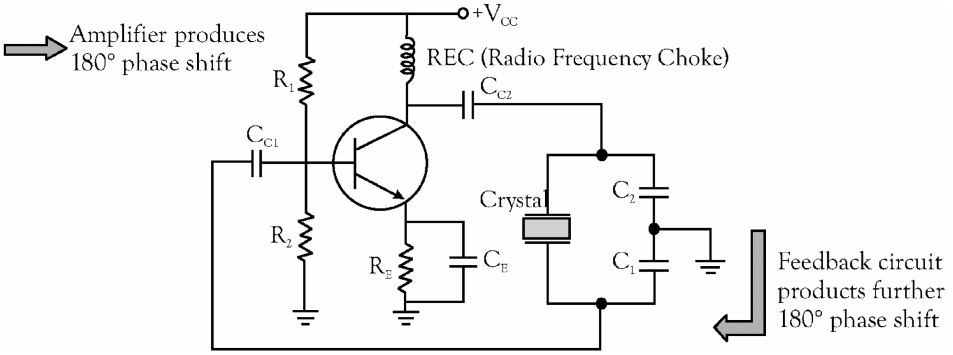


Figure 5.20 *Pierce crystal oscillator*

The **Colpitts** oscillator can be modified by using the crystal to behave as an inductor. The circuit is called Pierce crystal oscillator (Fig. 5.20). The crystal behaves as an inductor for a frequency slightly higher than the series resonance frequency f_r. The two capacitors C_1, C_2 required in the tank circuit along with a crystal as an inductor are used, as they are used in **Colpitts** oscillator circuit. As only inductor gets replaced by the crystal, which behaves as an inductor, the basic working principle of Pierce Crystal Oscillator is same as that of **Colpitts** oscillator.

5.12.3 Working

The resistors R_1 and R_2 form a voltage divider across V_{cc} for providing DC bias and R_E is for emitter stabilization. Capacitor C_E bypasses R_E in order to have a large voltage gain. RFC coil prevents AC signals from entering the DC line and also acts as the DC load of the collector. The coupling capacitor C_C has negligible impedance at the operating frequency, but prevents any DC link between collector and base.

The crystal frequency can be varied somewhat (by about 0.1 percent by means of an inductor or capacitor in parallel with the crystal. But the frequency is determined mainly by the thickness of the quartz wafer, and by the angle at which it is cut from the original quartz sample.

Because of a very high degree of stability of crystal oscillations, such oscillators are extensively employed in communication transmitters and receivers, where frequency stability is extremely important.

5.12.4 Frequency of Oscillation

The expression for the series resonating frequency f_s is,

$$\boxed{f = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}}} \qquad ...(5.28)$$

where Q = quality factor of crystal

$$\therefore \quad \boxed{Q = \frac{\omega L}{R}} \qquad ...(5.29)$$

The Q factor of the crystal is very high, typically 20,000. Value of Q upto 10^6 also can be achieved. Then the second factor in resonant frequency equation (eqn. 5.28) approaches unity. As a result, the Eqn (5.28) becomes:

$$\boxed{f_r = \frac{1}{2\pi\sqrt{LC}}} \qquad ...(5.30)$$

Since the resonant frequency of the crystal is inversely proportional to the thickness of the crystal, and as the thickness of the crystal decreases with increase in frequency and gets brittle and susceptible to break, crystal oscillators are used at low frequency upto 200 KHz. to 300 KHz only.

5.12.5 Series and Parallel Resonance

When the crystal capacitance C is much smaller than C_M, then the behaviour of crystal impedance versus frequency is shown in Fig. 5.21.

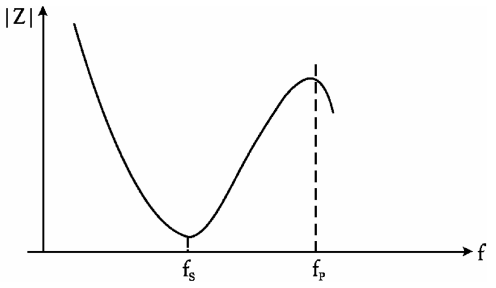


Figure 5.21 *Crystal impedance versus frequency*

One resonant condition occurs when the reactance of series RLC path are equal i.e. $X_L = X_C$. This is the series resonance condition. The frequency of oscillation at series resonance is:

$$\boxed{f_S = \frac{1}{2\pi\sqrt{LC_{eq}}}} \qquad ...(5.31)$$

The other resonant condition occurs when the reactance of series resonant path equals the reactance of the mounting capacitor C_M. This is parallel resonance condition.

Under parallel resonance, the equivalent capacitance is,

$$C_{eq} = \frac{C_M C}{C_M + C}$$

Hence the parallel resonating frequency is given by,

$$\boxed{f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}} \qquad ...(5.32)$$

5.12.6 Advantages

(1) It is a very simple circuit because no tuned circuit other than the crystal itself is required.

(2) The Quality Factor (Q) of the Crystal is very high. It may be over 10,000 as compared to 100 of an LC Tank Circuit.

(3) Due to the high Q of crystal, oscillators with very stable values of frequency are possible.

(4) In a crystal oscillator, frequency drift with time is very small.

(5) Different oscillation frequencies can be obtained by simply replacing one crystal with another. This makes it easy for a radio transmitter to work at different frequencies.

(6) Since frequency of oscillation is set by the crystal, it remains unaffected by changes in supply voltage, transistor parameters etc.

5.12.7 Disadvantages

(1) Crystals are fragile and therefore can be used for only low power circuits.

(2) The frequency of oscillations cannot be changed appreciably.

5.12.8 Difference between Crystal Oscillator and Other Oscillators

(1) Crystals have a very high Q value as compared to discrete *LC* tank circuits of oscillators (over 10,000 as against over 100).

(2) Due to high Q value of crystal, crystal oscillators have much more stable values of frequency than other oscillators.

(3) In a Crystal Oscillator, frequency drift with time is very small as compared to the drift in other oscillators.

SOLVED PROBLEMS

1. *A negative feedback amplifier has an open loop gain of 300 and a feedback factor of 0.1. If the open-loop gain changes by 10% due to temperature, find the percentage change in closed- loop gain.*

Solution:

Given: $A_v = 300$ and $\beta = 0.1$

(i) Closed loop gain = $A_f = A_V / (1 + A_V\beta) = 300 / (1 + (300 \times 0.1)) = 9.677$

(ii) If A_V decreases 10 %, new $A_V = 270$;

Then, $A_f = A_V / (1 + A_V\beta) = 270 / (1 + (270 \times 0.1)) = 9.643$

(iii) If A_V increases 10 % new $A_V = 330$

Then, $A_f = A_V / (1 + A_V\beta) = 330 / (1 + (330 \times 0.1)) = 9.706$

It is observed that while the open-loop amplifier gain varies by ±10%, the amplifier gain with feedback varied by only ± 0.35%, *i.e.*, an improvement of 10/0.35 = 29 times.

2. *A phase shift oscillator has 3 similar phase–advancing sections, each containing a 100 KΩ resistor and a 0.0005μF capacitor. Calculate the frequency of oscillations.*

Solution:

Given: Resistor $R = 100\ K\Omega = (100 \times 10^3)$ ohms, Capacitor $C = 0.0001\ \mu F = (0.0001 \times 10^{-6})$ Farads.

Frequency of Oscillations: $f = 1/(2\pi\sqrt{6}\,RC) = 1/ (2 \times 3.14 \times \sqrt{6} \times 100 \times 10^3 \times 0.0001 \times 10^{-6}) = 6500$ Hz.

3. *Estimate the values of R and C for an output frequency of 1 KHz in a RC Phase-Shift Oscillator.*
(March 99, V.T.U.)

Solution:

Given: f = 1 KHz = 10^3 Hz

Frequency of Oscillations : $f = 1/(2\pi\sqrt{6}\,RC)$

Let R = 100 KΩ = 10^5 Ω

$$\therefore \qquad 10^3 = \frac{1}{2\pi\sqrt{6}\times 10^5 \times C}$$

$$\therefore \qquad C = \frac{1}{10^3 \times 2\pi\sqrt{6}\times 10^5} = \frac{10^6}{10^8 \times 2\pi\sqrt{6}}\ \mu F = 0.00065\ \mu F$$

4. *For a transistor Colpitt's Oscillator, L = 100 micro henry, C_1 = 0.005 micro farad and C_2 = 0.01 micro farad. Calculate the frequency of oscillations generated.*

Solution:

Given: L = 100 μH = 100 x 10^{-6} H

The frequency of oscillation is given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{C_1 C_2}{C_1 + C_2} = \frac{\left(0.005\times 10^{-6}\right)\left(0.01\times 10^{-6}\right)}{10^{-6}\left(0.005+0.01\right)} = 0.00333\times 10^{-6}\ \text{Farad}$$

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{\left(100\times 10^{-6}\right)\left(0.00333\times 10^{-6}\right)}}$$

$$= 0.276 \times 10^6\ \text{Hz} = 0.276\ \text{MHz}$$

5. *In a Colpitt's Oscillator if the desired frequency is 500 KHz, estimate the values of L and C.*
(Mar 99, V.T.U)

Solution:

The frequency of oscillation is given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

or $$\sqrt{LC} = \frac{1}{2\pi f} = \frac{1}{2\pi \times (500 \times 1000)} = \frac{1}{\pi \times 10^6}$$

or $$LC = \frac{1}{\pi^2 \times 10^{12}} \quad ...(i)$$

Let us assume that C = 1000 pF. Thus, substituting in eqn (i) above,

$$L(1000 \times 10^{-12}) = \frac{1}{\pi^2 \times 10^{12}}$$

or L = 0.0000101 H = 10.1 μH.

Hence the estimated values are C = 1000 pF and L = 10.1 μH

6. *In a Collpitt's Oscillator, $C_1 = C_2 = C$ and L = 100 μH, frequency of oscillation = 500 KHz. Determine C.*

Solution:

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad ...(i)$$

where $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

Given: $C_1 = C_2 = C$ and L= 100 μH, frequency of oscillation = 500 KHz.

$\therefore$ $$C_{eq} = \frac{C \times C}{C + C} = 0.5C$$

Substituting the values in Eqn. (i),

$$500 \times 10^3 = \frac{1}{2\pi\sqrt{(100 \times 10^{-6})(0.5C)}}$$

or $$500 \times 10^3 = \frac{1}{2\pi \times 10^{-3}\sqrt{(50C)}}$$

or $$\sqrt{(50C)} = \frac{1}{2\pi \times 500}$$

$\therefore$ C = 0.002 μF

7. *Calculate the period of oscillations of a Hartley Oscillators having L_1 = 1 mH, L_2 = 2 mH and C = 0.1 microfarad.*

Solution:

Given:

L_1 = 1 mH = 1 x 10^{-3} Henry, L_2 = 2 mH = 2 x 10^{-3} Henry, C = 0.1 μF = 0.1 x 10^{-6} Farad

Formula :

$$\text{Frequency} = f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}$$

$$= \frac{1}{2\pi\sqrt{(0.1\times10^{-6})(3\times10^{-3})}} = 9192 \text{ Hz}$$

∴ Period of oscillations T = 1/f = 1/9192 = 0.00011 Sec = 110 μs

EXERCISES

I. Descriptive Type Questions

1. What is an Amplifier ? Explain classification schemes of Amplifiers?
2. Describe Decibel in terms of power, voltage and current?
3. Explain various characteristics of decibel system?
4. Write a note on variation of Amplifier gain with frequency?
5. What is 3 dB frequency and Half-power point?
6. Explain α and β cut-off frequencies?
7. With circuit diagram, explain the working of RC coupled single stage CE amplifier? Also explain the use of various biasing components used in the circuit?
8. List various characteristics and uses of CE single stage amplifier?
9. With a neat circuit diagram, obtain expressions for various currents in single stage RC coupled CE amplifier? Draw its frequency response curve? *(VTU Jan 2009, VTU Jan 2010)*
10. Using ac equivalent circuit of CE amplifier, obtain expression for Input impedance, Output impedance, Voltage gain and Current gain of a single stage RC coupled CE amplifier?
11. Write a note on Capacitor coupled two stage CE amplifier? *(VTU June 2008)*
12. Explain the principles of negative feedback in amplifiers?
13. List the advantages of negative feedback in amplifiers? *(VTU Jan 2010)*
14. Explain in detail, various types of negative feedback?
15. Explain in detail, the effect of negative feedback on (a) gain, (b) bandwidth (c) input impedance and (d) output impedance of an amplifier? *(VTU Jan 2008)*
16. Explain in detail, the effect of negative feedback on (a) decibel, (b) harmonic distortion (c) attenuation (d) Phase shift and (e) circuit noise?
17. What is an Oscillator?
18. How do you compare Amplifiers & Oscillators? Explain various classification schemes of Oscillators?
19. With a block diagram of an Oscillator with feedback, explain Barkhausen Criterion? *(VTU June 2008)*
20. With principle and neat circuit diagram, explain the working of RC Phase-shift Oscillator. Obtain an expression for frequency of oscillation? Also list the advantages and disadvantages? *(VTU Jan 2009)*

21. With principle and neat circuit diagram, explain the working of Hartley Oscillator. Obtain an expression for frequency of oscillation? What are its applications? *(VTU June 2009)*
22. With principle and neat circuit diagram, explain the working of Colpitt's Oscillator. Obtain an expression for frequency of oscillation? What are its applications?
23. Write a note on crystal Oscillators?
24. What are the advantages of crystal oscillators over other oscillators?
25. With a neat circuit diagram, explain the working of single stage RC coupled amplifier, and thus draw frequency response curve and explain the curve. *(VTU Jan 2010)*
26. List and explain the advantages of negative feedback in amplifiers. *(VTU Jan 2010)*
27. Explain with neat block diagram, Barkhausen criterion to generate oscillations, with special reference to the condition $A\beta < 1$, $A\beta > 1$, $A\beta = 1$. *(VTU July 2007).*
28. Compare positive feedback amplifier with negative feedback amplifier with the help of a neat block diagram. *(VTU Jan 2007).*

II. Multiple Choice Questions

1. An audio amplifier works over the frequency range _____
   (a) 20 Hz to 20 KHz (b) 20 Hz to 1 MHz
   (c) 1 KHz to 4 KHz (d) None of these
2. An oscillator requires _____ feed back for its operations
   (a) Negative (b) Positive
   (c) High (d) Low
3. The frequency of a Hartley oscillator for $L_1 = L_2 = 60$ mH and C = 200 pF is _____
   (a) 50.3 KHz (b) 100 KHz
   (c) 150 KHz (d) None of these
4. The conditions $A\beta = 1$ for oscillations is known as the _____ criterion
   (a) Nyquist's (b) Barkhaular
   (c) Routh–Horwitz (d) None of these
5. The stability of an amplifier _____ with negative feedback.
   (a) Improves (b) Deteriorates
   (c) is Not affected (d) Depends on amount of negative feed back
6. The Barkhausen criterion states that _____
   (a) $A = \beta$ (b) $A = 1/\beta$
   (c) $A.\beta = 1$ (d) $A\beta = 0$

7. In an Oscillator we use _____ feedback
   (a) Positive (b) Negative
   (c) Neither (d) Unity Gain
8. The input capacitor in CE amplifier blocks _____
   (a) AC signal (b) DC signal
   (c) Both AC & DC signal (d) Noise of a particular frequency
9. Negative feedback results in _____ bandwidth.
   (a) Increased (b) Decreased
   (c) Zero (d) None
10. The frequency of Hartley oscillator is given by f = _____
    (a) $1/ (2\pi\sqrt{LC})$ (b) $1/ (2\pi\sqrt{RC})$
    (c) $1/ (2\pi\sqrt{C})$ (d) $1/ (2\pi LC)$
11. The overall voltage gain of two stage capacitor coupled CE amplifier is _____ than a single stage CE amplifier.
    (a) Greater (b) Less
    (c) Equal (d) None
12. The gain of the feedback amplifier depends only on _____
    (a) The gain of the amplifier (b) The feedback network
    (c) Both (a) and (b) (d) None of these
13. Negative feedback can _____
    (a) Stabilizes the gain (b) Provides constant gain for all the frequencies
    (c) Increases the bandwidth (d) All of these
14. Negative feedback can _____
    (a) Increases the input resistance (b) Decreases the output resistance
    (c) Both (a) and (b) (d) None of these
15. The feedback network should introduce 180° phase shift to ensure _____
    (a) Positive feedback (b) Negative feedback
    (c) Both (a) and (b) (d) None of these
16. Barkhausen Criterion for oscillation is _____
    (a) Total phase shift between input signal and feedback signal should be 0° or 360°
    (b) $|A\beta| = 1$ (c) Both (a) and (b)
    (d) None of these

17. The decibel is the unit of ——
    (a) power (b) voltage
    (c) current (d) power level
18. One decibel represents a power ratio of _____
    (a) 1.26 (b) 0.707
    (c) 28 % (d) Both (a) & (c) are correct
19. Decibel system is a ——— system of comparing two physical quantities.
    (a) Log based system (b) Exponential system
    (c) Comparative system (d) Systematic system
20. The output voltage of an amplifier is measured as 1 V at 5 KHz, and as 0.707 V at 20 KHz. The output power change is _____
    (a) 1 dB (b) – 1 dB
    (c) – 3 dB (d) + 3 dB
21. The following oscillator gives stable output frequency signal _____
    (a) Phase Shift oscillator (b) Colpitts Oscillator
    (c) Crystal Oscillator (d) Hartley Oscillator
22. Which of the following oscillator can produce audio frequency signal
    (a) Phase Shift oscillator (b) Colpitts Oscillator
    (c) Crystal Oscillator (d) Hartley Oscillator
23. The property of the crystal used in crystal oscillator is _____
    (a) Negative feed back (b) Positive feedback
    (c) Piezoelectric property (d) Mounting capacitance
24. In two stage CE amplifier, the total gain is _____
    (a) Sum of the gains individual stages
    (b) Difference of the gains individual stages
    (c) Product of the gains individual stages
    (d) Ratio of the gains individual stages
25. CE amplifier produces _____
    (a) 90° Phase difference between input and output
    (b) 180° Phase difference between input and output
    (c) 360° Phase difference between input and output
    (d) 0° Phase difference between input and output

III. Numerical Problems

1. The output voltage of an amplifier is maximum at 10 V at 5 KHz and 7.07 V at 25 KHz. Calculate the decibel change in output power level. **(Ans : – 3 dB)**
2. A negative feedback amplifier has an open loop gain of 400 and a feedback factor of 0.1. If the open-loop gain changes by 20% due to temperature, find the percentage change in closed-loop gain. **(Ans : A_v = 9.75, Percentage change = 40 times)**
3. A three-section ladder-type phase shift oscillator has 3 similar phase - advancing sections, each containing a 100 KΩ resistor and a 0.0005 μF capacitor. Calculate the frequency of oscillations.
4. For a *RC* phase-shift oscillator, the phase-shift network uses resistances *R* = 2.2 K ohms and a capacitor C = 0.47 microfarads. Find the frequency of oscillations.
5. In a phase-shift oscillator, if the phase shift network uses *R* = 3.3 KΩ and C = 0.47 microfarads, find the frequency of oscillations.
6. Estimate the values of R and C for an output frequency of 1 KHz in a *RC* Phase-Shift Oscillator.
7. Calculate the frequency of oscillations of Colpitts Oscillator having C_1 = C_2 = 1000 Pico-farads and L = 1 mH in the tank circuit. **(Ans : 0.2251 MHz)**
8. For a transistor Colpitts Oscillator, *L* = 100 microhenry, C_1 = 0.005 microfarad and C_2 = 0.01 microfarad. Calculate the frequency of oscillations generated. **(Ans : 0.276 MHz.)**
9. Calculate the frequency of oscillations of a Colpitts Oscillator with C_1 = C_2 = 500 pF and L = 1 mH. **(Ans : = 318.471 KHz.)**
10. Determine the frequency of oscillation of a Colpitts Oscillator if the parametric values of its tank circuit are C_1 = 750 pF, C_2 = 2500 pF, L = 40 mH. **(Ans : 0.1526 MHz.)**
11. Calculate the frequency of oscillations of a Colpitts Oscillator: L = 100 μH, C_1 = 100 μF, C_2 = 1000 pF. **(Ans : 0.5 MHz.)**
12. A transistor Colpitts Oscillator has C_1 = 750 pF and C_2 = 2500 pF and L = 40 μH in its resonating circuit. Determine its frequency of oscillation. **(Ans : = 1.0478 MHz)**
13. In a Colpitts Oscillator if the desired frequency is 500 KHz, estimate the values of L and C. **(Ans : = C = 1000 pF and L = 10 μH)**
14. **In a Collpitt's Oscillator, C_1 = C_2 = C and *L* = 100 μH, frequency of oscillation = 500 KHz. Determine C.**
15. **A Hartley Oscillator has L_1 = L_2 = 100 microhenries, C = 1000 pico-farads. Calculate the frequency of oscillations. (Ans : = 0.3562 MHz)**
16. **Calculate the frequency of oscillation of a Hartley Oscillator which has L_1 = L_2 = 0.1 mH and C = 0.1 microfarad. (Ans : = 35.56 KHz)**
17. **Calculate the period of oscillations of a Hartley Oscillator having L_1 = 1 mH, L_2 = 2 mH and C = 0.1 microfarad.**

18. In a Hartley Oscillator, L_1 = 100 μH, L_2 = 1 mH, and the mutual inductance between the coils is M = 20 μH; C = 10 pF. Determine its frequency of oscillation.

19. A Hartley Oscillator has tank circuit inductances $L_1 = L_2$ = 100 mH. It is required to design the oscillator to produce oscillations at 50 KHz. Obtain the exact value of the tank circuit capacitance for the above requirement. Draw the tank circuit with L and C values. **(Ans : C = 0.05 μF)**

20. **Calculate the frequency of oscillations of a Hartley oscillator having L_1 = 0.5 mH, L_2 = 1 mH, & C = 0.2 μF. (Ans : = 0.29 MHz)**

21. **In a Hartley oscillator L_1 = 20 μH, L_2 = 2 mH, and C is variable. Find the range of C if frequency is to be varied from 1 MHz to 2.5 MHz. Neglect Mutual Inductance.**

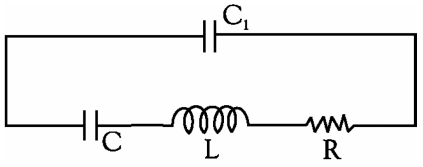
(Ans : C = 2.0244 pF & C = 12.6525 pF)

22. **In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 KHz to 2050 KHz. Calculate the range over which the capacitor is to be varied. (Ans : 2.98 pF to 13.89 pF)**

23. **The parameters of a crystal fitted in a crystal oscillator are as follows:**

L = 0.4 H, C = 0.08 pF, C_1 = 1 pF and R = 6 KΩ, Determine : (i) The Series Resonant Frequency (ii) The Parallel Resonant Frequency (iii) Q of the crystal.

Hint : $f_s = 1/(2\pi\sqrt{LC})$ and $f_p = 1/(2\pi\sqrt{LC_T})$ where $C_T = (C.C_1)/(C + C_1)$



Ans : f_s = = 0.8896 MHz, f_p = = 0.9242 MHz

24. Design a Colpitt's oscillator for a frequency of 100 KHz. *(VTU June 2009)*

25. In a Cilpitt's oscillator, if the desired frequency is 800 Hz, determine the capacitor C.

(VTU June 2008)

26. Calculate the frequency of oscillations Colpitt's oscillator having C_1 = 2000 pF, C_2 = 1000 pF and L = 4 mH. What should be the value of L if the frequency of oscillation is 140 KHz.

(VTU Jan 2008)

27. Estimate the values of R and C for an output frequency of 1 KHz in a RC phase shift oscillator. Assume R_C = 4 KΩ, V_{CC} = 12 V, β = 75. *(VTU July 2007)*

28. The gain of a transistor amplifier is 40. If positive feedback is introduced with β = 0.025, estimate the gain of the amplifier with feedback. Also estimate the gain of the amplifier if negative feedback is introduced with β = 0.025. *(VTU July 2007).*

29. Calculate the frequency of oscillations of the Hartley oscillator which has L_1 = 0.5 mH, L_2 = 1 mH, and C = 0.2 μF. What should be the value of C, if the frequency of oscillation were to be 12 KHz with other components of the circuit intact ? *(VTU Jan 2007).*

Answers to Multiple Choice Questions

1. (a)	2. (b)	3. (d)	4. (d)	5. (a)	6. (c)	7. (a)	8. (b)	9. (a)	10. (a)	11. (a)
12 (c)	13. (d)	14. (c)	15. (d)	16. (c)	17. (d)	18. (a)	19. (a)	20. (c)	21. (c)	22. (a)
23. (c)	24. (c)	25. (b).								

UNIT 6

INTRODUCTION TO OPERATIONAL AMPLIFIERS

OBJECTIVES

In this Unit we will study the constructional features, characteristics and applications of another electronic circuit called Operational Amplifier (OP-AMP) usually available in the form of Integrated Circuit (I.C.) used to amplify/control the input signal. The Unit objectives are:

(1) To study the characteristics of Ideal OP-AMP and Saturable property of an OP-AMP

(2) To study inverting and non inverting amplifier circuits using OP-AMP.

(3) To analyze the need of OP-AMP and Characteristics of practical OP-AMP.

(4) To study applications of OP-AMP as voltage follower, and for addition, subtraction, integration and differentiation.

(5) To study the construction, working and applications of Cathode Ray Oscilloscope (CRO).

6.1 INTRODUCTION

The term 'operational amplifier' describes an important amplifier circuit that can form the basis of audio and video amplifiers, filters, buffers, line drivers, instrumentation amplifiers, comparators, oscillators, and many other analogue circuits. The operational amplifier is commonly referred to as an OP-AMP and mainly used for voltage amplification. Although the OP-AMP circuit can be designed from discrete components, it is almost always used in integrated circuit (IC) form.

The OP-AMP is a simple building block. It has two inputs, one is called the inverting input (often labelled as –) and the other is called the non-inverting input (often labeled as +). Usually OP-AMPs have a single output, but special OP-AMPs used in radio frequency circuits have two outputs. Only single output devices will be described in detail, and the symbol used in circuit diagrams and the pin configuration are shown in Fig. 6.1.

The OP-AMP also has two power supply connections, one for the positive rail and another for the negative rail. The OP-AMP is a high gain DC amplifier (the DC gain is usually >1,00,000; or >100 dB). With suitable capacitive coupling, the OP-AMP is used in many AC amplifier circuits. In an OP-AMP, the output voltage is simply the difference in voltage between the inverting and non-inverting inputs, multiplied by the gain. Thus, the OP-AMP is a differential amplifier. If the inverting (–) input has the

higher voltage, the output voltage will become more negative. If the non-inverting (+) input has the higher voltage, the output will become more positive. Since the gain is very high, the differential voltage between the input terminals is usually very small.

The OP-AMP must have feedback in order to perform useful functions. Most designs use negative feedback to control the gain and to provide linear operation. Negative feedback is provided by components, such as resistors, connected between the OP-AMP's output and its inverting (–) input. Nonlinear circuits, such as comparators and oscillators, use positive feedback by having components connected between the OP-AMP's output and its non-inverting (+) input.

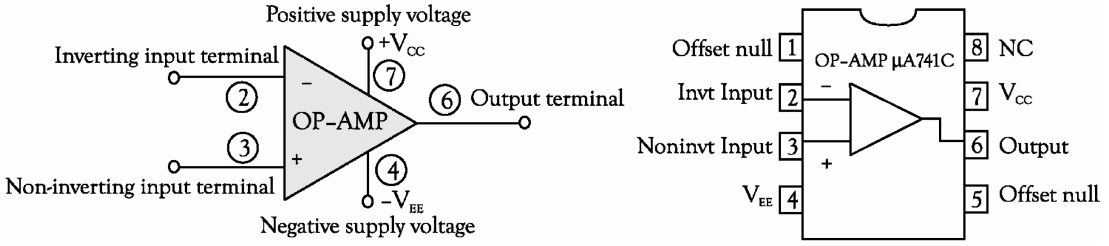


Figure 6.1 *OP-AMP symbol and pin-configuration*

6.2. OP–AMP CHARACTERISTICS

1. Differential Gain (A_d)

The output voltage of an OP–AMP is equals to the gain times the difference between the input voltages. This gain is called differential gain.

Let V_1 is the input voltage applied to non-inverting terminal and V_2 is the voltage applied the inverting terminal of OP–AMP. Then $V_O = A_d(V_1 - V_2)$ ...(6.1)

where A_d is called Differential gain.

2. Common Mode Gain (A_{CM})

It is the gain of an OP–AMP when the difference between input voltage applied to non-inverting terminal and the input voltage applied to inverting terminal is equal to zero. It is a negative quantity.

$$A_{CM} = \frac{V_{OCM}}{V_{CM}} \qquad ...(6.2)$$

where common mode voltage, $V_{CM} = V_1 = V_2$ when $V_1 = V_2$ and V_{OCM} is output voltage when input is common mode voltage.

3. Common Mode Rejection Ratio

It is defined as the ratio of differential voltage gain to common mode voltage gain.

$$CMRR = \frac{A_d}{-A_{CM}} \qquad ...(6.3)$$

where, the negative sign is included to get a positive ratio. For instance, if A_d = 200 and A_{CM} = –0.5, then CMRR = 200/0.5 = 400. Also, CMRR (dB) = 20 $\log_{10}$ CMRR. Typical value of CMRR range between 80 to 100 dB.

6.3 IDEAL OP–AMP

When analyzing feedback circuits, it is convenient to assume that the amplifier has certain ideal characteristics.

1. The output of the ideal differential amplifier depends only on the difference between the voltages applied to the two input terminals.
2. The performance is entirely dependent on input and feedback networks.
3. No current flows into the amplifier input terminals.
4. The frequency response extends from zero to infinity, ensuring a response to all DC and AC signals, with zero response time, and no phase change with frequency.
5. The amplifier is unaffected by the load.
6. When the input signal voltage is zero, the output signal will also be zero – regardless of the input source resistance.

An ideal OP–AMP has an equivalent circuit shown in Figure 6.2. It is a difference amplifier, with output equal to the amplified difference of the two inputs.

An ideal OP–AMP has the following properties:

(1) Infinite input resistance, R_i, so that almost any signal source can drive it and there is no loading of preceding stage.

(2) Zero output resistance, R_O, so that output can drive an infinite number of other devices.

(3) Zero offset voltage, so that output voltage is zero when input voltage is zero.

(4) Infinite bandwidth so that signals of frequency from 0 to ∞ Hz can be amplified without attenuation.

(5) Infinite common-mode rejection ratio so that the output common mode noise voltage is zero.

(6) Infinite open-loop voltage gain, A_d

(7) Infinite Slew rate so that the output voltage changes occurs simultaneously with the input voltage change.

A practical OP-AMP will have large but finite open-loop gain in the range from 10^5 to 10^9. It also has a very large input resistance 10^6 to 10^{10} ohms and low output resistance in the range of 50 to 125 ohms. The offset voltage is small but finite and the frequency response will deviate considerably from the infinite frequency response. The common-mode rejection ratio is not infinite but finite.

6.4. SATURABLE PROPERTY OF AN OP–AMP

Consider the circuit of Fig. 6.2. The output, $A_d(V_2 - V_1)$, reduces to either A_dV_2 or A_dV_1 depending on whether V_1 or V_2 is zero. Although A is ideally infinite, the output of an OP–AMP does not vary

from + ∞ to – ∞; rather, it is limited by the magnitude of power supply voltage. If the supply voltages are ±15 V, the output is limited to approximately ±l4 V. Once the output reaches this level, it does not increase further even if the input voltages are increased. The amplifier is then considered to be saturated. This property of an OP–AMP is used as comparator for comparing two voltages. However, for other applications of OP–AMP, a feedback circuit from output to input of OP–AMP is commonly used.

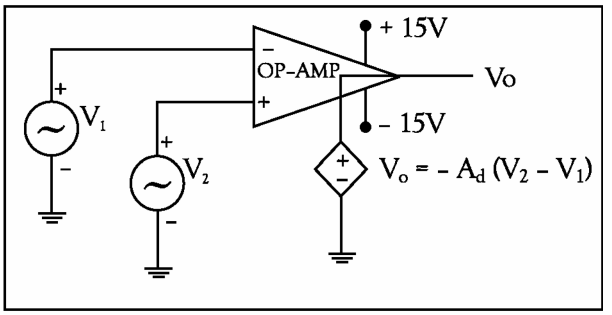


Figure 6.2. *Differential amplifier using OP–AMP*

6.4.1 OP–AMP Comparator

In a comparator circuit, the saturable property of OP–AMP is used as principle.

Circuit:

The circuit diagram of OP–AMP Comparator is shown in Fig. 6.3. In this circuit, a reference voltage V_{ref} applied to one of its input and the voltage to be compared with reference voltage is applied to other input. The output voltage which compared voltage is held at the positive or negative saturation voltage.

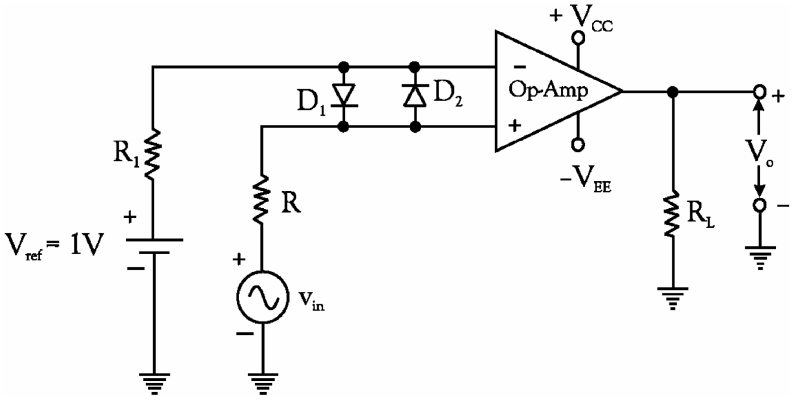


Figure 6.3 *Comparator circuit using OP-AMP*

Working

A time-varying signal V_{in} is applied to the non-inverting terminal through a resistor *R*, and the reference voltage V_{ref} of 1 V is applied to the inverting terminal through resistor R_1. When $V_{in} < V_{ref}$, the voltage at the inverting (–) terminal is greater than the voltage at the non-inverting (+) terminal and hence $Vo = -V_{sat}$, it being approximately equal to $- V_{EE}$.

When $V_{in} > V_{ref}$, the voltage at the non-inverting (+) terminal is greater than the voltage at the inverting (–) terminal and hence $V_o = + V_{sat}$, it being approximately equal to + Vcc. Therefore, when V_{in} crosses V_{ref}, the output voltage v_0 changes instantaneously from one saturation level to the other (i.e. from $+V_{CC}$ to $-V_{EE}$ or from $-V_{EE}$ to $+V_{CC}$).

Output Waveform

Waveforms of a sinusoidal input v_{in} along with the reference voltage, and the output square wave extending from + V_{sat} to – V_{sat}, as shown in Fig. 6.4 (a) and (b). Diodes D_1 and D_2 are used to protect the OP–AMP against excessive input voltages.

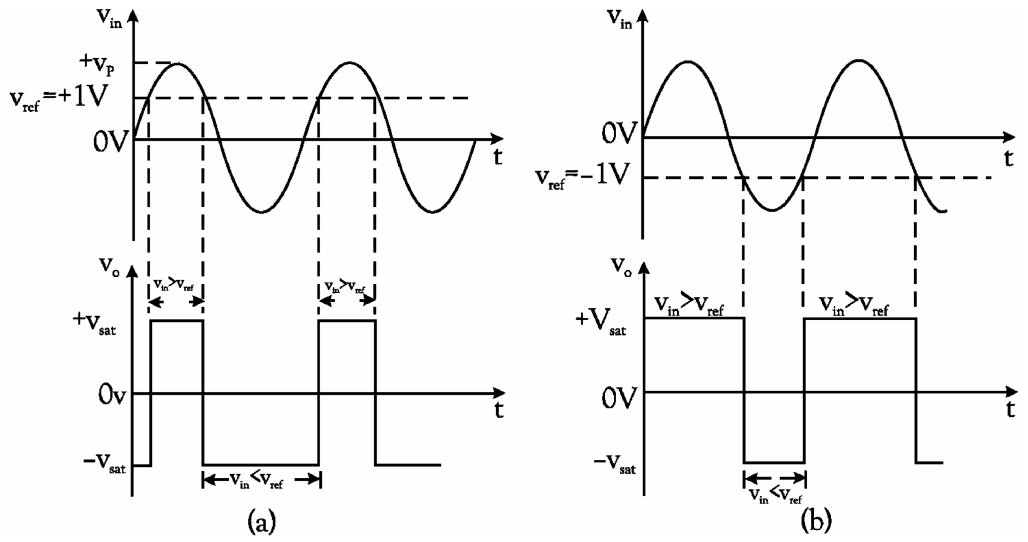


Figure 6.4 *Input and output waveforms of a comparator for (a) V_{ref} is positive (b) V_{ref} is negative*

Since the reference voltage is connected to the inverting terminals, the comparator is identified as a non-inverting comparator. If the reference voltage is zero, the circuit functions as a zero crossing comparator or detector. On the other hand, if the reference voltage is connected to non-inverting terminal, the comparator is identified as inverting comparator.

6.5 INVERTING AND NON INVERTING OP–AMP CIRCUITS

6.5.1 Inverting OP–AMP Circuit

An Inverting OP–AMP circuit amplifies input signal and the output is out of phase by 180° with respect to the input. The Fig. 6.5 shows an OP–AMP circuit with a very small input v_i applied to the inverting terminal and the non–inverting terminal is connected to ground.

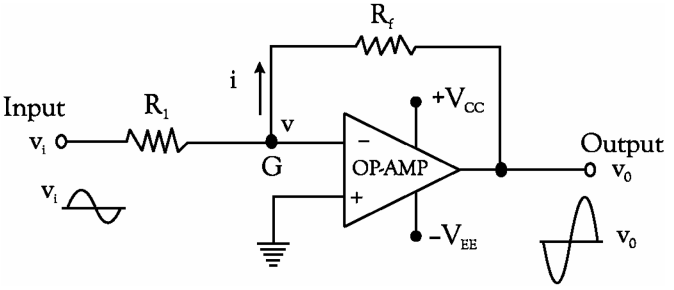


Figure 6.5 *Inverting OP-AMP circuit*

Since the non-inverting input is directly connected to ground, and the differential voltage between non-inverting and inverting input is always zero, the point G is called the **'virtual ground'**.

The current through R_1 is $$i = \frac{(V_i - 0)}{R_1} \quad ...(6.4)$$

The potential V at G = 0.

Because of the infinite input impedance of the OP–AMP, no current enters the OP–AMP. Hence the same current flows through the feedback resistor R_f.

$$i = \frac{(0 - V_0)}{R_f} \quad ...(6.5)$$

From Eqn. (6.4) and Eqn. (6.5) we get, $\frac{(V_i - 0)}{R_1} = \frac{(0 - V_0)}{R_f}$

i.e., $$\frac{(V_i)}{R_1} = -\frac{(V_0)}{R_f} \text{ or } \frac{(V_0)}{(V_i)} = -\left[\frac{R_f}{R_1}\right] \quad ...(6.6)$$

or $$V_0 = -\left[\frac{R_f}{R_1}\right] V_i \quad ...(6.7)$$

The ratio V_O/V_i is called closed loop voltage gain V_{CL} of the circuit. As there is a feedback loop, the gain is known as the *closed loop gain* and depends only on the values of the external resistances R_1 and R_f. The minus sign (–) in the above gain equation indicates that the output is inverted with respect to the input. Thus the above circuit is called as *inverting amplifier.*

6.5.2 Non-inverting OP–AMP Circuit

A Non-inverting OP–AMP circuit amplifies input signal and the output is in phase with respect to the input. The Fig. 6.6 shows an OP–AMP circuit with a very small input v_i applied to the non-inverting terminal and the inverting terminal is connected to ground through resistor R_1. R_f is feedback resistor.

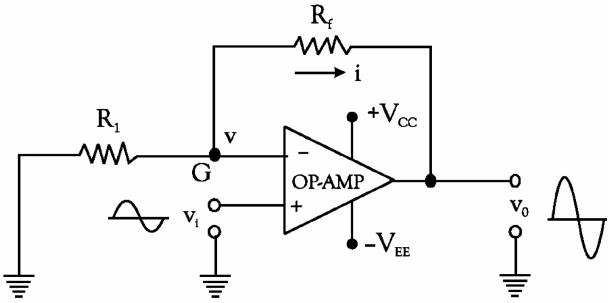


Figure 6.6 *Non-inverting OP-AMP circuit*

Due to infinite gain of OP–AMP, practically no voltage drop exists between the input terminals. Hence the potential at G is also taken to be v_i. Further, assuming no current flows through the OP–AMP, the same current i flows through R_1 and R_f. Thus we have

$$\frac{(V_i - 0)}{R_1} = \frac{(V_0 - V_i)}{R_f} \qquad ...(6.8)$$

or $$\frac{(V_0 - V_i)}{V_i} = \frac{R_f}{R_1}$$

or $$\left(\frac{V_0}{V_i}\right) - 1 = \frac{R_f}{R_1}$$

or $$\left(\frac{V_0}{V_i}\right) = 1 + \frac{R_f}{R_1} \qquad ...(6.9)$$

Hence Gain of Amplifier $= \left[1 + \left(\frac{R_f}{R_1}\right)\right]$

Since the gain is positive, there is no phase change occurs at the output signal.

6.5.3 Difference between Inverting and Non-inverting Amplifiers

(1) The sign of the closed-loop gain is negative for inverting amplifier and is positive for non-inverting amplifier.

(2) The effective input resistance that they present to the signal source V_i is different. Inverting amplifier has higher input resistance than non-inverting amplifier.

6.6 NEED FOR OP–AMP

The need of OP–AMP amplifier instead of BJT-RC coupled amplifier is illustrated bellow:

Consider a circuit as shown in Fig. 6.7, where, two signals v_1 and v_2 are added using resistors R_1 and R_2. The output is tapped across R_O, and R_L is the load resistor.

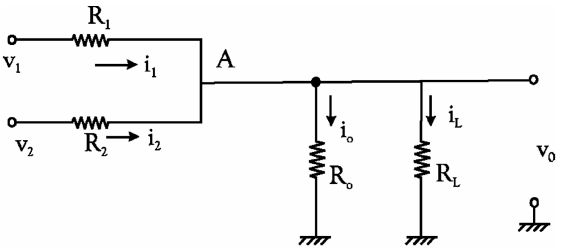


Figure 6.7 *Circuit for summing two input signals*

Application of KCL at junction A yields

$$\frac{v_1 - v_o}{R_1} + \frac{v_2 - v_0}{R_2} = \frac{v_o}{R_o} + \frac{v_o}{R_L}$$

Representing the parallel combination of R_o and R_L by R_p, we obtain

$$v_0\left[\frac{1}{R_p} + \frac{1}{R_1} + \frac{1}{R_2}\right] = \frac{v_1}{R_1} + \frac{v_2}{R_2}$$

The output voltage V_o is given by the expression

$$v_0 = \frac{v_1\left[\frac{R_P}{R_1}\right] + v_2\left[\frac{R_P}{R_2}\right]}{\left[1 + \frac{R_P}{R_1} + \frac{R_p}{R_2}\right]} \qquad \text{...(6.10)}$$

from which it is seen that V_o depends on R_L. If it is desired to make V_o independent of R_L, it is necessary to choose $R_o << R_L$. This will result in a large signal attenuation which is undesirable.

To overcome this difficulty, an amplifier with some gain must be used. However, the use of a conventional amplifier (such as RC coupled) introduces other problems. With a RC coupled amplifier one needs an infinite value of coupling capacitance if dc signals are to be amplified. Also, its value depends on the frequency or frequency components of the signal. With transformer coupling, dc signals can not be amplified. Direct coupling may be employed using difference amplifiers. However, since the gain of a single stage is limited, many stages have to be used. Moreover, the design of such a circuit requires advanced knowledge of circuit design.

Alternatively, we may use an operational amplifier - a specialized amplifier due to the fact that the closed loop gain of the OP-AMP depends only on circuit components external to it and is independent of the open loop gain, A of the amplifier. Thus OP-AMP is well suited device to overcome the problems commonly faced by conventional amplifiers.

6.7 CHARACTERISTICS AND APPLICATIONS OF OP–AMP

6.7.1 Equivalent Circuit of an OP–AMP

The circuit shows the OP–AMP parameters like input resistance, output resistance, the open loop voltage gain in terms of circuit components like R_{in}, R_o etc. The OP–AMP amplifies the difference between the two input voltages.

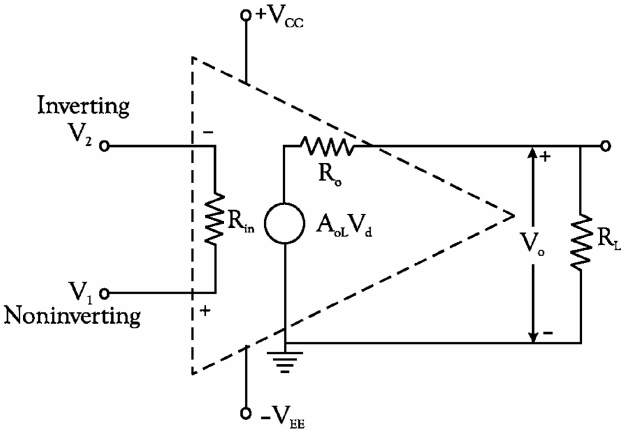


Figure 6.8 *Equivalent circuit of an OP-AMP*

$$V_O = A_{OL} V_d = A_{OL} (V_1 - V_2) \quad \text{...(6.11)}$$

A_{OL} = Large signal open loop voltage gain

V_d = Difference voltage $V_1 - V_2$

V_1 = Non-inverting input voltage with respect to ground

V_2 = Inverting input voltage with respect to ground

R_{in} = Input resistance of OP–AMP

R_O = Output resistance of OP–AMP

6.7.2 Practical OP–AMP Characteristics

Unlike the properties of an ideal OP–AMP, a practical OP–AMP possesses finite values of input resistance, gain, bandwidth, output resistance etc. These characteristics are mentioned below:

(i) Input Impedance: Input impedance of an OP–AMP is the ratio of the input voltage change to input current change, measured at one input terminal. Input impedance may be in the range of 1 MΩ to 100 MΩ.

(ii) Output Impedance: Output Impedance of an OP–AMP is the ratio of the output voltage change to output current change. Output impedance could be in the range of tens to hundreds of ohms. With the help of negative feedback it can be reduced to lower value say 1 Ω to 5 Ω.

(iii) Gain: Even though an ideal OP–AMP has infinite gain, a practical OP–AMP has a gain of the order of 5×10^4.

(iv) Common Mode Rejection Ratio (CMRR): The common-mode rejection ratio is the relative sensitivity of an OP–AMP to a difference signal as compared to a common mode signal, and is given by **CMRR** = A_d/A_{CM}, where, A_d is differential voltage gain and A_{CM} is common mode voltage gain. For commercial OP–AMPs the CMRR lies in the range 60 to 100 dB.

(v) Output Voltage Swing: This is the peak output voltage with respect to zero, available at the output without distortion. It is a function of the supply voltage. Thus, in an amplifier operating between supply voltages +6 and -6 V, the peak-to-peak undistorted output swing might be from -4 V to +4V (in practice the allowable voltage swing is not always symmetrical). The output swing is a function of the supply voltage and may range from about 50 to 80 percent of the supply voltage.

(vi) Input Common-mode Voltage Swing: This is the maximum range of input voltage that can be simultaneously applied to both inputs without causing cut off or saturation of amplifier stages. This is the maximum voltage which can be applied to the input without causing abnormal functioning or damage to the OP–AMP. It could be as high as the supply voltage but often it is limited to one-third or one-half of the supply voltage.

(vii) Input Offset Current (I_{io}): This is the difference of the currents in the input terminals when the output at zero volts. If we supply equal d.c. currents to the two inputs of an OP–AMP, then ideally we should have $V_o = 0$. In a practical amplifier, because of the lack of perfect symmetry in the input differential stage of an OP–AMP, such is not the case. To establish $V_o = 0$, we need to make the input currents different by an amount I_{io}. The current typically lies in the range of 20 to 60 nA and is measured under the condition $V_i = 0$.

(viii) Input Offset Voltage (V_{io}): Whenever both the input terminals of the OP–AMP are grounded, ideally, the output voltage should be zero. However, in this condition, the practical OP–AMP shows a small non-zero output voltage. To make this output voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals. Such a voltage makes the output exactly zero. This d.c. voltage, which makes the output voltage zero, when the other terminal is grounded is called *input offset voltage* denoted as V_{io}, which typically lies in the range 1 to 4 mV. How much voltage, to which terminal and with what polarity to be applied, is specified by the manufacturer in the data sheet. The input offset

voltage depends on the temperature.

(ix) Output Offset Voltage : The voltage existing at the output of an OP-AMP when inputs are zero is called output offset voltage and denoted as V_{oos}.

(x) Input Bias Current: Input bias current can be defined as the average current flowing into each of the two input terminals when they are biased to the same voltage level (say grounded). Typical value of input bias current is 80 nA.

(xi) Power-supply Voltage-rejection ratio: A change in one supply voltage (ΔV_{cc}) will produce a change in the amplifier output voltage (ΔV_o). The power-supply voltage-rejection ratio $\Delta V_o/\Delta V_{cc}$ by keeping V_{EE} constant, is usually specified for the condition that the difference voltage input $V_i = 0$. Typically this ratio is in the range 10^{-5} to 7×10^{-5}.

(xii) Frequency Response: OP–AMPs are usually low-frequency devices. The open-loop gain of OP-AMP at low frequency (up to 10 Hz) is very high at about 10^5 dB. At higher frequencies, the gain falls very rapidly (6 dB/octave) and becomes 0 dB (= 1) at 1 MHz.

The use of negative feedback reduces the gain, and at the same time, increases the bandwidth. So, by using feedback, it is possible to provide useful gain (which could be in the range 1 to 10) over a frequency range extending upto 10 MHz.

(xiii) Slew Rate : The slew rate is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/μ sec. Thus Slew rate = S = Max. of (dV_o/dt).

(xiv) Band width : The bandwidth of practical OP–AMP in open loop configuration is very small. By application of negative feedback, it can be increased to a desired value.

Table 6.1 shows the properties of the general purpose IC 741 OP–AMP.

Sr. No.	Parameter	Symbol	Ideal	Typical for 741 IC
1.	Open loop voltage gain	A_{DL}	∞	2×10^5
2.	Output Impedance	Z_{out}	0	75Ω
3.	Input Impedance	Z_{in}	∞	2 MΩ
4.	Input offset current	I_{ios}	0	20 nA
5.	Input offset voltage	V_{ios}	0	2 mV
6.	Bandwidth	B.W	∞	1 MHz
7.	CMRR	ρ	∞	90 dB
8.	Slew rate	S	∞	0.5 V/μ sec
9.	Input bias current	I_b	0	80 nA
10.	Power supply rejection ratio	PSRR	0	30 μV/V

Some of the basic commercially available OP-AMPs are (1) MC 1741 of Motorola Semiconductor Inc. (2) μA 741 of Fairchild semiconductor Corporation. (3) LM 741 of National Semiconductor, (4) SN52741 of TEXAS Instruments, and (5) N5741 of Signetics.

6.7.3 Voltage follower using OP–AMP

Voltage follower is an electronic circuit with unity voltage gain. Fig. 6.9 shows the OP-AMP circuit of a voltage follower. It is seen that this circuit may be derived from the general non-inverting amplifier circuit of Fig. 6.6 by setting $R_f = 0$ and $R_1 = 0$. It is easily seen, from Eq. 6.9, that voltage follower has unity gain by letting $R_f \rightarrow 0$. This means that $V_O = V_i$. One may question the usefulness of an amplifier with a gain of unity. The fact is that the voltage follower circuit is extremely useful because of its very high input resistance and low output resistance. This type of amplifier may therefore be used as a buffer to feed a low resistance load from a high resistance source.

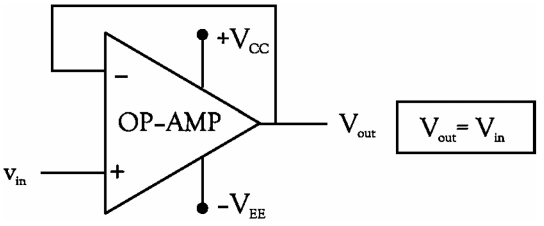


Figure 6.9 *The voltage follower*

6.7.4 Addition Using OP–AMP

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. Fig. 6.10 shows a three-input inverting adder circuit. As seen, the output voltage is phase-inverted.

Circuit

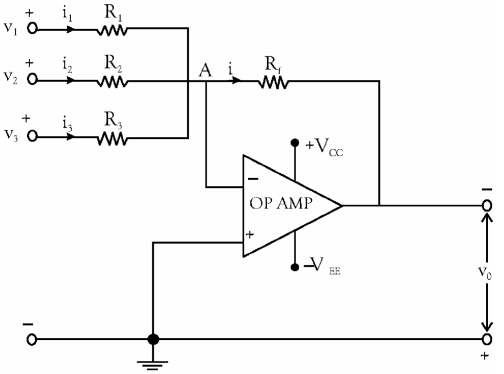


Figure 6.10 *Adder circuit*

Calculations

As before, we will treat point A as virtual ground

$$i_1 = \frac{v_1}{R_1} \text{ and } i_2 = \frac{v_2}{R_2}$$

$$i_3 = \frac{v_3}{R_3} \text{ and } i = -\frac{v_0}{R_f}$$

Applying KCL to point A, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or $$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} - \left(\frac{-v_o}{R_f}\right) = 0$$

$\therefore$ $$v_0 = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$$

The overall negative sign is unavoidable because we are using the inverting input terminal. If $R_1 = R_2 = R_3 = R$, then

$$v_0 = -\frac{R_f}{R}(v_1 + v_2 + v_3)$$

or $$v_0 = -K[v_1 + v_2 + v_3] \quad \text{...(6.12 a)}$$

where $$K = \frac{R_f}{R}$$

Hence, output voltage is proportional to *(not equal to)* the algebraic sum of the three input voltages. If $R_f = R$, then output exactly equals the sum of inputs and the circuit functions like an Adder.

However, if $R_f = R/3$, then

$$v_0 = -\frac{R/3}{R}[v_1 + v_2 + v_3]$$

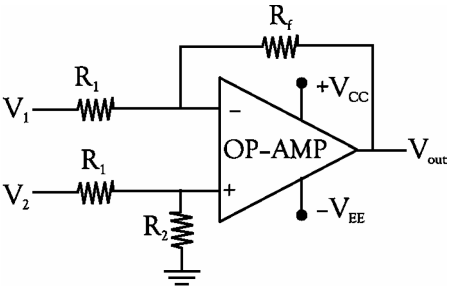
$$v_0 = -\frac{1}{3}[v_1 + v_2 + v_3] \quad \text{...(6.12 b)}$$

Obviously, the output is equal to the average of the three inputs and the circuit functions as an averager.

6.7.5 Subtraction Using OP–AMP

The function of a subtractor is to provide an output proportional to or equal to the difference of two input signals. As shown in Fig. 6.11, we have to apply the inputs at the inverting as well as non-inverting terminals.

Circuit



$$V_{out} = \frac{R_f}{R_1}(V_2 - V_1)$$

Figure 6.11 *OP–AMP Subtractor*

Calculations

According to Superposition Theorem ,

$$V_0 = V_0' + V_0''$$

where V_0' is the output produced by V_1 and V_0'' is that produced by V_2

Now, $$V_0' = - \frac{R_f}{R_1} V_1$$

$$V_0'' = \left(1 + \frac{R_f}{R_1}\right) V_2$$

$\therefore$ $$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_2 - \frac{R_f}{R_1} V_1$$

Since $R_f >> R_1$ and $\frac{R_f}{R_1} >> 1$, hence

$$V_0 \cong \frac{R_f}{R_1}(V_2 - V_1) = K(V_2 - V_1) \qquad ...(6.13)$$

Further, if $R_f = R_1$, then

$V_0 = (V_2 - V_1)$ = difference of the two input voltages and the circuit functions as a subtractor.

6.7.6 Integration Using OP–AMP

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage.

A simple example of integration is shown in Fig. 6.12(a), where input is dc voltage and its integral is *a linearly-increasing ramp voltage.*

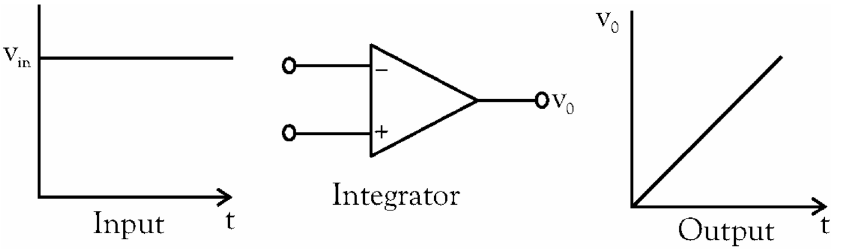


Figure 6.12 (a) *Input and output waveforms of an integrator circuit*

Circuit

The actual integrating circuit using OP–AMP is shown in Fig. 6.12 (b). The feedback component is a capacitor C_f connected between input and output.

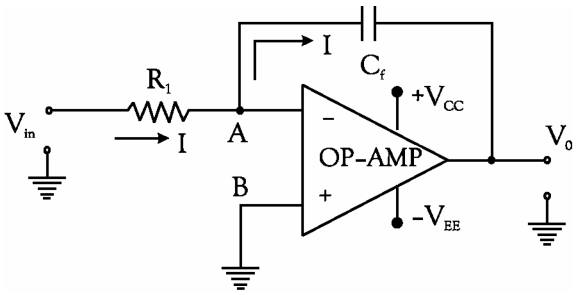


Figure 6.12 (b) *OP–AMP integrator circuit*

As input current of OP-AMP is zero, the entire current I flowing through R_1, also flows through C_f,

Calculations

From input side we can write

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \qquad \text{...(6.14)}$$

From output side we can write,

$$I = C_f \frac{d(V_A - V_o)}{dt}$$

or $$I = - C_f \frac{dV_o}{dt} \quad ...(6.15)$$

Equating the two equations (6.14) and (6.15)

$$\frac{V_{in}}{R_1} = - C_f \frac{dV_o}{dt} \quad ...(6.16)$$

Integrating both sides,

$$\int_0^t \frac{V_{in}}{R_1} dt = - C_f \int \frac{dV_0}{dt} . dt$$

i.e., $$\int_0^t \frac{V_{in}}{R_1} dt = - C_f V_o \quad ...(6.17)$$

$$\boxed{V_o = - \frac{1}{R_1 C_f} \int_0^t V_{in}\, dt + V_0(0)} \quad ...(6.18)$$

where $V_0(0)$ is the constant of integration, indicating the initial output voltage. The equation (6.18) shows that the output is $- 1/R_1C_f$ times the integral of input and R_1C_f is called time constant of the integrator.

6.7.7 Differentiation using OP–AMP

The function of a differentiator is to provide an output voltage which is *proportional to the rate of change of the input voltage.* It is an inverse mathematical operation to that of an integrator. As shown in Fig. 6.13, when we feed a ramp voltage to a differentiator, we get a constant dc voltage as output.

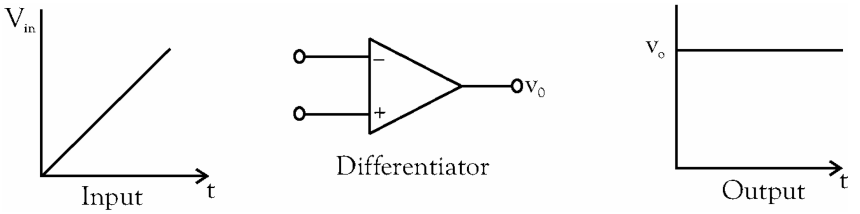


Figure 6.13 *Input and output waveforms of a differentiator circuit*

Circuit

Differentiator circuit can be obtained by interchanging the resistor and capacitor of integrator circuit as shown in Fig. 6.14. The node B is grounded. The node A is also at the virtual ground potential hence $V_A = 0$.

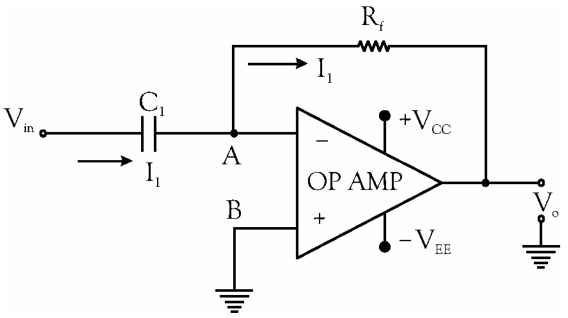


Figure 6.14 *OP–AMP differentiator*

As input current of OP–AMP is zero, entire current I_1 flows through the resistance R_f.

Calculations

From the input side we can write,

$$I_1 = C_1 \frac{d(V_{in} - V_A)}{dt} = C_1 \frac{dV_{in}}{dt} \quad \text{...(6.19)}$$

From the output side we can write,

$$I_1 = \frac{(V_A - V_o)}{R_f} = -\frac{V_o}{R_f} \quad \text{...(6.20)}$$

Equating the two equations,

$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_f} \quad \text{...(6.21)}$$

$$\boxed{V_o = -C_1 R_f \frac{dV_{in}}{dt}} \quad \text{...(6.22)}$$

The equation shows that the output is C_1R_f times the differentiation of the input and product C_1R_f is called *time constant* of the differentiator.

The negative sign indicates that there is a phase shift of 180° between input and output. The main advantage of such an active differentiator is the small time constant required for differentiation.

6.8 CATHODE RAY OSCILLOSCOPE (CRO)

The Cathode Ray Oscilloscope (CRO) is an electronic device used to display and measure electrical quantities like a.c./d.c. voltages, time phase relationships, frequency, and a wide range of waveform characteristics like rise-time, fall-time, and overshoot etc. Non-electrical quantities like pressure, strain, temperature, and acceleration etc. can also be measured by converting them into an equivalent voltage and using different transducers.

6.8.1 Block Diagram of CRO

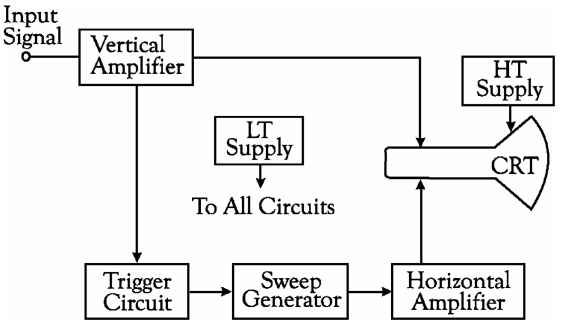


Figure 6.15 *Block diagram of CRO*

The functions of various blocks of CRO (Fig. 6.15) are explained bellow:

1. Cathode Ray Tube (CRT) : This displays the quantity being measured.
2. Vertical Amplifier: It amplifies the signal waveform which is to be displayed.
3. Horizontal Amplifier: It is fed with a sawtooth voltage, which is then impressed upon the X-plates.
4. Sweep Generator: This produces a sawtooth voltage waveform, which is used for horizontal deflection of the electron beam.
5. Trigger Circuit: This generates trigger pulses to start horizontal sweep/scan.
6. High and Low-Voltage Power Supply.

6.8.2 Operation of a CRO

A Cathode Ray Oscilloscope is a very useful and versatile laboratory instrument, used for measurement and analysis of waveforms and other phenomena of electronic circuits. It can allow viewing of signals of frequencies up to 50 MHz or so and can provide number of waveform displays simultaneously on the screen. Two signals can be compared by applying them to separate channels. CRO has the ability to hold the displays of the signal on the screen for short or long time so that the original signal may be compared with the later applied signal.

For operation as an oscilloscope, the electron beam is deflected horizontally by a sweep voltage and vertically by the voltage to be measured. While the electron beam is moved across the screen of the CRT by the horizontal sweep signal, the input signal deflects the beam vertically, resulting in a display of the input signal waveform. One sweep of the beam scanned across the screen of the tube, followed by a "blank" period during which the beam is turned off while being returned to the starting point across the tube screen, constitutes one sweep of the beam. Steady display is obtained when the beam repeatedly sweeps across the tube with exactly the same image each sweep. This requires a synchronization, starting

the sweep at the same point in a repetitive waveform cycle. If the signal is properly synchronized, the display will be stationary. In the absence of synchronization, the picture will appear to drift or move horizontally across the screen.

6.8.3 Cathode Ray Tube (CRT)

A cathode ray oscilloscope consists of a cathode ray tube (CRT), which is the heart of the oscilloscope, and some additional circuitry to operate the CRT (Fig. 6.16).

A CRT is an evacuated glass envelope of a special geometrical shape, which contains several electrodes. The cathode produces an electron beam, which is accelerated by the various electrodes into a high velocity beam called a cathode ray, which is then projected into the space of the tube, until it strikes the screen. A fluorescent material is coated to the internal portion of the screen to produce a spot of light, wherever electrons strike it. The electron beam may be deflected on its journey in any direction by appropriate magnetic or electrostatic fields.

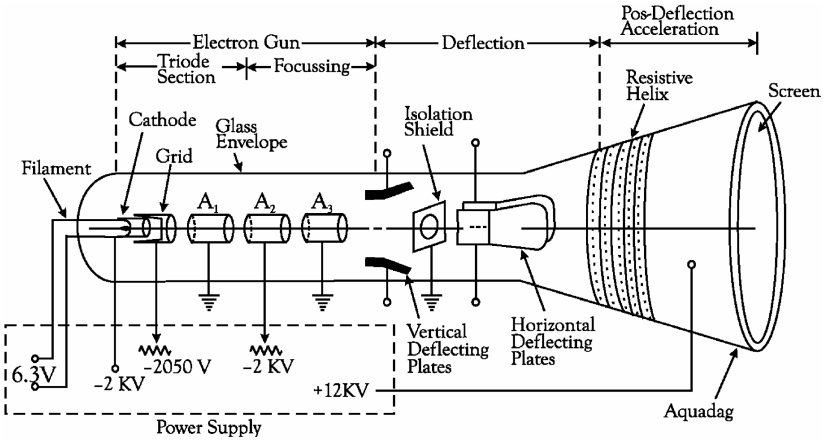


Figure 6.16 *Cathode ray tube*

The cathode ray tube consists of three sections:

(1) *The electron gun,* which produces, accelerates, and focuses the emitted electrons into a narrow beam.

(2) *The deflection system,* which deflects the electron beam either electrostatically or magnetically, in accordance with the current or voltage waveform to be displayed.

(3) *A fluorescent screen,* upon which the beam of electrons impinges, to produce a visible spot.

The Electron Gun: This consists of the Triode Section and the Focussing System.

(a) Triode Section: The grid, which is a nickel cup with a hole in it, almost completely encloses the cathode. The cathode, also made of nickel, is cylinder shaped, with a flat oxide-coated electron-emitting surface, directed towards the hole in the grid. Cathode is heated internally by a filament. The

cathode is at -2 KV, and the grid potential is adjustable from -2000 to -2050 Volts. Therefore, the grid potential controls the electron flow from the cathode, and this controls the number of electrons directed to the screen. A large number of electrons striking one point will cause the screen to glow brightly, and a small number of the same will produce a dim glow. Therefore, the grid potential controls the *brightness (or intensity)* on the screen.

The first anode, A_1 is cylinder shaped, open at one end and closed at the other end, with a hole in its centre. Since A_1 is grounded, and the cathode is at a high negative potential, A_1 is highly positive with respect to the cathode. Electrons are accelerated from the cathode, through the holes in the grid and anode, to the focusing section of the tube.

(b) Focussing Section: The focussing electrodes A_1, A_2 and A_3 are called the Electron Lens. Their function is to focus the electrons to a fine point at the screen of the tube. A_1 provides the accelerating field, to draw the electrons from the cathode, and the hole in A_1 limits the initial cross-section of the electron beam.

The Deflection System

The electron beam can be deflected either magnetically or electrostatically. However, most of practical methods uses electrostatic deflection. An electrostatic field can be produced between two metal electrodes by applying a potential difference between them.

Fluorescent Screen: If the electron beam leaving the electron gun were not deflected, it would produce a luminous spot at the centre of the fluorescent screen. The intensity of this spot can be controlled by adjusting the control grid bias voltage; but it also depends on the fluorescent material, called phosphor, coated on the inside surface of the tube.

Aquadag Coating: Some measures have to be adopted to remove the electrons from the screen and return them to the cathode, or else there will be a build-up of negative charge on the screen to such an extent that it will not allow any more electrons to reach it. The method adopted, to remove the electrons from the screen is to place a conducting coating of carbon particles, called Aquadag, along the side walls of the tube, and to connect the coating to the cathode.

6.8.4 Lissajous Figures

Lissajous figures are formed when two sine waves are applied simultaneously to the vertical and horizontal deflecting plates of a CRO. The two sine waves may be obtained from two audio-oscillators. The shape of the Lissajous Pattern depends on the frequency and phase relationships of the two sine waves. Two sine waves of the same frequency and amplitude may produce a straight line, an ellipse or a circle, depending on their phase difference (Fig. 6.17).

In general, the shape of Lissajous figures depends on :

(i) amplitude

(ii) phase difference and

(iii) ratio of frequency of the two waves.

Lissajous figures are used for:

(i) determining an unknown frequency by comparing it with a known frequency.

(ii) checking audio oscillator with a known frequency signal.

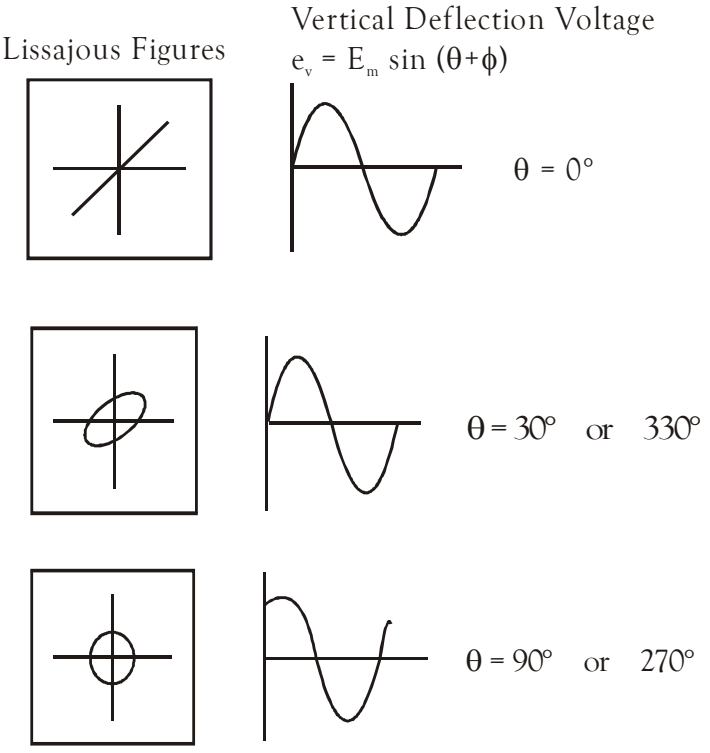
(iii) checking audio amplifiers and feedback networks for phase shift.

Measurement of Frequency using Lissajous Figures

To measure the frequency of a sine wave voltage, it is applied to one set of deflection plates of CRO. The sinusoidal voltage obtained from a standard variable frequency oscillator is applied to other set of deflection plates. The frequency of this oscillator is varied until a suitable stationary Lissajous figure is obtained. Knowing the oscillator frequency and counting the number of times the sides of the pattern are tangent to a horizontal and a vertical line, the unknown frequency can be determined.

The ratio of the two frequencies is given by:

$$\frac{f_H}{f_v} = \frac{\text{No. of points of horizontal tangency}}{\text{No. of points of vertical tangency}} \qquad ...(6.23)$$



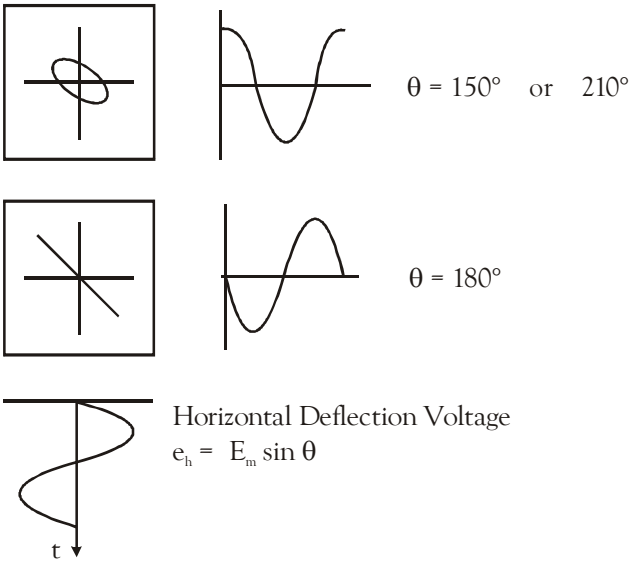


Figure 6.17 *Lissajous figures*

SOLVED PROBLEMS

1. *An Inverting Amplifier has R_1 =20 KΩ and R_f = 100 KΩ. Find the Output Voltage, the Input Resistance and the Input Current for an input voltage of 1V.*

Solution:

Formula : $V_O = - V_i (R_f/R_1)$; Input current = V_i/R_i

$V_O = - 1 (100/20) = - 5V$

$R_i = R_1$; Input current = $V_i/R_i = V_i/R_1 = 1/20$ KΩ = 0.05 mA.

2. *Design an inverting amplifier with an input resistance of 30 KΩ and a closed loop gain of –10.*

Given: Closed loop gain $A_{CL} = -10$ and $R_1 = 30$ KΩ

Formula: For Inverting amplifier, the closed loop gain $A_{CL} = - R_f/R_1$

Solution: $R_f = -A_{CL} R_1$ => – (–10) x 30 KΩ => 300 KΩ

3. *An inverting amplifier has a load resistor of 50 KΩ connected to its output. If the input voltage is 0.5 V, find the load current, output voltage and input current. Given : R_1 = 20 KΩ, R_f = 200 KΩ.*

Solution:

Input current $$i = \frac{V_i}{R_1} = \frac{0.5V}{20\ K\Omega} = 0.025\ mA$$

Output Voltage $V_0 = - i R_f = - (0.025 \times 200)\ V = 5\ V$

Load current $I_L = \dfrac{V_O}{R_L} = \dfrac{5V}{50\ K\Omega} = 0.1\ mA$

4. *Find the output voltage of an OP–AMP inverting adder for the following sets of input voltages and resistors. In all cases, R_f =1 MΩ, V_1 = –3V, V_2 = + 3V, V_3 = + 2V; R_1 = 250 KΩ; R_2 = 500 KΩ; R_3 = 1 MΩ.*

Solution:

$$v_0 = - (K_1V_1 + K_2V_2 + K_3V_3)$$

$$K_1 = \frac{R_f}{R_1} = \frac{1000\ K\Omega}{250\ K\Omega} = 4;\ K_2 = \frac{1000\ K\Omega}{500\ K\Omega} = 2;\ K_3 = \frac{1\ M\Omega}{1\ M\Omega} = 1$$

$\therefore$ $V_0 = - [(4 \times - 3) + (2 \times 3) + (1 \times 2)] = 4V$

5. *In the subtractor circuit of Fig. 6.11, R_1 = 5 K, R_f = 10 K, V_I = 4 V and V_2 = 5 V. Find the value of output voltage.*

Solution:

$$v_0 = \left(1 + \frac{R_f}{R_1}\right) v_1 - \frac{R_f}{R_1} v_2 = \left(1 + \frac{10}{5}\right) 4 - \frac{10}{5} \times 5 = +\ 2V$$

6. *A 5 mV, 1 KHz sinusoidal signal is applied to the input of an OP–AMP integrator of Fig. 6.12(b) for which R = 100 KΩ and C = 1 μF. Find the output voltage.*

Solution:

$$\text{Scale factor} = - \frac{1}{CR} = \frac{1}{10^5 \times 10^{-6}} = - 10$$

The equation for the sinusoidal voltage is

$$v_1 = 5 \sin 2\pi ft = 5 \sin 2000\ \pi\ t$$

Obviously, it has been assumed that at t = 0, v_1 = 0

$\therefore$ $$V_0\ (t) = - 10 \int_0^t 5 \sin 2000\ \pi\ t = - 50 \left| \frac{- \cos 2000\ \pi t}{2000} \right|_0^t$$

$$= \frac{1}{40\ \pi} \left(\cos 2000\ \pi\ t - 1\right)$$

7. *The input to the differentiator circuit of Fig. 6.14 is a sinusoidal voltage of peak value 5 mV and frequency 1 KHz. Find out the output if R = 100 KΩ and C =1 μF.*

Solution:

The equation of the input voltage is

$$v_1 = 5 \sin 2\pi \times 1000t = 5 \sin 2000\ \pi t \text{ mV}$$

scale factor =

$$CR = 10^{-6} \times 10^5 = 0.1$$

$$v_o = 0.1 \frac{d}{dt}(5 \sin 2000\ \pi t) = (0.5 \times 2000\ \pi) \cos 2000\ \pi t$$

$$= 1000\ \pi \cos 2000\ \pi t \text{ mV}$$

As seen, output is a cosinusoidal voltage of frequency 1 KHz and peak value 1000 π mV.

EXERCISES

I. Descriptive Type Questions

1. Describe an OP-AMP and its important characteristics ? *(VTU Jan 2007)*
2. What is saturating characteristics of an OP-AMP ? Mention the typical value if saturating output voltage for an IC-741 OP–AMP operating at ± 12 V DC supply. *(VTU Jan 2007)*
3. Draw the non inverting voltage amplifier circuit using an Op-AMP and show that the closed loop voltage gain is given by $A_{Vf} = A_V / (1 + A_V\beta)$.
4. List the characteristics of an ideal OP–AMP. *(Sept 99, V.T.U.)*
5. Explain the application of an OP–AMP as a Voltage Follower.
6. Define the terms 'Slew Rate' and 'CMRR' of an OP–AMP.
7. With the help of circuit diagram explain the working of an integrator. Give the typical input and output waveforms.
8. Explain the working of an OP–AMP as (i) Summing Amplifier (ii) Integrator (iii) Differentiator.
9. Draw the block diagram of CRO and explain its function of each stage ?
10. Draw the circuit diagram of OP–AMP as integrator and derive an expression for output voltage. *(VTU Jan 2008)*
11. What are the ideal characteristics of OP–AMP? *(VTU Jan 2010)*
12. With a neat diagram, explain the working of an op-amp summing amplifier. *(VTU Jan 2010)*
13. Show how OP–AMP can be used as an inverting amplifier. Derive an expression for the voltage gain. *(VTU Jan 2010)*
14. Explain why closed loop configuration of OP-AMP is used in all the practical amplifier circuit and bring out the advantages of closed loop operation with negative feedback.

II. Multiple Choice Questions

1. The CMRR of an OP–AMP is.....

   (a) Greater than 1 (b) Less than 1

   (c) Equal to 1 (c) Equal to 0

2. The inverting amplifier circuit has an input resistance R_1 = 1KΩ feedback resistance R_F = 3KΩ. The output voltage is .....

   (a) 6 V (b) 12 V

   (c) 18 V (c) –12 V

3. Lissajous figures are used to measure .....difference between two sinusoidal Signals

   (a) Phase (b) Amplitude
   (c) Frequency (d) Time

4. CMRR of an Ideal OP–AMP is _____

   (a) 0 (b) 90
   (c) ∞ (d) 180

5. The gain of voltage follower is _____

   (a) Unity (b) Zero
   (c) ∞ (d) None

6. In inverting amplifier, there is _____ phase shift with input and output

   (a) 0° (b) 90°
   (c) 180° (d) 360°

7. The maximum rate at which amplifier output can change in volts per micro second (V/μS) is called _____

   (a) Over rate (b) Slew rate
   (c) Under rate (d) None

8. The OP-AMP is basically a _____ amplifier

   (a) Positive feedback (b) Differential
   (c) Common emitter (d) Common signal

9. In an inverting amplifier, R_1 = 1 KΩ, and R_f = 2 KΩ. If the input voltage is 2V, output voltage is __

   (a) –2 V (b) –0.5 V
   (c) 4V (d) – 4 V

10. The CMRR should be _____

    (a) Close to Unity (b) Much larger than Unity
    (c) Zero (d) Much smaller than Unity

11. When both inputs of OP-AMP are grounded, the voltage across the output is called _____

    (a) Output off set voltage (b) Output grounded voltage
    (c) Output bias voltage (d) Output common voltage

12. When two sine waves are applied simultaneously to the vertical and horizontal deflecting plates of a CRO produces _____

    (a) Lissajous figures (b) Differentiated signal
    (c) Deflection of the signal (d) Sawtooth signal

13. The full form of CRO is _____
    (a) Cathode Ray Oscillator (b) Cathode Ray Oscilloscope
    (c) Cathode Ray Organizer (d) None of these
14. The output of Integrator is _____
    (a) Linearly-increasing ramp output (b) Linearly-increasing square output
    (c) Integrated zigzag signal (d) None of these
15. The carbon particles coating in CRT, to remove the electrons along the side walls of the tube is called _____
    (a) Aquadag coating (b) Florescent coating
    (c) Both of these (d) None of these
16. The differential voltage between non-inverting and inverting input of an OP–AMP is always zero, and is called
    (a) The virtual ground (b) Real ground
    (c) Differentiated output (d) Zero input resistance
17. The OP–AMP comparator circuit, uses _____ as principle.
    (a) Saturable property of OP–AMP (b) Integration property of OP–AMP
    (c) Comparing property of OP–AMP (d) Feedback property of OP–AMP
18. In OP–AMP, the maximum rate of change of output voltage with time is _____
    (a) CMRR (b) Slew rate
    (c) Offset voltage (d) Offset rate
19. The value of slew rate for ordinary OP–AMP is _____
    (a) 0.7 V/μV (b) Offset voltage
    (c) 7 V/μV (d) None of these
20. Common Mode Gain (A_{CM}) of an OP-AMP is _____
    (a) Positive quantity (b) Negative quantity
    (c) Non positive quantity (d) Non-negative Quantity
21. CMRR =
    (a) $A_d / -A_{CM}$ (b) A_d / A_{CM}
    (c) A_{CM}/A_d (d) $A_{CM}/-A_d$
22. Ideal OP–AMP has _____
    (a) Zero open loop gain (b) Infinite open loop gain
    (c) Positive open loop gain (d) Negative open loop gain

23. OP–AMP need _____ for operation

    (a) One battery supply (b) Dual battery supply

    (c) Three phase supply (d) Power supply

24. Lissajous figures are used for _____

    (a) determining an unknown frequency by comparing it with a known frequency.

    (b) checking audio oscillator with a known frequency signal.

    (c) checking audio amplifiers and feedback networks for phase shift.

    (d) all the above.

25. The product of C and R in differentiator circuit is called _____

    (a) CR product of differentiator (b) Time constant of differentiator

    (c) Differentiation coefficient (d) None of These

III. Numerical Problems

1. An Inverting Amplifier has R_1 =20 Ω fill and R_f =100 KΩ. Find the Output Voltage, the Input Resistance and the Input Current for an input voltage of 1V.

   Ans: R_{in} = 20 KΩ, I_{in} = 0.05 mA

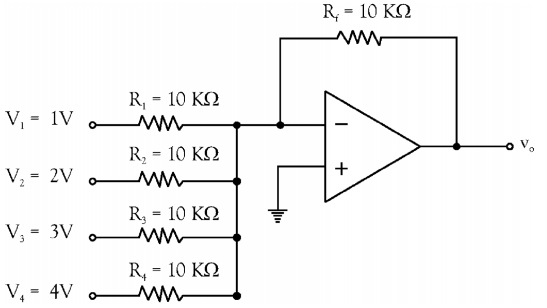
2. Design an inverting amplifier with an input resistance of 30 KΩ and a closed loop gain of -10.

   Ans: R_f = 300 KΩ

3. A non inverting amplifier has input resistance 10 KΩ and feedback resistance 60 KΩ with load resistance 47 KΩ. Draw the circuit and calculate output voltage, voltage gain and load current when input voltage is 1.5 V. *(VTU Jan 2008)*

4. An inverting amplifier circuit has input series resistor of 20 KΩ, feedback resistor of 100 KΩ and a load resistor of 50 KΩ. Draw the circuit and calculate the input current, load current, and the output voltage when the applied input voltage is equal to +1.5 volt. *(VTU July 2007)*

5. For the circuit shown in following figure, determine the output voltage.



   Ans: V_O = – 0.5 V

6. Find the output voltage of a three-input adder circuit in which $R_1 = R_2 = R_3 = 4$ KΩ and the feedback resistance $R_f = 6$ KΩ. Given $V_1 = -4$ V, $V_2 = -2$ V and $V_3 = 3$ V.

Ans : $V_O = 4.5$ V

Answers to Multiple Choice Questions

1. (a)	2. (d)	3. (a)	4. (c)	5. (a)	6. (c)	7. (b)	8. (b)	9. (d)	10. (b)	11. (a)
12 (a)	13. (b)	14. (a)	15. (a)	16. (a)	17. (a)	18. (b)	19. (d)	20. (b)	21. (a)	22. (b)
23. (b)	24. (d)	25. (b).								

UNIT 7

COMMUNICATION SYSTEMS

OBJECTIVES

Electronic communication system using radio waves has an advantage to send information in the form of voice, data or picture for longer distance at low cost. The advents in electronic communication in the form of analog communication, digital communication, microwave communication, optical communication, of audio and video signals and its impact on wire and wireless communication have changed the human lifestyle. In this Unit we will study the electronic methods of radio communication. The Unit objectives are:

(1) To study the various processes involved in communication system.

(2) To study Modulation and detailed analysis of various types of modulation.

(3) To study AM & FM Radio Systems and Superhetrodyne Receivers.

(4) To study decimal, Binary, Octal and Hexadecimal number systems.

(5) To study addition, subtraction, multiplication and division, and fractional numbers in various number systems.

(6) To study Binary Coded Decimal numbers.

7.1 INTRODUCTION

The present era is the era of 'information and communication revolution'. In electronics, the term 'communication' refers to sending, receiving and processing of information electronically. In 1840's, communication started with telegraphy. Few decades later, telephony was developed followed by radio at the beginning of twentieth century. Radio communication was made possible by the invention of the electronic valves. It subsequently became even more widely used and refined through the invention and use of the transistors, integrated circuits and other semiconductor devices.

More recently, the use of satellites and fiber optics has made communications even more widespread, with an increasing emphasis on computer and other data communications. Radar, telemetry and satellite links play vital role in navigation, defence, scientific research etc. For communication purposes, only a part of the electromagnetic waves like radio waves and microwaves are being used.

7.2 BLOCK DIAGRAM OF COMMUNICATION SYSTEM

The model of a communication system is shown in Fig. 7.1, which involves some basic signal processing operation in the transmission of information, irrespective of the mode and nature of transmission. In the process of communication, several equipments are to be used in an integrated and sequential manner. This set up as a whole is called the *communication system.*

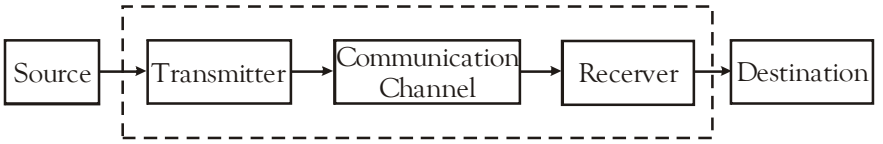


Figure 7.1 *Model of a communication system*

In a communication system, the Source provides input signal which is an electrical signal containing required input information to be transmitted. The information in any form can be converted into electrical signal using a transducer. This electrical signal is further processed for long range transmission and transmitted using a transmission system. The transmitted signal propagates towards destination through physical wire or, wireless free space or optical fiber. At destination, the signal is received by means of a receiver and processed and then converted back into required output information by means of another transducer.

The communication system has three main components: *Transmitter, Communication Channel* and *Receiver.*

- **Transmitter:** It processes the input signal in a form suitable for transmission over the *communication channel* - wire or wireless media or optical fiber. This operation is called *modulation* and it is a process designed to match the properties of the signal to be transmitted to that of the channel - through the use of carrier wave. It is the systematic variation of some attributes of the carrier wave such as the amplitude, the phase or the frequency in accordance with a function of the input signal.
- **Communication channel:** It provides physical connection between the transmitter and the receiver. The channels are generally of two types: *point to point channels* (Ex. Telephone wires, Cables, Microwave links, etc.) and *broadcast channels* (Ex. Satellite in geostationary orbit wherein many receiving stations can get the information from the satellite, free space for electro-magnetic signal).
- **Receiver:** It receives and processes the signal and produces an *estimate* of the original message signal. This operation is called *demodulation.* The word *estimate* is used, as the receiver cannot recover the signals perfectly. In addition to the demodulation, the receiver also performs amplification and filtering.

Based on the type of modulation scheme and the nature of output of the information source, communication systems may be categorized as:

- **Analog communication systems-** designed to transmit analog signals using analog modulation methods.

- **Digital communication systems-**designed to transmit digital information using digital modulation schemes and
- **Hybrid systems-** use sampled and quantized values of an analog message signal for digital modulation schemes for transmitting.

Frequency bandwidth: It is generally defined as the range of frequencies that could be transmitted free of distortion over a channel. For example, the telephone line has a Bandwidth (BW) of 3 KHz. Due to this limitation, the signal with high frequency components may suffer *amplitude* and *phase distortion* as it travels over the channel. In addition, unpredictable electrical signals, referred to as noise, also corrupts the signal.

Channel capacity, C: It is the maximum rate at which nearly errorless data transmission is theoretically possible. If the parameters of the channel are known, C may be computed. The channel capacity (C) with bandwidth (B) and, Signal to Noise Ratio, *(S/N)* is given by $C = [B \log_2 (1 + S/N)]$ bits/sec.

7.3 MODULATION

It is a process of converting certain parameters (like, amplitude, frequency, or phase) of high frequency radio signal according to the instantaneous value of low frequency information (such as audio) signal.

7.3.1 Need for Modulation

The information/intelligence such as human voice /audio signals cannot be transmitted over long distances due to the enormous amount of power required for transmission purposes and the requirement of large size of antenna. For example, for transmission at 15 KHz, height of the transmitting and receiving antenna is about 5000 meter, which is almost impossible due to construction constraints and huge power requirement. Hence, it is customary to modulate the information signal by another high frequency waveform called the carrier signal (radio wave) and transmit the resulting signal. At the receiving end, the information signal is separated from the carrier signal (Demodulation). Further, the advantage of modulation is the possibility of transmission of various frequencies on the same channel.

7.4 MODULATION METHODS

The process of converting certain parameters (like, amplitude, frequency, or phase) of high frequency radio signal according to the instantaneous value of low frequency information (such as audio signal) is called modulation. This occurs at transmitter stage. After receiving the modulated signal at receiver, the original information signal has to be recovered back and this process is called de-modulation.

In analog modulation process, the amplitude, or frequency, or phase of a high frequency signal called carrier signal is varied according to the instantaneous value of information signal (message) called modulating signal. Accordingly there are three types of modulation methods as Amplitude modulation, Frequency modulation and Phase modulation. Frequency modulation and Phase modulation are combindly called as Angle modulation.

7.4.1 Amplitude Modulation

Definition of AM

Amplitude Modulation (AM) is defined as the process of varying the maximum amplitude of a sinusoidal **carrier signal** according to the instantaneous value of **modulating signal** by keeping both frequency and phase of the carrier signal constant.

Graphical Representation:

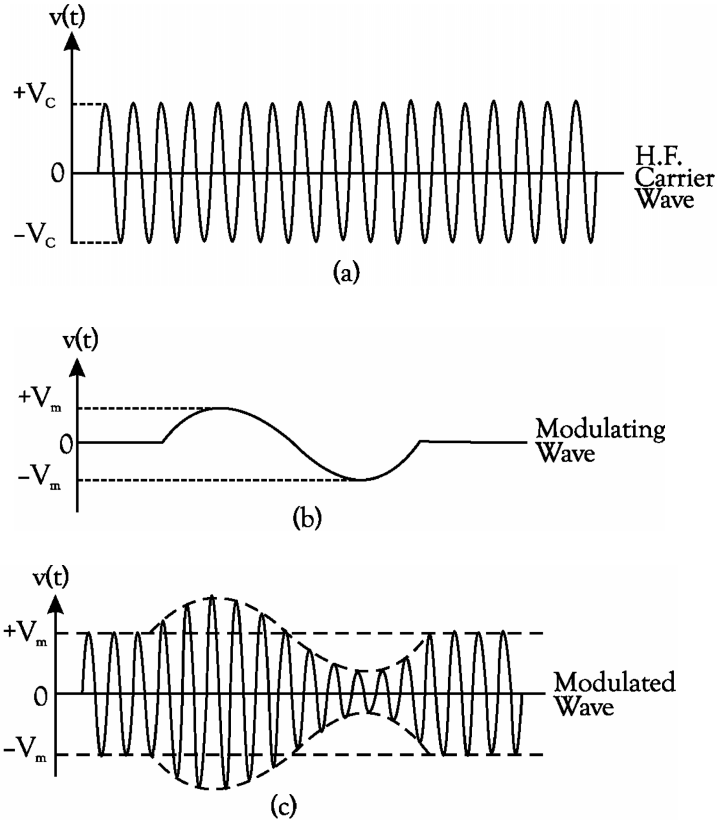


Figure 7.2 *Graphical representation of (a) Carrier signal, (b) Modulating signal, and (c) Amplitude modulated signal*

Expression for AM Signal

Consider a carrier signal with V_C as maximum amplitude and f_C as carrier frequency. Then the instantaneous voltage value of sinusoidal carrier wave $v_c(t)$ is defined by :

$$v_c(t) = V_c \sin 2\pi f_c t = V_c \sin \omega_c t \quad ...(7.1)$$

The instantaneous voltage value of modulating signal is:

$$v_m(t) = V_m \sin 2\pi f_m t = V_m \sin \omega_m t \quad ...(7.2)$$

After modulation, the maximum amplitude of carrier signal varies according to instantaneous voltage value of modulating signal. Then using Eqn. (7.1), the instantaneous value of modulated signal (v(t)) can be written as:

$$v(t) = [V_c + k_a v_m(t)] \sin \omega_c t$$

or

$$v(t) = [V_c + k_a V_m \sin \omega_m t] \sin \omega_c t \quad ...(7.3)$$

$$v(t) = V_c [\sin \omega_c t + (k_a V_m / V_c) \sin \omega_m t \,.\, \sin \omega_c t$$

$$v(t) = V_c [\sin \omega_c t + m_a \sin \omega_m t. \sin \omega_c t] \quad ...(7.4)$$

where, $m_a = k_a V_m / V_c$ = modulation index of AM signal and v(t) is instantaneous voltage value of modulated signal. k_a is called amplitude sensitivity and its value usually 1.

Hence modulation index of AM signal is defined as the ratio between peak value of modulating signal (V_m) to peak value of carrier signal (V_c).

$$m_a = V_m / V_c \quad ...(7.5)$$

Using Eqns. (7.5), Eqn. (7.4) can be written as

$$v(t) = V_c \sin \omega_C t + \frac{v_c m_a}{2} \left[2 \sin \omega_c t. \sin \omega_m t\right]$$

Using Trigonometric relation

$$\sin A \sin B = \frac{1}{2}\{\cos(A-B) - \cos(A+B)$$

$$v(t) = V_c \sin \omega_C t + \frac{V_c m_a}{2} \left[\cos(\omega_c - \omega_m)t - \cos(\omega_c + \omega_m)t\right]$$

Since, using Trigonometric relation

$$\sin A \sin B = \frac{1}{2}\{\cos(A - B) - \cos(A + B)$$

or

$$v(t) \underbrace{= V_c \sin \omega_c t}_{\text{Unmodulated carrier}} + \underbrace{\frac{V_c m_a}{2} \cos(\omega_c - \omega_m)t}_{\text{Lower Sideband}} - \underbrace{\frac{V_c m_a}{2} \cos(\omega_c + \omega_m)t]}_{\text{Upper Sideband}} \quad ...(7.6)$$

Since $\omega = 2\pi f$, the amplitude modulated signal described in Eqn. (7.6) contains three high frequency components and are shown in Fig. 7.3. They are:

(i) **Carrier Frequency Component** (C) with amplitude V_c and frequency f_c.

(ii) **Lower Side Band frequency component (LBS)** with amplitude $V_c m_a/2$ and frequency $(f_c - f_m)$

(iii) **Upper Side Band frequency component (USB)** with amplitude $V_c m_a/2$ and frequency $(f_c + f_m)$

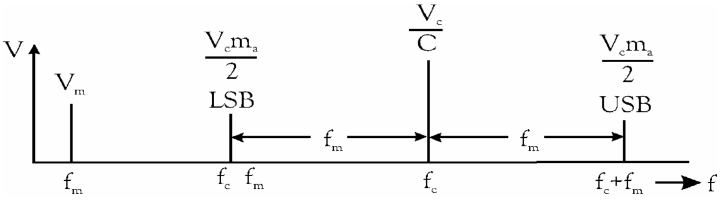


Figure 7.3 *Frequency spectrum of AM signal*

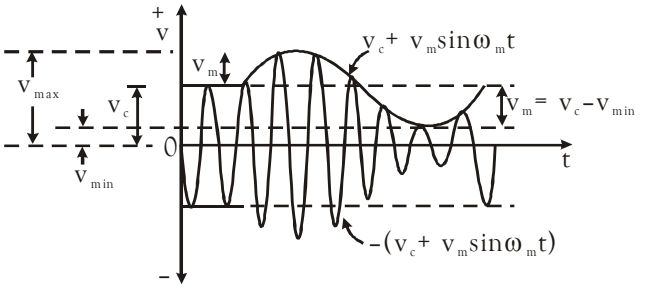


Figure 7.4 *A.M. signal*

Expression for Modulation Index

We know that $m_a = V_m/V_c$ ...(7.7)

Using the above Fig. 7.4, we can write $m_a = [(V_{max} - V_c) / V_c] = [(V_c - V_{min}) / V_c]$

or $V_C = (V_{max} + V_{min}) / 2$ ...(7.8)

also from the figure, we can write $2V_m = V_{max} - V_{min}$

or $V_m = (V_{max} - V_{min}) / 2$ ...(7.9)

Using Eqn. (7.8) and (7.9), in Eqn. (7.7), we get,

$$m_a = \frac{V_m}{V_c} = \frac{(V_{max} - V_{min})/2}{(V_{max} + V_{min})/2} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \quad ...(7.10)$$

Based on numerical value of m_a the following 3 cases arises and are shown in Fig. 7.5:

1. If $m_a > 1$, then the modulated signal is called **over modulated**.
2. If $m_a < 1$, then the modulated signal is called **under modulated**
3. If $m_a = 1$, then the modulated signal is called **100% or critically modulated**.

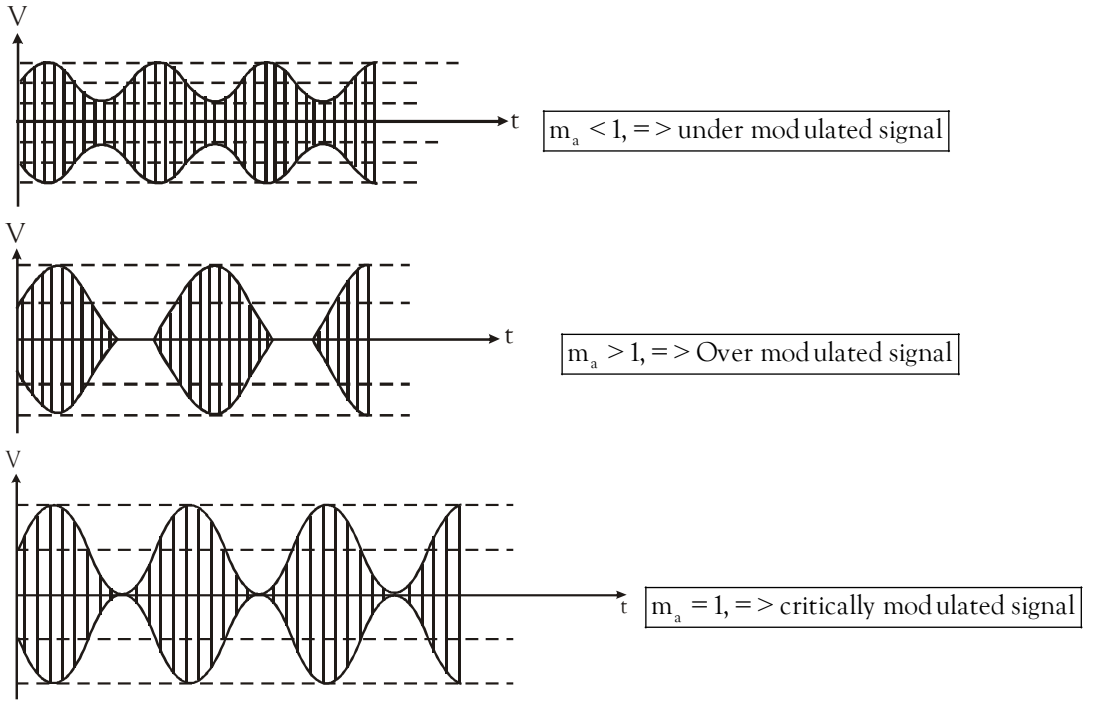


Figure 7.5 *AM signal for different modulation index*

Power in AM signal

The AM signal has 3 power components: $P_{Carrier}$, P_{USB} and P_{LSB}. where, $P_{LSB} = P_{USB}$. The LSB and USB power components depend on the modulation depth. Thus, the total power radiated is given by $P_t = P_{Carrier} + P_{LSB} + P_{USB}$

Now, $$P_t = \frac{V_{carr}^2}{R} + \frac{V_{LSB}^2}{R} + \frac{V_{USB}^2}{R} \quad .....(i) \qquad \left[\because power = \frac{V^2}{R}\right]$$

and R is the load resistance of the Antenna.

Power in the carrier signal,

$$P_c = \frac{V_{carr}^2}{R} = \frac{\left(V_c/\sqrt{2}\right)^2}{R} = \frac{V_c^2}{2R} \quad .....(ii)$$

we know that $m_a = \frac{V_m}{V_c}$ and $V_{LSB(max)} = \frac{V_m}{2}$

$\therefore$ $$V_{LSB} = \frac{V_{LSB(max)}}{\sqrt{2}} = \frac{\left(m_a V_c/2\right)}{\sqrt{2}}$$

Also, $$V_{USB} = \frac{(m_a V_c/2)}{\sqrt{2}}$$

Power in the side band,

$$P_{LSB} = P_{USB} = \frac{\left[\left\{\frac{m_a V_c}{2}/\sqrt{2}\right\}\right]^2}{R} = \frac{m^2 V_c^2}{8R} \quad \text{.....(iii)}$$

Substituting the values of P_C, P_{LSB} and P_{USB} in eqn (i), we get,

$$P_t = \frac{V_c^2}{2R} + \frac{m_a{}^2 V_c^2}{8R} + \frac{m_a{}^2 V_c^2}{8R} \quad \text{.....(iv)}$$

or $$P_t = \frac{V_c^2}{2R} + \frac{m_a{}^2 V_c^2}{4R}$$

or $$P_t = \frac{V_c^2}{2R}\left[1 + \frac{m_a{}^2}{2}\right]$$

The average power delivered, P_t, to a load resistor R of the antenna, is given by:

$$P_t = P_c\left[1 + \frac{m_a{}^2}{2}\right] \quad \text{...(7.11)}$$

when m_a = 1, the maximum power in the amplitude-modulated wave is,

$$P_t = P_c\left[1 + \frac{1}{2}\right] = 1.5\, P_c \quad \text{...(7.12)}$$

Hence, the total power of modulated signal is 1.5 times (or 150 %) that of carrier signal power for 100% modulation. Hence, it may be noted that AM is not very efficient due to the fact that most of the power is in the carrier itself.

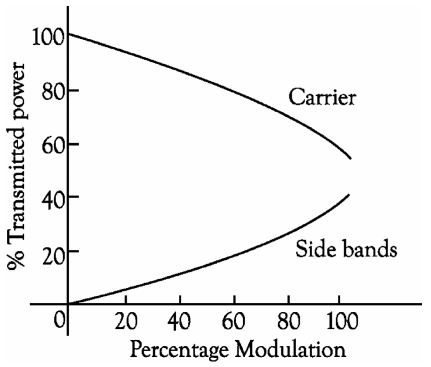


Figure 7.6 *Power in AM signal*

7.4.2 Frequency Modulation

Definition of FM Signal

Frequency modulation (FM) is defined as a process of varying the frequency of carrier signal according to the instantaneous voltage value of modulating signal by keeping both amplitude and phase of the carrier signal constant.

Graphical Representation:

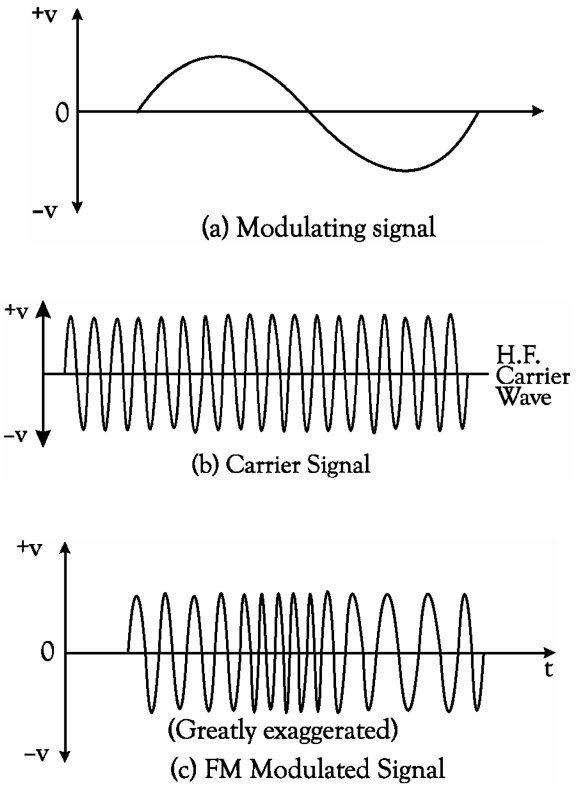


Figure 7.7 *Graphical representation of FM*

Expression for FM Signal:

The general representation for a carrier signal is given by:

$$v_c(t) = V_c \sin(\omega_c t + \varphi) \quad \text{...(7.13)}$$

and the expression for modulating signal is given by:

$$v_m(t) = V_m \cos \omega_m t \quad ...(7.14)$$

In FM, the instantaneous angular frequency ω of the frequency modulated signal changes according to instantaneous amplitude of modulating signal and is given by

$$\omega = \omega_c [1 + k_f V_m(t)] \quad ...(7.15)$$

$$= \omega_c [1 + k_f V_m \cos \omega_m t]$$

or $$2\pi f = 2\pi f_c [1 + k_f V_m \cos \omega_m t]$$

$$f = f_c [1 + k_f V_m \cos \omega_m t]$$

or $$f = [f_c + f_c k_f V_m \cos \omega_m t] \quad ...(7.16)$$

Maximum deviation in frequency occurs when $\cos \omega_m t = 1$. Hence at maximum frequency deviation (or depth of modulation) of FM signal = $\delta = f_c k_f V_m$. ...(7.17)

The instantaneous amplitude of the FM signal is given by the expression :

$$v(t) = V_c \sin \theta \quad ...(7.18)$$

To determine θ, it is necessary to integrate ω with respect to time. Thus,

$$\theta = \int \omega dt = \int \omega_c \left(1 + k_f V_m \cos \omega_m t\right) dt \quad ...(7.19)$$

$$= \omega_c \int \left(1 + k_f V_m \cos \omega_m t\right) dt$$

$$= \omega_c \left[t + \frac{k_f V_m \sin \omega_m t}{\omega_m} \right]$$

$$= \omega_c t + \frac{k_f V_m \omega_c \sin \omega_m t}{\omega_m} \quad ...(7.20)$$

$$= \omega_c t + \frac{k_f V_m f_c \sin \omega_m t}{f_m} \quad ...(7.21)$$

Substituting the value of δ eqn. (7.17) in eqn. (7.20) and (7.21) above, we have

$$\theta = \omega_c t + \frac{\delta}{f_m} \sin \omega_m t \quad ...(7.22)$$

Substituting the above value of θ in equation (7.18) we have

$$v(t) = V_c \sin \left[\omega_c t + \frac{\delta}{f_m} \sin \omega_m t \right] \quad ...(7.23)$$

Eqn. (7.23) gives the expression for instantaneous voltage for F.M. signal.

Modulation Index

The modulation index of the frequency modulated wave is defined as the ratio of the maximum frequency deviation to the modulating frequency, measured in radians.

$$m_f = \frac{Maximum\ frequency\ deviation}{Modulating\ frequency} = \frac{\delta}{f_m} \qquad ...(7.24)$$

Substituting the above in Eqn. (7.23), we have

$$v(t) = V_c \sin (\omega_c t + m_f \sin \omega_m t) \qquad ...(7.25)$$

It may be noted that for a given frequency deviation (δ) the modulation index varies inversely with the modulating frequency, but the amplitude of the modulated signal remains constant.

Frequency Spectrum of the FM Signal:

The expression for Frequency-Modulated signal as shown in Eqn. (7.25) contains the sine of' a sine term. Hence, to obtain the frequencies in a FM wave it becomes imperative to use *Bessel functions.* Using Bessel functions we can expand Eqn. (7.25) as follows:

$$\begin{aligned} v(t) = V_c [&J_0 (m_f) \sin \omega_c t] \\ &+ J_1 (m_f) \{\sin (\omega_c + \omega_m)t - \sin (\omega_c - \omega_m)t\} \\ &+ J_2 (m_f) \{\sin (\omega_c + 2\omega_m)t + \sin (\omega_c - 2\omega_m)t\} \\ &+ J_3 (m_f) \{\sin (\omega_c + 3\omega_m)t - \sin (\omega_c - 3\omega_m)t\} \\ &+ J_4 (m_f) \{\sin (\omega_c + 4\omega_m)t + \sin (\omega_c - 4\omega_m)t\} \ldots\ldots\ldots\ldots\ldots\ldots] \end{aligned} \qquad ...(7.26)$$

where J_0, J_1, J_2 ..... are the coefficients of zero order, first order, second order, ... of the *Bessel function,* and m_f is the argument.

Eqn. (7.26) shows that the frequency spectrum of FM contains infinite frequency terms of variable amplitude as shown in Fig. 7.8.

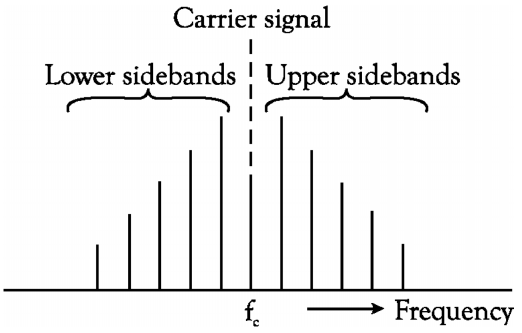


Figure 7.8 *FM spectrum*

Bandwidth

There are infinite number of side bands in the frequency spectrum of an FM wave. Hence in ideal case, the bandwidth of FM is infinity. But in practice the bandwidth of an FM wave is obtained by employing *Carsen's Rule,* which is as follows:

Band width of FM = 2 ($\delta + f_m$) ...(7.27)

where δ = frequency deviation

f_m = modulating signal frequency

Power in FM Signal:

Since the amplitude of an FM wave is not affected by modulation, the total power remains the same. If P_C is the average power of the carrier signal, the total average power in the frequency modulated wave is given by the relation

$$P_t = P_c \left[J_0^2 + 2\left(J_1^2 + J_2^2 + J_3^2 + ... \right) \right] \quad ...(7.28)$$

7.4.3 Phase Modulation

Definition of PM

Phase modulation(PM) is defined as the process of varying the phase angle of carrier signal according to the instantaneous amplitude of modulating signal by keeping both amplitude and frequency of the carrier signal constant.

Expression for Phase Modulated Signal

The expression for a PM wave is

$$v(t) = A \sin\left(\omega_c t + \phi_m \sin \omega_m t \right) \quad ...(7.29)$$

where φ_m is the maximum value of phase change due to this modulating signal and is proportional to the maximum amplitude of modulating signal.

$$v(t) = A \sin\left(\omega_c t + m_p \sin \omega_m t \right) \quad ...(7.30)$$

where $m_p = \varphi_m$ = modulation index for phase modulation. Comparison of the above Eqn. (7.30) and Eqn. (7.25) shows them to be identical, except for the different definitions of the modulation index. Thus, it is apparent that Frequency Modulation and Phase Modulation are similar to each other.

7.4.4 Comparison between AM & FM

S.No.	A.M. Method	F.M. Method
1	In AM method, the amplitude of carrier signal is varied according to the instantaneous amplitude of modulating signal.	In FM method, the frequency of carrier signal is varied according to the instantaneous amplitude of modulating signal.
2	In AM, the amplitude of modulated signal depends on the value of modulation index.	In FM, the amplitude of modulated signal is independent on modulation index.
3	In AM, only USB and LSB contain information and most of the transmitted power is carrier power which does not contain any information.	In FM, all the transmitted power is useful.
4	AM signals are prone to noise while travelling from transmitter to receiver. Hence AM signal has low signal to noise ratio.	In FM, since information is in frequency modulated form, any noise added to amplitude will not affect the quality. Hence FM signal has high signal to noise ratio.
5	AM signal has two sidebands, one on both sides of carrier frequency.	FM has infinite sidebands on both sides of carrier frequency.
6	In AM, noise can not be controlled by varying modulation index.	In FM, noise can be further reduced by increasing deviation.
7	Band width of AM is narrow.	Band width of FM is 7 to 15 times larger than AM.
8	AM transmitting and receiving equipments are simple and less expensive.	FM transmitting and receiving equipments are complex and expensive.

7.5. RADIO SYSTEMS

A radio system consists of a transmitter, free space, and one or more receivers to communicate the information to distant places. Depending on the modulation technique used, a radio system can be classified as AM radio system or FM radio system. An AM radio system consists of an AM transmitter and one or more AM receivers. A FM radio system consists of a FM transmitter and one or more FM receivers. A radio transmitter transmits modulated carrier signal. This modulated carrier signal propagates in free space in the form of electromagnetic signal with velocity 3×10^8 m/sec. The radio receiver receives these signals using its receiving antenna and separates the modulating signal from modulated carrier signal. Then the modulating signal is amplified and converted back in to sound by means a loud speaker.

7.5.1 AM Transmitter

AM transmitter is used to transmit amplitude modulated signal in radio communication system. Such transmitters are used for radio broadcasting, radio telephony, radio telegraphy, television picture broadcasting etc. The block diagram of a commonly used AM transmitter is shown in Fig. 7.9.

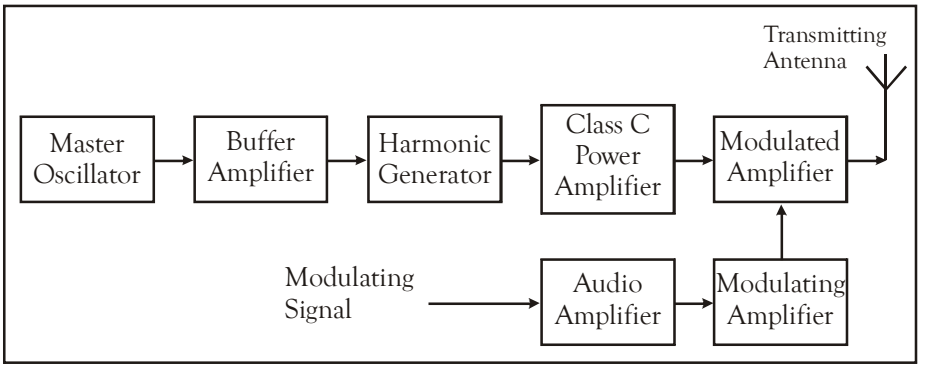


Figure 7.9 *Block diagram of A.M. transmitter*

The function of each stage is briefly explained below:

(1) **Master Oscillator:** It generates oscillations of desired constant frequency. The generated frequency is required to remain constant within close limits in spite of variations in the supply voltage, ambient temperature, temperature of components of load. Further frequency variations with time and with age of the transistor are to be avoided.

(2) **Buffer Amplifier:** If the master oscillator directly drives a harmonic generator or class C power amplifier, which may draw input current (base current in *CE* amplifier), then power is drawn from the master oscillator. This results in loading of master oscillator which in turn causes variation of effective resistance of the tank circuit of the oscillator and hence results in frequency variation. Accordingly, a buffer amplifier or isolating amplifier is placed between the master oscillator and the harmonic generators. This buffer amplifier does not draw any input current and hence causes no loading of the master oscillator. Changes in carrier frequency due to variations in loading are thus avoided.

(3) **Harmonic Generator:** Usually master oscillator generates voltage at a frequency which is a sub-multiple of the carrier frequency *i.e.* the frequency of the radiated power. Basically these harmonic generators are class C tunned amplifiers in which the output R.F. voltage is first distorted through class C operation and then the tuned circuit in the output circuit of amplifier selects the desired harmonic frequency.

(4) **Class C Amplifier:** R.F. voltage generated by the master oscillator has usually very small power, of the order of a few watts. The power level is required to be raised to the final high value in a chain of class C amplifiers having high output circuit efficiency of the order of 70%. In general, first few stages of class C amplifier act as harmonic generators as well.

(5) **Modulated Amplifier:** This is a class C tuned amplifier usually of push-pull type and output is modulated by audio modulating voltage from modulating amplifier. High efficiency series collector modulation is most popularly used in high power radio broadcast and radio telephone transmitters. Base bias modulation is sometimes used particularly for modulation at low power levels.

(6) **Modulating Amplifier:** This is usually a class B push-pull amplifier and feeds audio power into the modulated amplifier. Class B operation is generally used because of high collector circuit efficiency. However, class A modulating amplifiers are also sometimes used particularly in low power transmitters.

(7) **Transmitting Antenna:** It radiates the radio frequency AM signal fed to it as electromagnetic (EM) signal and the EM signal propagates around the antenna at a velocity of light.

7.5.2 FM Transmitter

FM transmitter is used to transmit frequency modulated signal in radio communication system. Such transmitters are used for FM radio broadcasting, television voice broadcasting etc. The block diagram of a commonly used FM transmitter of transmitting frequency 96 MHz, is shown in Fig. 7.10.

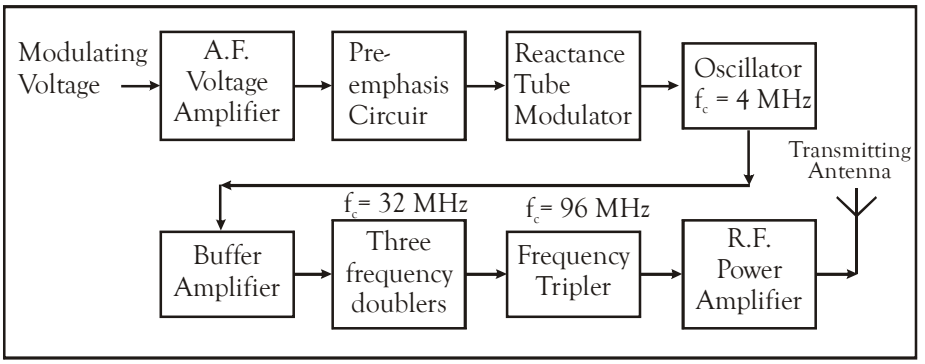


Figure 7.10 *Block diagram of F.M. transmitter*

The function of each stage is briefly explained below :

(1) **Modulating Voltage:** The electrical version of sound is obtained by means of a microphone called modulating voltage.

(2) **A.F. Voltage Amplifier:** The modulating voltage is amplified by means one or two stages of Audio Frequency voltage Amplifier.

(3) **Pre-emphasis Circuit:** During the modulating signals voltage amplification, low frequency part of modulating signal amplifies significantly and high frequency components of modulating signal amplifies less. To improve the amplitude of high frequency components of modulating signal before Frequency modulation, using reactance FET modulator, pre-emphasis circuit is used.

(4) **Reactance Tube Modulator:** This circuit changes the reactance of its output according to the instantaneous amplitude value of modulating signal and this change in reactance is applied across tuned circuit of next stage, i.e., Oscillator.

(5) **Local Oscillator:** The output signal frequency of local oscillator changes according to change in reactance of Oscillator, which in turn changes according to change in voltage value of modulating

signal. Hence output of the oscillator is FM signal. Let the design of local oscillator circuit is such that centre frequency of FM signal is 4 MHz.

(6) **Buffer Amplifier:** Buffer amplifier connects the FM signal from Local Oscillator to Frequency doublers stage by providing required impedance matching.

(7) **Frequency Doublers:** This circuit doubles the input frequency so that the output frequency will become double of input frequency. Three frequency doublers are used in a typical FM transmitter. The final frequency becomes 32 MHz.

(8) **Frequency Tripler:** This is a class C amplifier and acts like a frequency tripler. The output frequency of FM signal becomes 96 MHz.

(9) **R.F. Power Amplifier:** This stage increases the power of FM signal to required level to transmit it using a transmitting antenna.

(10) **Transmitting Antenna:** It radiates the radio frequency FM signal fed to it as Electromagnetic signal and the EM signal propagates around the antenna at a velocity of light.

7.6 SUPERHETRODYNE RECEIVERS

7.6.1 Principle of Superhetrodyning

Heterodyne means mixing. Heterodyne reception stands for the radio reception after converting the modulated carrier voltage into similarly modulated voltage at a different carrier frequency. Thus, the heterodyning process involves a simple change or translation of carrier frequency. This change in carrier frequency is achieved by heterodyning or mixing the modulated carrier voltage with a locally generated high frequency voltage in a non-linear device. This gives rise to a modulated carrier voltage at the difference carrier frequency, called the *intermediate frequency.*

Superheterodyne reception is a form of heterodyne reception in which frequency conversion takes place one or more times before the modulated carrier voltage is fed to the detector to recover the original modulation frequency voltage. In practice, however, the name super-heterodyne is used to those receivers in which only one frequency conversion takes place before detection. The receiver in which frequency conversion takes place twice before detection is called a *double super-heterodyne receiver.*

In a simple super-heterodyne receiver, the modulated carrier voltage of frequency f_C is fed to a nonlinear device called the frequency mixer (or simply mixer) to which is also fed the voltage of frequency f_O generated in a local oscillator and at the output we get voltages of sum and difference frequencies ($mf_C \pm nf_O$) where m and n are integers. A tuned circuit in the output of the mixer stage tuned to the difference frequency ($f_C - f_O$) picks up this difference frequency component called the intermediate frequency f_i (abbreviated as I.F.). This I.F. voltage is modulated exactly similar to the incoming modulated carrier voltage. This results only a translation or change in the carrier frequency from f_C to f_i. This intermediate frequency f_i is fixed for a receiver.

The constant intermediate frequency f_i is maintained between the local oscillator frequency and the RF signal frequency, usually through use of capacitance tuning wherein the capacitors in the R.F. tuned circuits and local oscillator are ganged together and operated in unison through use of a single control knob.

The IF amplifier, in practice, is a two or three stage tuned amplifier, tuned to the intermediate frequency and it provides most of the gain and hence the sensitivity of the receiver. It also fixes the 3-dB bandwidth (typically 10 KHz) of the receiver. The IF amplifier, being fixed frequency amplifier, has fairly uniform selectivity and sensitivity and hence, the entire super-heterodyne receiver has almost constant selectivity and sensitivity throughout the carrier frequency band.

7.6.2 AM Superhetrodyne Receiver

A.M. receiver is an electronic circuit used to receive AM signals from free space and separates the modulating signal (intelligence) from it to reproduce original intelligence using a loudspeaker. The block diagram of a super-heterodyne receiver is shown in Fig. 7.11.

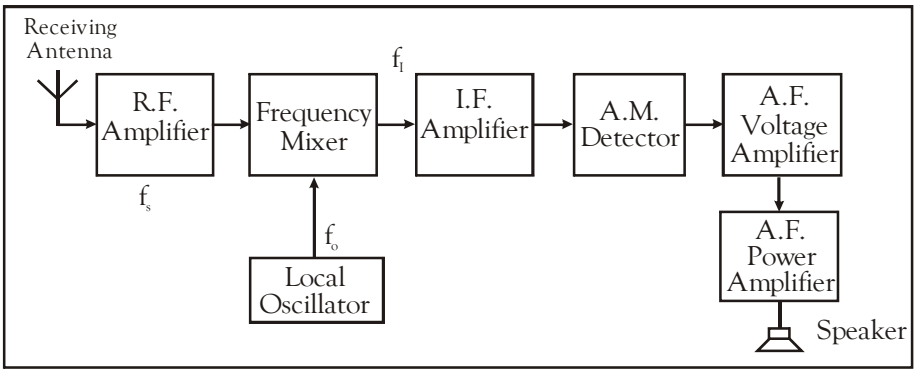


Figure 7.11 *Block diagram of A.M. superheterodyne receiver*

The functions of different stages of AM superheterodyne receiver is explained below:

(1) **Antenna:** It intercepts the electromagnetic waves. Voltages induced in the antenna are communicated to the receiver input circuit by means of a feeder wire. A parallel tuned circuit at the input of the receiver responds only to voltage at the desired carrier frequency and rejects voltages at all other frequencies. The voltage so picked up is fed to the input of the RF amplifier stage.

(2) **R.F. Amplifier:** This stage is generally a tuned voltage (small-signal) amplifier tuned to the desired carrier frequency. The chief functions of RF amplifier stage are:

(i) To amplify the input signal voltage to a suitably high level before feeding it to the frequency mixer, which contributes large noise. Thus signal/noise ratio is improved.

(ii) To provide discrimination or selectivity against image frequency signal (noise) and intermediate frequency signal (f_i).

(3) **Frequency Mixer:** This consists of a local oscillator and frequency mixer. Both the local oscillator voltage, as well as signal voltage is fed to the Frequency Mixer. The mixer, being a non-linear device, produces at its output the various intermodulation terms. The difference frequency voltage from intermodulation terms is picked up by the tuned circuit of the mixer. This difference frequency

is called the intermediate frequency, the value of which is constant for a receiver. In general, for all FM receivers, typical value of intermediate frequency is 465 KHz or 456 KHz. Sometimes, two separate transistors are used as local oscillator and frequency mixer but more often only one transistor functions both as local oscillator and frequency mixer. Such a transistor is then referred to as a frequency converter transistor. Thus with the help of frequency converter stage, RF signal of any carrier frequency is converted into similarly modulated fixed frequency IF signal.

(4) **I.F. Amplifier:** It consists of two or more stages of fixed frequency voltage amplifier having a 3-dB bandwidth of 10 KHz for AM broadcast. IF amplifier provides most of the receiver amplification and selectivity of the signal.

(5) **A.M. Detector:** Output of the last IF amplifier stage is fed to detector stage which is generally a linear diode detector. Output of this detector is the original modulating frequency voltage. For satisfactory operation of this detector, *i.e.* for linear detection, it is necessary that the carrier voltage fed to it be at least 1 volt. Hence the preceding amplifier stages must be designed to provide enough gain so as to feed a carrier of at least one volt to the detector for the weakest signal desired to be received by the receiver.

(6) **A.F. Voltage Amplifier:** Audio frequency output from A.M. detector is fed to the audio frequency amplifier which provides additional amplification. Usually one stage of audio voltage amplifier is used.

(7) **A.F. Power Amplifier:** The audio voltage amplifier is followed by one or more stages of audio power amplifier.

(8) **Loudspeaker:** Amplified audio output voltage of audio power amplifier is fed to loudspeaker through impedance matching transformer. The loudspeaker reproduces the original voice/program at the output.

7.6.3 FM Superheterodyne Receiver

F.M. receiver is an electronic circuit used to receive FM signals from free space and separate the modulating signal (intelligence) by means of de-modulator circuit and reproduce the original information using a loudspeaker. The block diagram of a super-heterodyne receiver is shown in Fig. 7.12.

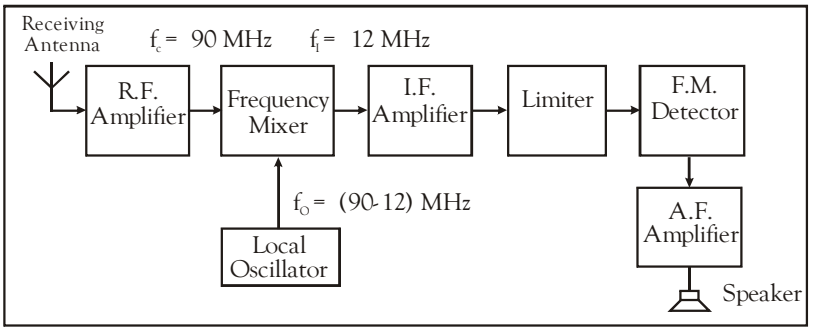


Figure 7.12 *Block diagram of F.M. superheterodyne receiver*

(1) **Antenna:** It intercepts the electromagnetic waves. Voltages induced in the antenna are

communicated to the receiver input circuit by means of a feeder wire. A parallel tuned circuit at the input of the receiver responds only to voltage at the desired carrier frequency and rejects voltages at all other frequencies. The voltage so picked up is fed to the input of the RF amplifier stage.

(2) **R.F. Amplifier or Signal Frequency Amplifier:** It serves the same function as in amplitude modulation super-heterodyne receiver. Thus it is used *(a)* to raise the signal level appreciably before the signal is fed to the mixer and *(b)* to discriminate against the image signal. But in F.M. broadcast, the signal bandwidth is large being 150 KHz as against 10 KHz in A.M. broadcast. Hence the R.F. amplifier must be designed to handle this large bandwidth.

(3) **Frequency Mixer:** It performs the usual function of mixing or heterodyning the signal frequency voltage and the local oscillator voltage to produce the difference frequency signal which is the intermediate frequency voltage. Since F.M. broadcast takes place either in the VHF band or UHF band, single transistor frequency convertor is not used. A separate local oscillator is always used and another transistor serves as the frequency mixer. The intermediate frequency used in F.M. receivers is higher than that in A.M. receivers operating at short waves. Typical value of intermediate frequency is 12 MHz. This high intermediate frequency helps in image rejection.

(4) **Local Oscillator:** A separate local oscillator is always used. At ultra high frequencies, it is preferred to keep the local oscillator frequency smaller than the signal frequency by an amount equal to the intermediate frequency (I.F).

(5) **I.F. Amplifier:** A multistage I.F. amplifier is used to provide large gain. Further this I.F. amplifier should be designed to have high overall bandwidth of the order of 150 KHz. Since the overall bandwidth of amplifier decreases as the number of stages in cascade increases, it is necessary to design individual stages to have correspondingly higher bandwidth than the overall bandwidth desired.

(6) **Limiter:** The I.F. amplifier is followed by a limiter which limits the I.F. voltage to a predetermined level and thus removes all amplitude variations which may be incidentally caused due to changes in the transmission path or by man made static or natural static noise.

(7) **F.M. Detector:** This extracts the original modulating signal from the frequency modulated carrier signal. A discriminator is used as the F.M. detector.

(8) **Audio Amplifier:** The output of the F.M. detector is fed to an audio frequency small signal amplifier and one or more audio frequency large-signal amplifiers. The output audio voltage is then fed to the loudspeaker. In F.M. broadcast, the maximum modulating frequency permitted is 15 KHz and hence the audio frequency must be designed to accommodate such large bandwidth. Similarly the loudspeaker must be capable of reproducing all high frequency tones upto 15 KHz. Often two or more loudspeakers are used, each reproducing a limited range of frequencies.

(9) **Loudspeaker:** Amplified audio output voltage of audio power amplifier is fed to loudspeaker through impedance matching transformer. The loudspeaker reproduces the original voice/program at the output.

SOLVED PROBLEMS

1. *A 10 MHz sinusoidal carrier signal of amplitude 10 mV is amplitude modulated by a 5 KHz sinusoidal audio signal of amplitude 6 mV. Find the frequency component of the resultant modulated wave and their amplitudes?*

Ans: Given : f_C = 10 MHz, f_m = 5 KHz = 0.005 MHz.

(i) f_C = 10 MHz

(ii) LSB frequency = $(f_c - f_m)$ = (10 – 0.005) MHz = 9.995 MHz.

(iii) USB frequency = $(f_c + f_m)$ = (10 + 0.005) MHz = 10.005 MHz

(iv) Modulation index $(m_a) = V_m/V_c = 6/10 = 0.6$

(v) Percentage of modulation = m_a x 100 = 60 %

2. *The total power content of a AM signal is 1500 W. For 100 % modulation, determine (i) power transmitted by the carrier, (i) power transmitted by each sideband.*

Solution:

Given: P_T = 1500 W, m_a = 1, P_C = ?, P_{USB} = ?, P_{LSB} = ?

(i) $P_T = P_C [1 + (m_a^2/2)]$ or $P_C = P_T (2/(2 + m_a^2)) = P_T (2/(2 + 1^2)) = (2/3)P_T = (2/3)$ x 1,500 = 1,000 W

(ii) $P_{USB} = P_{LSB} = P_C (m_a^2/4) = 1000 \times (1^2/4) = 250$ W

3. *The total power content of an AM signal is 3 KW at a modulation index of 80 %. Determine (i) power transmitted by the carrier, (ii) power transmitted by each sideband.*

Solution:

Given: P_T = 3000 W, m = 0.8 P_C = ?, P_{USB} = ?, P_{LSB} = ?

(i) $P_T = P_C [1 + (m_a^2/2)]$ or $P_C = P_T (2/(2 + m_a^2)) = 3 \times 10^3 (2/(2 + 0.8^2)) = 2{,}273$ W

(ii) $P_{USB} = P_{LSB} = P_C (m_a^2/4) = 2{,}273 \times (0.8^2/4) = 363.68$ W

4. *A 500 W, 100 KHz carrier is modulated to a depth of 60 % by modulating signal of frequency 1 KHz. Calculate the total power transmitted. What are the side-band components of the A.M wave?*

(March 99, V.T.U.)

Solution:

Given P_C = 100 KHz and m = 0.6

(i) Total power $P_T = P_C [1 + (m_a^2/2)] = 500 (1 + (0.6^2/2)) = 590$ W

(ii) USB = $f_c + f_m$ = 101 KHz

(iii) LSB = $f_c - f_m$ = 99 KHz

5. *An amplitude-modulated carrier wave has maximum and minimum amplitudes of 750 mV and 250 mV respectively. Calculate the modulation index and the percentage modulation.*

Solution:

Given: V_{max} = 750 mV and V_{min} = 250 mV

(i) Modulation index,

$$m_a = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} = \frac{\left(750 \times 10^{-3}\right) - \left(250 \times 10^{-3}\right)}{\left(750 \times 10^{-3}\right) + \left(250 \times 10^{-3}\right)} = \frac{500}{1000} = 0.5$$

(ii) Percentage of modulation = m_a x 100 = 50 %

6. *A 100 MHz carrier wave is frequency modulated by a 10 KHz sinusoidal modulating signal. If the maximum frequency deviation is 50 KHz, find the modulation index.*

Solution:

Given: f_m = 10 KHz, Maximum frequency deviation = δ = 50 KHz

The Modulation Index for FM, m_f is defined as:

m_f = (Maximum frequency deviation / Modulating frequency) = δ/f_m = 50 KHz/10 KHz = 5

7. *Find the carrier frequency, modulating frequency, modulation index and the frequency deviation of the FM wave represented by v(t) = 12 sin (6 x 10^8) + 5 sin (1250t)*

Solution: The standard equation of FM is $v(t) = V_C \sin(\omega_C t + m_f \sin \omega_m t)$

Comparing the equation given in the problem with the above standard equation, we have

V_C = 12 V, $\omega_C = (6 \times 10^8)$, m_f = 5 and ω_m = 1250 Hz

(i) Carrier frequency, $f_c = \frac{\omega_c}{2\pi} = \frac{6 \times 10^8}{2 \times 3.142} = 95.48\ MHz$

(ii) Modulating frequency, $f_m = \frac{\omega_m}{2\pi} = \frac{1250}{2 \times 3.142} = 198.91 Hz$

(iii) Frequency deviation, $\delta = m_f f_m = 5 \times 198.91 = 994.55\ Hz$

(iv) Modulation Index, m_f = 5

7. 7 NUMBER SYSTEMS

A group of defined digits used to count the objects makes a number system. Number systems are differs in terms of their radix or base. A digit is a symbol given to an element of a number system. The radix, or base of a counting system is defined as the number of unique digits in a given number system.

The decimal number system with which we are all so familiar can be said to have a radix of 10 as it has 10 independent digits, i.e. 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. Similarly, the binary number system with only two independent digits, 0 and 1, is a radix-2 number system. The octal and hexadecimal number systems have a radix (or base) of 8 and 16 respectively.

7.7.1 Decimal Number System

The decimal number system has radix-10 and therefore uses 10 different digits or symbols. These are 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. All higher numbers after '9' are represented in terms of these 10 digits only. The process of writing higher-order numbers after '9' consists in writing the second digit (i.e. '1') first, followed by the other digits, one by one, to obtain the next 10 numbers from '10' to '19'. The next 10 numbers from '20' to '29' are obtained by writing the third digit (i.e. '2') first, followed by digits '0' to '9', one by one. The process continues until we have exhausted all possible two-digit combinations and reached '99'. Then we begin with three-digit combinations. The first three-digit number consists of the lowest two-digit number followed by '0' (i.e. 100), and the process goes on endlessly.

The place values of different digits in a mixed decimal number, starting from the decimal point, are 10^0, 10^1, 10^2 and so on (for the integer part) and 10^{-1}, 10^{-2}, 10^{-3} and so on (for the fractional part). The value or magnitude of a given decimal number can be expressed as the sum of the various digits multiplied by their place values or weights.

7.7.2 Binary Number System

The binary number system is a radix-2 number system with '0' and '1' as the two independent digits. All larger binary numbers are represented in terms of '0' and '1'. The procedure for writing higher order binary numbers after '1' is similar to the one explained in the case of the decimal number system. For example, the first 16 numbers in the binary number system would be 0, 1, 10, 11, 100, 101, 110, 111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 and 1111. The next number after 1111 is 10000, which is the lowest binary number with five digits. This also proves the point made earlier that a maximum of only 16 (= 2^4) numbers could be written with four digits. Starting from the binary point, the place values of different digits in a mixed binary number are 2^0, 2^1, 2^2 and so on (for the integer part) and 2^{-1}, 2^{-2}, 2^{-3} and so on (for the fractional part). A binary digit is shortly called bit.

The bit on the far right is known as the Least significant bit (LSB), and the bit on the far left is known as the Most significant bit (MSB). Various notations used in digital systems are:

4 bits = Nibble

8 bits = Byte

16 bits = Word

32 bits = Double word

64 bits = Quad Word (or paragraph)

When writing binary numbers we have to specify the base 2, for example take the value 101, as it is written it would be hard to know whether it is a binary or decimal (denary) value. To get around this problem it is common to denote the base to which the number belongs, by writing the base value with the number.

Ex. 1:

101_2 is a binary number and 101_{10} is a decimal (binary) value.

Once we know the base then it is easy to work out the value, for example:

$101_2 = 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 5$ (five)

$101_{10} = 1 \times 10^2 + 0 \times 10^1 + 1 \times 10^0 = 101$ (one hundred and one)

Advantages of Binary Number System:

Binary number system uses two digits 0 and 1 to represent any number. These two digits can be used to represent presence and absence of signal and hence used in digital communication and digital computation to represent and process information in binary form.

Binary to Decimal Conversion:

Procedure :

Step 1 : Multiply each bit of binary number with its associated place value.

Step 2 : Add the result and write as decimal equivalent number

Ex. 2: Convert $(0110)_2$ to decimal equivalent

Ans: $[(0 \times 2^3) + (1 \times 2^2) + (1 \times 2^1) + (0 \times 2^0)] = [0 + 4 + 2 + 0] = [6]_{10}$

Ex. 3: Convert $(1010.\ 11)_2$ to decimal equivalent

Ans: $[(1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1) + (0 \times 2^0) + (1 \times 2^{-1}) + (1 \times 2^{-2})] = [8 + 0 + 2 + 0 + (1 \times ½) + (1 \times ¼)] = [10.75]_{10}$

Ex. 4: Convert $(101101.10101)_2$ to decimal equivalent

Ans: $[1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4} + 1 \times 2^{-5}]$

$= 32 + 0 + 8 + 4 + 0 + 1/2 + 0 + 1/8 + 0 + 1/32$

$= (45.65625)_{10}$

Ex. 5: Convert $(1001.0101)_2$ to decimal equivalent

Ans: $[1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}]$

$= 8 + 0 + 0 + 1 + 0 + 1/4 + 0 + 1/16 = 9 + 0.25 + 0.0625$

$= (9.3125)_{10}$

Decimal to Binary Conversion:

Procedure:

For Integer Part :

Step 1 : Divide the given decimal number by 2.

Step 2 : Write the remainders bottom to top as binary number

For Fractional Part:

Step 1 : Multiply the given Fraction by 2 and keep track of integers generated

Step 2 : Write the Integers generated from left to right after binary point.

Ex. 6: Convert $(23)_{10}$ to equivalent binary number.

Ans: Divide 23 by 2 and write the remainder separately as shown below :

2	23	
2	11	– 1
2	5	– 1
2	2	– 1
2	1	– 0
2	0	– 1

Read binary number $(23)_{10}$ = $(10111)_2$

Read down to up and becomes binary equialent number

This says that binary 1 0 1 1 1 is equivalent to decimal 23.

Ex. 7: Convert $(13)_{10}$ to equivalent binary number.

Ans: Divide 13 by 2 and write the remainder separately as shown below :

2	13	
2	6	– 1
2	3	– 0
2	1	– 1
2	0	– 1

Write the remainders Bottom to Top as binary number i.e. $(1101)_2$

$(13)_{10} = (1101)_2$

Ex. 8: Convert $(0.65625)_{10}$ to equivalent binary number.

$0.65625 \times 2 = 1.31250$ ——> 1

$0.31250 \times 2 = 0.62500$ ——> 0

$0.62500 \times 2 = 1.25000$ ——> 1

$0.25000 \times 2 = 0.50000$ ——> 0

$0.50000 \times 2 = 1.00000$ ——> 1

$\therefore \quad (0.65625)_{10} = (0.10101)_2$

Ex. 9: Convert $(25.50)_{10}$ to equivalent binary number

(a) Integer Part: 25

2	25	
2	12	– 1
2	6	– 0
2	3	– 0
2	1	– 1
2	0	– 1

Read the reminders Bottom to Top ⟶ $(25)_{10} = (11001)_2$

(b) Fractional Part:

$0.5 \times 2 = 1.0$ ⟶ 1

$(0.5)_{10} = (0.1)_2$

Thus $(25.5)_{10} = (11001.1)_2$

Ex. 10: Convert $(10.625)_{10}$ to equivalent binary number

(a) Integer Part: $(10)_{10}$

2	10	– 0
2	05	– 1
2	02	– 0
2	01	– 1

Read Bottom to Top ⟶ $(10)_{10} = (1010)_2$

(b) Fractional Part: $(0.625)_{10}$

$0.625 \times 2 = 1.25$ ⟶ 1

$0.25 \times 2 = 0.50$ ⟶ 0

$0.50 \times 2 = 1.00$ ⟶ 1

Read Top to Bottom ⟶ $(0.625)_{10} = (0.101)_2$

Thus $(10.625)_{10} = (1010.101)_2$

7.7.3 Octal and Hexadecimal Number Systems

Octal Number System:

The octal number system has a radix of 8 and therefore has eight distinct digits. All higher-order numbers are expressed as a combination of these on the same pattern as the one followed in the case of

the binary and decimal number systems. The independent digits are 0, 1, 2, 3, 4, 5, 6 and 7. The next 10 numbers that follow '7', for example, would be 10, 11, 12, 13, 14, 15, 16, 17, 20 and 21. In fact, if we omit all the numbers containing the digits 8 or 9, or both, from the decimal number system, we end up with an octal number system. The place values for the different digits in the octal number system are 8^0, 8^1, 8^2 and so on (for the integer part) and 8^{-1}, 8^{-2}, 8^{-3} and so on (for the fractional part).

Decimal to Octal Conversion:

Procedure:

For Integer Part:

Step 1 : Divide the given decimal number by 8.

Step 2 : Write the remainders Bottom to Top as octal number

For Fractional Part :

Step 1 : Multiply the given Fraction by 8 and keep track of integers generated

Step 2 : Write the Integers generated from Top to Bottom after decimal point.

Ex. 11: Convert 247 to Octal

		Quotient	Remainder
8 | 247			
8 | 30	– 7	30	7
8 | 3	– 6	3	6
8 | 0	– 3	0	3

Read the reminder from Bottom to Top. $(247)_{10} = (367)_8$

Ex. 12: Convert 0.6875 to Octal

0.6875 x 8 = 5.5000 ——> 5

0.5000 x 8 = 4.0000 ——> 4

Read the generated integers Top to Bottom $(0.6875)_{10} = (0.54)_8$

Ex. 13: Convert $(3287.5100098)_{10}$ to Octal

Integer Part:

		Quotient	Remainder
8 | 3287			
8 | 410	– 7	410	7
8 | 51	– 2	51	2
8 | 6	– 3	6	3
8 0	– 6	0	6

Read the reminder from Bottom to Top as $(3287)_{10} = (6327)_8$

Fractional Part:

0.5100098	0.0800784	0.6406272	0.1250176
× 8	× 8	× 8	× 8
4.0800784	0.6406272	5.1250176	1.0001408
4	0	5	1

Read the Integers from Left to Right as $(0.5100098)_{10} = (0.4051)_8$

Thus $(3287.5100098)_{10} = (6327.4051)_8$

Octal to Decimal Conversion:

Procedure:

Step 1 : Multiply each digit of octal number with its associated place value.

Step 2 : Add the result and write as decimal equivalent number

Ex. 14: Convert $(567)_8$ to Decimal equivalent number

Ans: $(5 \times 64) + (6 \times 8) + (7 \times 1) = (375)_{10}$

Ex. 15: Convert $(321.37)_8$ to Decimal equivalent number

Ans: (3 x 64) + (2 x 8) + (1 x 1) . (3 x 1/8) + (7 x 1/64) = (192 + 16 + 1) . (0.375 + 0.109375)

= $(209.4844)_{10}$

Octal to Binary Conversion:

Procedure:

Step 1 : Convert each digit of octal number in to corresponding three bit binary number.

Step 2 : Write the three bit binary numbers together to represent in binary form.

Ex. 16: Convert $(351)_8$ to binary equivalent

3 ——> 011

5 ——> 101

1 ——> 001

$(351)_8 = (011101001)_2$

Ex. 17: Convert $(730)_8$ to binary equivalent

7 ——> 111

3 ——> 011

0 ——> 000

$(730)_8 = (111011000)_2$

Binary to Octal Conversion:

Procedure:

Step 1 : Separate given binary number in to three bit groups by adding 0 at left side if required.

Step 2 : Convert each three bit group into its equivalent octal number and write them together.

Ex. 18: Convert $(010111100001)_2$ to octal equivalent

010 = 2

111 = 7

100 = 4

001 = 1

$(010111100001)_2 = (2741)_8$

Ex. 19: Convert $(110011001)_2$ in to octal equivalent

110 = 6

011 = 3

001 = 1

$(110011001)_2 = (631)_8$

Hexadecimal Number System:

The hexadecimal number system is a radix-16 number system and its 16 basic digits are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F. The place values or weights of different digits in a mixed hexadecimal number are 16^0, 16^1, 16^2 and so on (for the integer part) and 16^{-1}, 16^{-2}, 16^{-3} and so on (for the fractional part). The decimal equivalent of A, B, C, D, E and F are 10, 11, 12, 13, 14 and 15 respectively, for obvious reasons.

The hexadecimal number system provides a condensed way of representing large binary numbers stored and processed inside the computer. One such example is in representing addresses of different memory locations. Let us assume that a machine has 64 K of memory. Such a memory has 64 K (= 2^{16} = 65,536) memory locations and needs 65,536 different addresses. These addresses can be designated as 0 to 65,535 in the decimal number system and 00000000 00000000 to 11111111 11111111 in the binary number system. The decimal number system is not used in computers and the binary notation here appears too cumbersome and inconvenient to handle. In the hexadecimal number system, 65,536 different addresses can be expressed with four digits from 0000 to FFFF. Similarly, the contents of the memory when represented in hexadecimal form are very convenient to handle.

Table 7.1 Hexadecimal numbers with equivalent decimal and binary numbers

Decimal (base10)	Binary (base 2)	Hexadecimal (base 16)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Hexadecimal to Binary Conversion:

To convert a hexadecimal number into a binary number we follow the following two steps:

Step 1 : Convert each Hexadecimal in to its 4-bit binary equivalent (Nibble).

Step 2 : Combine these nibbles by removing the spaces.

Ex. 20: Convert $(4ED3)_{16}$ to Binary equivalent

Step 1 : 0100, 1110, 1101, 0011

Step 2 : $(0100111011010011)_2$

Ex. 21: Convert $(63B1)_{16}$ to binary equivalent

Step 1 : 0110, 0011, 1011, 0001

Step 2 : $(0110001110110001)_2$

Ex. 22: Convert $(4A.91C)_{16}$ to binary equivalent

Step 1 : 0100, 1010, . 1001, 0001, 1100

Step 2 : $(01001010 . 100100011100)_2$

Hexadecimal numbers offer the two features:

(1) hex numbers are very compact

(2) it is easy to convert from hex to binary and binary to hex.

The Hexadecimal system is based on the binary system using a Nibble or 4-bit unit. In Assembly Language programming, most assemblers require the first digit of a hexadecimal number to be 0, and place an "h" at the end of the number to denote the number base.

Binary to Hexadecimal Conversion:

Step 1 : Group the bits of given binary number in to nibbles by adding 0's in left side if required.

Step 2 : Convert each nibble into its equivalent hexadecimal unit number.

Step 3 : Arrange these hexadecimal units into corresponding hexadecimal number

Ex. 23: Convert $(1001101011)_2$ to hexadecimal number

Step 1 : Add two zeros to the left to get 3 nibbles : 0010, 0110, 1011

Step 2 : Convert each nibble in to its hexadecimal equivalent unit : 2, 6, A

Step 3 : Arrange into corresponding hexadecimal number : $(26A)_{16}$

Ex. 24: Convert $(101101101101111)_2$ to hexadecimal number

Step 1 : Add one zero to the left to get 4 nibbles : 0101, 1011, 0110, 1111

Step 2 : Convert each nibble in to its hexadecimal equivalent unit : 5, A, 6, E

Step 3 : Arrange into corresponding hexadecimal number : $(5A6E)_{16}$

Ex. 25: Convert $(11101111001. 01110001)_2$ to hexadecimal number

Step 1 : Add one zero to the left to get 5 nibbles : 0111, 0111, 1001, . 0111, 0001

Step 2 : Convert each nibble in to its hexadecimal equivalent unit : 5, 5, 9, . 7, 1

Step 3 : Arrange into corresponding hexadecimal number : $(559. 71)_{16}$

Hexadecimal to Decimal Conversion:

Procedure :

Step 1 : Each hexadecimal digit is multiplied by corresponding position value.

Step 2 : Add all resultant numbers to get decimal equivalent

Ex.26: Convert $(2BC3)_{16}$ to decimal equivalent

$= 2 \times 16^3 + B \times 16^2 + C \times 16^1 + 3 \times 16^0$

$= 2 \times 16^3 + 11 \times 16^2 + 12 \times 16^1 + 3 \times 16^0$

= 8192 + 2816 + 192 + 3

= $(11203)_{10}$

Decimal to Hexadecimal Conversion:

Procedure:

Step 1 : Divide the given decimal number by 16.

Step 2 : Write the remainders Bottom to Top as hexadecimal number

Ex. 27: Convert $(17203)_{10}$ to hexadecimal equivalent

16 | 17203 ——> 1

16 | 120 ——> 7

16 | 53 ——> 3

16 | 5 ——> 5

Hence $(17203)_{10} = (5371)_{16}$

7.7.4 Binary Arithmetic

Two types of operation that are performed on binary data include arithmetic and logic operations. Basic arithmetic operations include addition, subtraction, multiplication and division. The basic logic functions are AND, OR and NOT. The rules of arithmetic operations are discussed for addition and subtraction.

Addition

The basic principles of binary addition is that while adding '0' to a certain digit produces the same digit as the sum, and, while adding '1' to a certain digit or number in the binary number system, is the next higher digit of number. Similarly the case in decimal number system. For example, 6 + 1 in decimal equals '7' because '7' immediately follows '6' in the decimal number system. Also, 7 + 1 in octal equals '10' as, in the octal number system, the next adjacent higher number after '7' is '10'. Similarly, 9 + 1 in the hexadecimal number system is 'A'. With this background, we can write the basic rules of binary addition as follows:

1. 0 + 0 = 0.
2. 0 + 1 = 1.
3. 1 + 0 = 1.
4. 1 + 1 = 0 with a carry of '1' to the next more significant bit.
5. 1 + 1 + 1 = 1 with a carry of '1' to the next more significant bit.

Table 7.2 summarizes the sum and carry outputs of all possible three-bit combinations. We have taken three-bit combinations as, in all practical situations involving the addition of two larger bit numbers, we need to add three bits at a time. Two of the three bits are the bits that are part of the two binary numbers to be added, and the third bit is the carry-in from the next less significant bit column.

Table 7.2 Binary addition of 3 bits

A	B	Carryin (C_{in})	Sum	Carry out (C_o)	A	B	Carryin (C_{in})	Sum (C_o)	Carry out
0	0	0	0	0	1	0	0	1	0
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
0	1	1	0	1	1	1	1	1	1

The addition of larger binary integers, fractions or mixed binary numbers is performed columnwise in just the same way as in the case of decimal numbers. In the case of binary numbers, however, we follow the basic rules of addition of two or three binary digits, as outlined earlier.

Consider two generalized four-bit binary numbers ($A_3\ A_2\ A_1\ A_0$) and ($B_3\ B_2\ B_1\ B_0$), with A_0 and B_0 representing the LSB and A_3 and B_3 representing the MSB of the two numbers. The addition of these two numbers is performed as follows. We begin with the LSB position. We add the LSB bits and record the sum S_0 below these bits in the same column and take the carry C_0, if any, to the next column of bits. For instance, if $A_0 = 1$ and $B_0 = 0$, then $S_0 = 1$ and $C_0 = 0$. Next we add the bits A_1 and B_1 and the carry C_0 from the previous addition. The process continues until we reach the MSB bits. The four steps are shown in Table 7.3. C_0, C_1, C_2 and C_3 are carrys, if any, produced as a result of adding first, second, third and fourth column bits respectively, starting from LSB and proceeding towards MSB. A similar procedure is followed when the given numbers have both integer as well as fractional parts:

Table 7.3 Procedure of binary addition

			(C_0)		
1.	A_3	A_2	A_1	A_0	
	B_3	B_2	B_1	B_0	
				S_0	

			(C_1)	(C_0)	
2.	A_3	A_2	A_1	A_0	
	B_3	B_2	B_1	B_0	
			S_1	S_0	

	(C_2)	(C_1)	(C_0)		
3.	A_3	A_2	A_1	A_0	
	B_3	B_2	B_1	B_0	
		S_2	S_1	S_0	

		(C_2)	(C_1)	(C_0)	
4.		A_3	A_2	A_1	A_0
		B_3	B_2	B_1	B_0
	C_3	S_3	S_2	S_1	S_0

Ex. 28: Add 101_2 and 110_2

Solution:

$$\begin{array}{r} 101 \\ \underline{110} \\ 1011 \end{array}$$

Ex. 29: Add 1101_2 and 1010_2

Solution:

$$\begin{array}{r} 1101 \\ \underline{1010} \\ 01111 \end{array}$$

Ex. 30: Add 110111_2 and 100110_2

Solution:

$$\begin{array}{r} 110111 \\ \underline{100110} \\ 1011101 \end{array}$$

Subtraction

The basic principles of binary subtraction include the following :

1. $0 - 0 = 0$.
2. $1 - 0 = 1$.
3. $1 - 1 = 0$.
4. $0 - 1 = 1$ with a borrow of 1 from the next more significant bit.

The above-mentioned rules can also be explained by recalling rules for subtracting decimal numbers. Subtracting '0' from any digit or number leaves the digit or number unchanged. This explains the first two rules. Subtracting '1' from any digit or number in decimal produces the immediately preceding digit or number as the answer. In general, the subtraction operation of larger-bit binary numbers also involves three bits, including the two bits involved in the subtraction, called the minuend (the upper bit) and the subtrahend (the lower bit), and the borrow-in. The subtraction operation produces the difference output and borrow-out, if any. Table 7.4 summarizes the binary subtraction operation. The entries in Table 7.4 can be explained by recalling the basic rules of binary subtraction mentioned above, and that the subtraction operation involving three bits, that is, the minuend (A), the subtrahend (B) and the borrow-in (B_{in}), produces a difference output equal to ($A - B - B_{in}$).

It may be mentioned here that, in the case of subtraction of larger-bit binary numbers, the least significant bit column always involves two bits to produce a difference output bit and the borrow-out bit. The borrow-out bit produced here becomes the borrow-in bit for the next more significant bit column, and the process continues until we reach the most significant bit column.

Table 7.4 Binary subtraction

Inputs			Outputs	
Minuend (A)	Subtrahend (B)	Borrow-in (B_{in})	Dirrerence (D)	Borrow-out (B_o)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Subtraction is also done columnwise in the same way as in the case of the decimal number system. In the first step, we subtract the LSBs and subsequently proceed towards the MSB. Wherever the subtrahend (the bit to be subtracted) is larger than the minuend, we borrow from the next adjacent higher bit position having a '1'.

As an example, let us go through different steps of subtracting $(1001)_2$ from $(1100)_2$. In this case, '1' is borrowed from the second MSB position, leaving a '0' in that position. The borrow is first brought to the third MSB position to make it '10'. Out of '10' in this position, '1' is taken to the LSB position to make '10' there, leaving a '1' in the third MSB position.

10—1 in the LSB column gives '1', 1— 0 in the third MSB column gives '1', 0 — 0 in the second MSB column gives '0' and 1 — 1 in the MSB also gives '0' to complete subtraction. Subtraction of mixed numbers is also done in the same manner. The above-mentioned steps are summarized in Table 7.5:

Table 7.5 Example for binary subtraction

1.	1	1	0	0	**2.**	1	1	0	0
	1	0	0	1		1	0	0	1
				1				1	1
3.	1	1	0	0	**4.**	1	1	0	0
	1	0	0	1		1	0	0	1
		0	1	1		0	0	1	1

Ex. 31: Subtract $(1110.011)_2$ from $(11011.11)_2$ using basic rules of binary subtraction and verify the result by showing equivalent decimal subtraction.

$$\begin{array}{r} 11011.110 \\ -01110.011 \\ \hline 01101.011 \end{array}$$

Complement of a Number

In binary system, two types of complementary system are used for binary subtraction. They are 1's complement and 2's complement.

1's Complement:

1's complement of a binary number is obtained by changing its each 0 into 1 and each 1 into 0. It is also called radix minus one complement. For example, 1's complement of 100_2 is 011_2 and 1110_2 is 0001_2.

2's Complement:

The 2's complement of a binary number is obtained by adding 1 to its 1's complement.

2's complement = 1's complement + 1

It is also called true complement. For example, to find 2's complement of 1100_2, first calculate 1's complement as 0011_2 then add 1 leads to 0100_2. Hence 2's complement of 1100_2 is 0100_2.

The complement method of subtraction is popular in digital computers because :

(i) Only adder circuits are needed thus simplifying the circuitry.

(ii) It is easy with digital circuits to get the complements.

1's Complement Subtraction:

In this method, instead of subtracting a number (subtrahend) from given number (minuend), we add its 1's complement to the given number and the last carry (whether 0 or 1) is then added to get the final number. The procedure for subtraction is given below:

(1) Compute 1's complement of the subtrahend by changing all its 1's to 0's and all its 0s to 1's.

(2) Add this complement number to the minuend

(3) Perform end-around-carry of the last 1 or 0

(4) If the end around carry is 0, the answer must be re-complemented and a negative sign must be attached to it. This is the answer.

(5) If the end-around-carry is 1, then no re-complementing is required and the result is the answer.

Ex. 32: Subtract 101_2 from 111_2

Ans: 111 – 101 => 111 + 010 => $(1001)_2$.

Since the end-around carry is 1, this carry has to be added to the remainder => 001 + 1 = 010.

Hence the answer is 010.

Ex. 33: Subtract 1101_2 from 1010_2

Ans: 1010 – 1101 => 1010 + 0010 => 01100. Since the end around carry is 0, the answer must be re-complemented and negative sign must be attached to it.

Hence the final answer is $(-\ 0011)_2$

Ex. 34: Using 1's complement method, subtract 01101_2 from 11011_2

Ans: 11011 – 01101 => 11011 + 10010 = 101101. Since the end around carry is 1, this carry has to be added to the remainder => 01101 + 1 = $(01110)_2$

Ex. 35: Using 1's complement method, subtract 11011_2 from 01101_2

Ans: 01101 — 11011 => 01101 + 00100 = 010001 => Since end around carry is 0. Re-complement and attach negative sign. Hence the final answer is $(-\ 01110)_2$.

2's Complement Subtraction:

The procedure of subtraction using 2's complement is given below:

(1) Find the 2's complement of the subtrahend

(2) Add this complement to the minuend

(3) Drop the final carry

(4) If the carry is 1, the answer is positive and needs no re-complementing

(5) If there is no carry, re-complement the answer and attach the minus sign

Ex. 36: Using 2's complement subtract 1010_2 from 1101_2

Ans: 1101 – 1010 => 1's complement of 1010 = 0101. The 2's complement is 0101 + 1 = 0110.

1101 + 0110 = 10011 => Since end around carry is 1, the answer is positive and needs no re-complementing and also drop the final carry. Hence the answer is 0011_2

Ex. 37: Using 2's complement subtract 1101_2 from 1010_2

Ans: 1010 – 1101 => 1010 + (0010 +1) = 1010 + 0011 = 01101 => Since end around carry is 0, we have to re-complemet the answer. i.e., subtract 1 and complement the answer. => 1101 – 1 = 1100 => complementing gives => 0011_2.

Fractional number

Floating-point notation can be used conveniently to represent both large as well as small fractional or mixed numbers. This makes the process of arithmetic operations on these numbers relatively much easier. Floating-point representation greatly increases the range of numbers, from the smallest to the largest, that can be represented using a given number of digits. Floating-point numbers are in general expressed in the form

$$N = m \times be \qquad ...(7.1)$$

where m is the fractional part, called the *significand* or *mantissa*, e is the integer part, called the *exponent*, and b is the *base* of the number system or numeration. Fractional part m is a p-digit number of

the form (±d.*dddd _ _ _ dd*), with each digit d being an integer between 0 and b – 1 inclusive. If the leading digit of m is nonzero, then the number is said to be normalized.

Equation (7.1) in the case of decimal, hexadecimal and binary number systems will be written as follows:

Decimal system

N = m × 10e

Hexadecimal system

N = m × 16e

Binary system

N = m × 2e

For example, decimal numbers 0.0003754 and 3754 will be represented in floating-point notation as 3.754×10^{-4} and 3.754×10^{3} respectively. A hex number 257.ABF will be represented as $2.57ABF \times 16^{2}$. In the case of normalized binary numbers, the leading digit, which is the most significant bit, is always '1' and thus does not need to be stored explicitly.

Also, while expressing a given mixed binary number as a floating-point number, the radix point is so shifted as to have the most significant bit immediately to the right of the radix point as a '1'. Both the mantissa and the exponent can have a positive or a negative value.

The mixed binary number $(110.1011)_2$ will be represented in floating-point notation as $.1101011 \times 2^3 = .1101011e+0011$. Here, .1101011 is the mantissa and e+0011 implies that the exponent is +3. As another example, $(0.000111)_2$ will be written as .111e – 0011, with .111 being the mantissa and e–0011 implying an exponent of –3. Also, $(-0.00000101)_2$ may be written as $-.101 \times 2^{-5} = -.101e-0101$, where –.101 is the mantissa and e–0101 indicates an exponent of –5. If we wanted to represent the mantissas using eight bits, then .1101011 and .111 would be represented as .11010110 and .11100000.

7.7.5 Binary Coded Decimal numbers

The binary coded decimal (BCD) is a type of binary code used to represent a given decimal number in an equivalent binary form. BCD-to-decimal and decimal-to-BCD conversions are very easy and straightforward. It is also far less cumbersome an exercise to represent a given decimal number in an equivalent BCD code than to represent it in the equivalent straight binary form.

The BCD equivalent of a decimal number is written by replacing each decimal digit in the integer and fractional parts with its four-bit binary equivalent. As an example, the BCD equivalent of $(23.15)_{10}$ is written as $(0010\ 0011.0001\ 0101)_{BCD}$. The BCD code described above is more precisely known as the 8421 BCD code, with 8, 4, 2 and 1 representing the weights of different bits in the four-bit groups, starting from MSB and proceeding towards LSB. This feature makes it a weighted code, which means that each bit in the four-bit group representing a given decimal digit has an assigned weight. Other weighted BCD codes include the 4221 BCD and 5421 BCD codes. Again, 4, 2, 2 and 1 in the 4221 BCD code and 5, 4, 2 and 1 in the 5421 BCD code represent weights of the relevant bits. Table 7.6 shows a comparison of 8421, 4221 and 5421 BCD codes. As an example, $(98.16)_{10}$ will be written as 1111 1110.0001

1100 in 4221 BCD code and 1100 1011.0001 1001 in 5421 BCD code. Since the 8421 code is the most popular of all the BCD codes, it is simply referred to as the BCD code.

Table 7.6 BCD codes

Decimal	8421 BCD code	4221 BCD code	5421 BCD code
0	0000	0000	0000
1	0001	0001	0001
2	0010	0010	0010
3	0011	0011	0011
4	0100	1000	0100
5	0101	0111	1000
6	0110	1100	1001
7	0111	1101	1010
8	1000	1110	1011
9	1001	1111	1100

BCD-to-Binary Conversion

A given BCD number can be converted into an equivalent binary number by first writing its decimal equivalent and then converting it into its binary equivalent.

Ex. 38: Find the binary equivalent of the BCD number 0010 1001.0111 0101

- BCD number: 0010 1001.0111 0101.
- Corresponding decimal number: 29.75.
- The binary equivalent of 29.75 can be determined to be 11101 for the integer part and .11 for the fractional part.
- Therefore, $(0010\ 1001.0111\ 0101)_{BCD} = (11101.11)_2$.

Binary-to-BCD Conversion

The process of binary-to-BCD conversion is the same as the process of BCD-to-binary conversion executed in reverse order. A given binary number can be converted into an equivalent BCD number by first determining its decimal equivalent and then writing the corresponding BCD equivalent.

Ex. 39: Find the BCD equivalent of the binary number $(10101011.101)_2$.

- The decimal equivalent of this binary number can be determined to be 171.625.
- The BCD equivalent can then be written as 0001 0111 0001.0110 0010 0101.

EXERCISES

I. Descriptive Type Questions

1. With block diagram, explain the process & components of electronic communication.
2. What is modulation ? Explain various types of modulation ?
3. What is the need of modulation ?
4. Obtain an expression for voltage in A.M. signal. What are the side bands and modulation index ?
5. Obtain an expression for power relations in A.M.
6. Define Frequency modulation ? Obtain an expression for FM signal and modulation index ?
7. Write a note on frequency spectrum of F.M. ?
8. Define Phase modulation and obtain an expression for it ?
9. Compare AM & FM ?
10. With block diagram, explain various stages of AM transmitter ?
11. With block diagram, explain various stages of FM transmitter ?
12. What is the principle of superhetrodyne ?
13. With block diagram, explain various stages of AM superhetrodyne receiver ?
14. With block diagram, explain various stages of FM superhetrodyne receiver ?
15. Explain the need of modulation *(VTU Jan 2009)*
16. Calculate the modulation index using AM wave *(VTU June 2007)*
17. Explain with neat wave forms the principle of amplitude modulation. Write the expression for AM wave. *(VTU Jan 2010)*
18. Draw the block diagram of super hetrodyne AM receiver and explain the function of each block. *(VTU June 2009, VTU Jan 2009)*
19. Draw the block diagram of a super heterodyne AM receiver and explain the function of each block.
20. Distinguish between weighted and unweighted codes. Give two examples each of both types of code.
21. What is meant by the radix or base of a number system? Briefly describe why hex representation is used for the addresses and the contents of the memory locations in the main memory of a computer.

II. Multiple Choice Questions

1 The AM signal that occupies the greatest bandwidths is the one modulated by _____

(a) 1 KHz sine wave (b) 10 KHz sine wave

(c) 1 KHz square wave (d) 5 KHz square wave

2. The circuit that recovers the original modulating information from an AM signal is known as ___
   (a) Modulator (b) Mixer
   (c) Demodulator (d) Oscillator
3. On an FM signal, maximum deviation occurs at _____
   (a) Zero crossing point (b) Peak positive amplitude
   (c) Peak negative amplitude (d) Both (A) and (C)
4. The binary equivalent of the decimal nummber 5 is _____
   (a) 100 (b) 101
   (c) 110 (d) 1001
5. $(11011)_2$ = (_____)
   (a) $(33)_8$ (b) $(17)_8$
   (c) $(25)_8$ (d) $(28)_8$
6. The 2's complement of 1100110 is _____
   (a) 0011001 (b) 0011010
   (c) 1100001 (d) 1100010
7. The BCD representation of decimal 10 is _____
   (a) 00001010 (b) 00001001
   (c) 00010000 (d) 10100000
8. The binary equivalent of $(A5)_{16}$ is _____
   (a) 00100111 (b) 00100101
   (c) 10100101 (d) 10100000
9. $(25)_{10} = (?)_2$
   (a) $(00111)_2$ (b) $(11001)_2$
   (c) $(11000)_2$ (d) $(00011)_2$
10. $(101011.11001)_2 = (?)_{16}$
    (a) $(AB.2C)_{16}$ (b) $(2C.B8)_{16}$
    (c) $(2B.C8)_{16}$ (d) $(2C.2D)_{16}$
11. 2's complement of binary number 10110 is _____
    (a) 00011 (b) 01010
    (c) 11100 (d) 11111
12. $(763.634)_8 = (?)_2$
    (a) $(111110011.110011100)_2$ (b) $(101011001.110011001)_2$
    (c) $(000011110.111100001)_2$ (d) $(010101010.001100110)_2$

13. The digital systems usually operate on _____ system.
    (a) binary (b) decimal
    (c) octal (d) hexadecimal
14. The binary system uses powers of _____ for positional values.
    (a) 2 (b) 10
    (c) 8 (d) 16
15. The number 1000_2 is equivalent to decimal number
    (a) one thousand (b) eight
    (c) four (d) sixteen
16. The binary addition 1+1+1 gives
    (a) 111 (b) 10
    (c) 110 (d) 11
17. The 2's complement of 1000_2 is
    (a) 0111 (b) 0101
    (c) 1000 (d) 0001
18. The chief reason why digital computers use complemental subtraction is that
    (a) simplifies their circuitry (b) is a very simple process
    (c) can handle negative numbers easily (d) avoids direct subtraction
19. The number 12_8 is equivalent to decimal
    (a) 12 (b) 20
    (c) 10 (d) 4
20. The number 100101_2 is equivalent to
    (a) 54 (b) 45
    (c) 37 (d) 25
21. The number 17_8 is equivalent to binary
    (a) 111 (b) 1110
    (c) 10000 (d) 1111
22. Which of the following is NOT an octal number?
    (a) 19 (b) 77
    (c) 15 (d) 101

23. Hexadecimal number system is used as a shorthand language for representing _____ numbers.
    (a) decimal (b) binary
    (c) octal (d) large
24. The binary equivalent of A_{16} is
    (a) 1010 (b) 1011
    (c) 1000 (d) 1110
25. In amplitude modulation ____
    (a) The amplitude of the carrier signal varies according to modulating signal
    (b) The frequency of the carrier signal varies according to modulating signal
    (c) The phase angle of the carrier signal varies according to modulating signal
    (d) All of these
26. The expression for channel capacity with band width B and, Signal to Noise Ratio *S/N* is ____
    (a) [B $\log_2$ (l + S/N)] bits/sec. (b) [$\log_2$ (B + S/N)] bits/sec.
    (b) [B $\log_2$ (l - S/N)] bits/sec. (c) [$\log_2$ (B + S/N)] bits/sec.
27. The telephone line has a Band width (BW) of _____
    (a) 3 KHz (b) 30 KHz
    (c) 3 MHz (d) 30 MHz

III. Numerical Problems

1. A 500 W, 100 KHz carrier is modulated to a depth of 60 % by modulating signal frequency of 1 KHz. Calculate the total power transmitted. What are the sideband components of the AM wave? *(VTU Jan 2010)*
2. A carrier of 750 W, 1 MHz is amplitude modulated by sinusoidal signal of 2 KHz to a depth of 50%. Calculate bandwidth, power in each side band and total power transmitted.*(VTU Jan 2008)*
3. A carrier of 500 W, 1 MHz is amplitude modulated by sinusoidal signal of 1 KHz to a depth of 60%. Calculate bandwidth, power in each side band and total power transmitted. *(VTU Jan 2007)*
4. For an AM, amplitude of modulating signal is 0.5 V and carrier amplitude is 1 V. Find modulation index. *(VTU Jan 2007)*
5. A carrier of 500 W, 100 KHz is amplitude modulated by sinusoidal signal of 1 KHz to a depth of 60%. Calculate bandwidth, power in each side band and total power transmitted. *(VTU Jan 2010)*
6. Convert the following binary numbers to decimal numbers.
    (i) 1101 (ii) 10001
    (iii) 10101.

7. (i) Convert $(10110011010)_2$ into octal, decimal and hexadeciamal; (ii) Subtract using 2's complement $(15 - 7)_{10}$ *(VTU June 2009)*
8. Subtract using 2's complement : (i) [4 – 9], (ii) [8 – 2]
9. Convert the following hexadecimal numbers into decimal : (i) $A3B_H$, (ii) $2F3_H$
10. Convert each decimal to binary (i) 11.125, (ii) 0.625
11. Determine the base value of x if $(211)x = (152)_8$
12. Convert the following decimal numbers to binary:
    (a) 623 (b) 73.17
    (c) 53.45 (d) 2.575
13. Convert the following binary numbers to decimal:
    (a) 10110110 (b) 110000101
    (c) 100.1101 (d) 1.001101
14. Convert the following binary numbers to hexadecimal and octal:
    (a) 100101010011 (b) 001011101111
    (c) 1011.111010101101 (d) 1111.100000011110
15. Convert the following octal numbers to binary and hexadecimal:
    (a) 1026 (b) 7456
    (c) 5566 (d) 236.2345
16. Convert the following hexadecimal numbers to binary and octal:
    (a) EF69 (b) 98AB5
    (c) DAC.IBA (d) FF.EE
17. Perform the addition of the following binary numbers:

    (a)
    $$\begin{array}{r} 100011 \\ +\ 1101 \\ \hline \end{array}$$

    (b)
    $$\begin{array}{r} 10110110 \\ +\ 11100011 \\ \hline \end{array}$$

    (c)
    $$\begin{array}{r} 10110011 \\ +\ 1101010 \\ \hline \end{array}$$

18. Perform the following subtractions, where each of the numbers is in binary form:

    (a)
    $$\begin{array}{r} 101101 \\ -\ 111110 \\ \hline \end{array}$$

    (b)
    $$\begin{array}{r} 1010001 \\ -\ 1001111 \\ \hline \end{array}$$

    (c)
    $$\begin{array}{r} 10000110 \\ -\ 1110001 \\ \hline \end{array}$$

19. Add the following pairs of numbers, where each number is in hexadecimal form:

(a) ABCD + 75EF

(b) 129A + Ab22

(c) EF23 + C89

20. Add the following pairs of numbers, where each number is in octal form:

(a) 7521 + 4370

(b) 62354 + 3256

(c) 3567 + 2750

Answers to Multiple Choice Questions

1. (b)	2. (c)	3. (d)	4. (b)	5. (a)	6. (b)	7. (c)	8. (c)	9. (b)	10. (c)	11. (b)
12 (a)	13. (a)	14. (a)	15. (b)	16. (d)	17. (c)	18. (a)	19. (c)	20. (c)	21. (d)	22. (a)
23. (b)	24. (a)	25. (a).	26. (a)	27. (a)						

UNIT 8

DIGITAL LOGIC

OBJECTIVES

Digital techniques proved their importance both in electronic computers and electronic communications due to many advantages compared to analog techniques. The basic building blocks of digital circuits are logic gates which can be used in the design and construction of both combinational and sequential logic circuits. Logic gates functions using the principle of non conventional algebra called Boolean algebra. By understanding Boolean algebra and various logic gates which functions using the principle of Boolean algebra, one can design complicated electronic circuits for digital computers and digital communication devices. In this chapter, we will study the Boolean algebra, various logic gates and binary adders using logic gates.

The objectives are:

(1) To study and understand Boolean algebra and Boolean properties.

(2) To design and analyze Logic gates.

(3) To design and analyze Half-adder, Full-adder, and Parallel Binary adder.

8.1 INTRODUCTION

8.1.1 Digital Signal

A digital signal is an electrical signal with two levels, (say, 0 volt & 5 volts) or states representing 0 and 1 digits of binary system. It varies between these two levels instantaneously and abruptly depending on the value of the signal. It can be represented in rectangular or square waveform as shown in Fig 8.1.

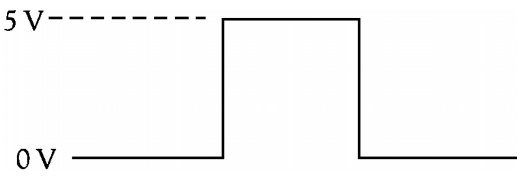


Figure 8.1 *Representation of digital signal*

8.1.2 Digital Systems

A digital circuit is one in which the voltage levels assume a finite number of distinct values. Digital circuits are often called switching circuits, because the voltage levels in a digital circuit are assumed to be switched from one value to another instantaneously, that is, the transition time is assumed to be zero. Digital circuits are also called logic circuits, because each type of digital circuit obeys a certain set of logic rules. Digital systems are used extensively in computation and data processing, control systems, communications and measurement.

Digital systems have a number of advantages over analog systems. Many tasks formally done by analog systems are now being performed digitally. The main reasons for the shift to digital technology are given below :

(i) **Digital systems are easier to design:** The switching circuits in which there are only two voltage levels, HIGH and LOW, are easier to design. The exact numerical values of voltages are not important because they have only logical significance; only the range in which they fall is important. In analog systems, signals have numerical significance; so, their design is more complex.

(ii) **Information storage is easy:** There are many types of semiconductor and magnetic memories of large capacity which can store data for long periods.

(iii) **Accuracy and precision are greater:** Digital systems are much more accurate and precise than analog systems, because digital systems can be easily expanded to handle more digits by adding more switching circuits. Analog systems will be quite complex and costly for the same accuracy and precision.

(iv) **Digital systems are more versatile:** It is fairly easy to design digital systems whose operation is controlled by a set of stored instructions called the *program*. Any time the system operation is to be changed, it can easily be accomplished by modifying the program. Even though analog systems can also be programmed, the variety of the available operations is severely limited.

(v) **Digital circuits are less affected by noise:** Unwanted electrical signals are called noise. In analog systems the exact values of voltages are important and in digital systems only the range of values is important. The effect of noise is more severe in analog systems. In digital systems, noise is not critical as long as it is not large enough to prevent us from distinguishing a HIGH from a LOW.

(vi) **More digital circuitry can be fabricated on IC chips:** The fabrication of digital ICs is simpler and economical than that of analog ICs. Moreover, higher densities of integration can be achieved in digital ICs than in analog ICs, because digital design does not require high value capacitors, precision resistors, inductors and transformers (which cannot be integrated economically) like the analog design.

Limitations of digital techniques:

Even though digital techniques have a number of advantages, they have only one major drawback. THE REAL WORLD IS ANALOG. Most physical quantities are analog in nature, and it is these quantities that are often the inputs and outputs and continually monitored, operated and controlled by a system. When these, quantities are processed and expressed digitally, we are really making a digital approximation to an analog quantity. Instead of processing the analog information directly, it is first converted into digital form and then processed using digital techniques. The results of processing can be converted

back to analog form for interpretation. Because of these conversions, the processing time increases and the system becomes more complex. In most cases, these disadvantages are outweighed by numerous advantages of digital techniques. However, there are situations where using only analog techniques is simpler and more economical. Both the analog and digital techniques can be employed in the same system to advantage. Such systems are called *hybrid systems.* But the tendency today is towards employing digital systems because the economic benefits of integration are of overriding importance.

8.1.3 Logic Levels

Digital systems use the binary number system. Therefore, two-state devices are used to represent the two binary digits 1 and 0 by two different voltage levels, called HIGH and LOW. If the HIGH voltage level is used to represent 1 and the LOW voltage level is used to represent 0, the system is called the *positive logic system.* On the other hand, if the HIGH voltage level represents 0 and the LOW voltage level represents 1, the system is called the *negative logic system.*

Normally, the binary 0 and 1 are represented by the logic voltage levels 0 V and + 5 V. So, in a positive logic system, 1 is represented by + 5 V (HIGH) and 0 is represented by 0 V (LOW); and in a negative logic system, 0 is represented by + 5 V (HIGH) and 1 is represented by 0 V (LOW). Both positive and negative logics are used in digital systems, but the positive logic is more common.

8.2 BOOLEAN ALGEBRA

Boolean algebra is a kind of logical mathematics developed by George Boole in the late 1830s. It resembles the algebra of real numbers but the basic numeric operations of multiplication, addition, and negation are replaced by basic logical operations of **conjunction, disjunction, and complement** and are also called OR operation, AND operation and NOT operation respectively. These basic local operators are used to represent and reduce all mathematics of logical expressions in Boolean algebra. Boolean algebra is also known as '**Laws of Thoughts**' which codified several rules of relationship between mathematical quantities limited to one of two possible values : **true or false, 1 or 0**.

8.2.1 Boolean Arithmetic

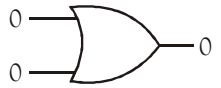
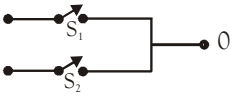
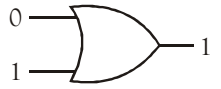
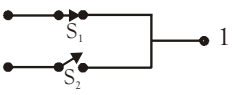
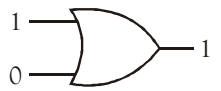
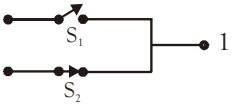
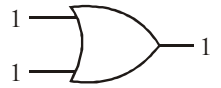
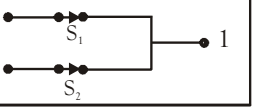
All arithmetic operations performed with Boolean quantities gives one of two possible outcomes : either 1 or 0. The Boolean arithmetic using OR, AND, and NOT logical operations are discussed below :

OR Logical Operation:

The Boolean arithmetic using OR logical operation is given below and is called Truth Table of OR logical operation. The equivalent logical symbol is also given.

0	+	0	=	0
0	+	1	=	1
1	+	0	=	1
1	+	1	=	1

Truth Table of OR logical operation

OR Operation	OR gate equivalent Symbol	Parallel switch equivalent
0 + 0 = 0		
0 + 1 = 1		
1 + 0 = 1		
1 + 1 = 1		

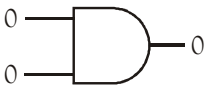
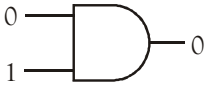
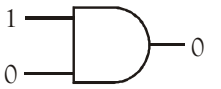
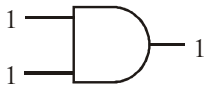
Boolean addition is equivalent to the OR logic operation as well as parallel switch contacts.

AND Logical Operation:

The Boolean arithmetic using AND logical operation is given below and is called Truth Table of AND logical operation. The equivalent logical symbol is also given.

0 . 0 = 0
0 . 1 = 0
1 . 0 = 0
1 . 1 = 1

Truth Table of AND logical operation

AND Operation	AND gate equivalent Symbol	Series switch equivalent
0 . 0 = 0		
0 . 1 = 0		
1 . 0 = 0		
1 . 1 = 1		

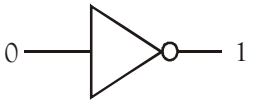
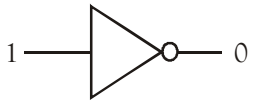
Boolean multiplication is equivalent to the AND logic operation as well as series switch contacts.

NOT Logical Operation:

The Boolean arithmetic using NOT logical operation is given below and is called Truth Table of NOT logical operation. The equivalent logical symbol is also given.

$\overline{0} = 1$
$\overline{1} = 0$

Truth Table of NOT logical operation

NOT Operation	NOT gate equivalent Symbol
$\overline{0} = 1$	
$\overline{1} = 0$	

Boolean complementation is equivalent to the NOT logic operation. In NOT operation, output is always complement of the input and hence it is called complement operation.

8.2.2 Boolean Identities

In mathematics, an identity is a statement which is true for all possible values of its variable. The algebraic identity A + 0 = A tells us that anything (A) added to zero equals the original anything, no matter what value that anything may be. Accordingly we can write basic Boolean Identities as follows :

Basic Boolean Algebraic Identities

Additive	Multiplicative
A + 0 = A	0 . A = 0
A + 1 = 1	1 . A = A
A + A = A	A . A = A
A + $\overline{A}$ = 1	A . $\overline{A}$ = 0

The basic Boolean identities, their symbolic representation are shown below:

Table 8.1 Boolean algebraic identities of additive type

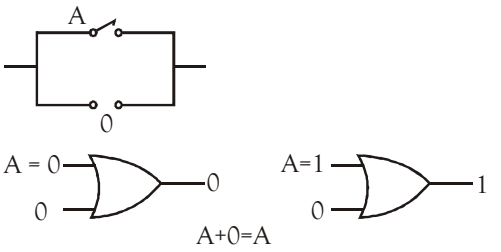
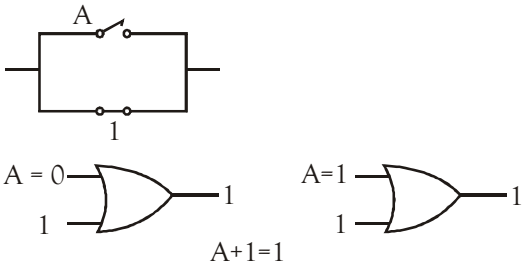
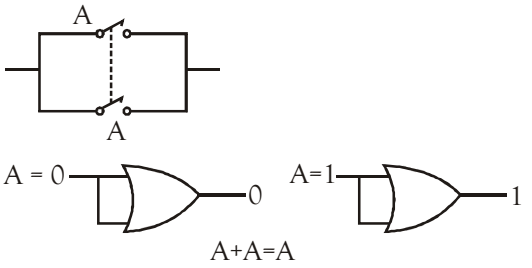
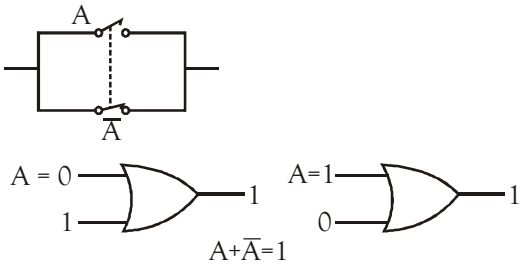
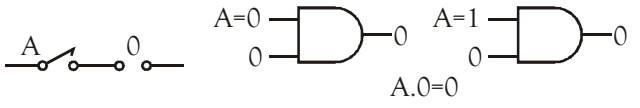
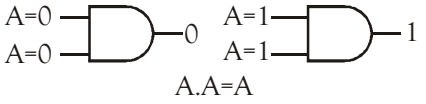
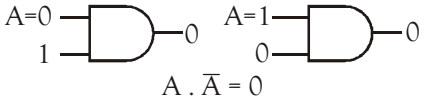
Identity	Logic Symbol Equivalent
A + 0 = A	
A + 1 = 1	
A + A = A	
A + $\overline{A}$ = 1	

Table 8.2 Boolean algebraic identities of multiplicative type

Identity	Logic Symbol Equivalent
A . 0 = 0	
A . 1 = A	
A . A = A	
A . $\overline{A}$ = 0	

8.2.3 Properties of Boolean Algebra

Another type of mathematical identity called "Property" or "Law" describes how different variables relate to each other in a system of numbers. These properties are mostly applicable equally to addition and multiplication. The properties applicable to Boolean Algebra are given below :

1. **Associative Law**

   (A.B).C = A.(B.C) = A.B.C

   (A + B) + C = A + (B + C) = A + B + C

2. **Commutative Law**

   A . B = B . A

   A + B = B + A

3. **Distributive Law**

   A.(B+C) = (A.B) + (A.C)

   A+(B.C) = (A+B) . (A+C)

4. **Precedence**

   AB = A.B

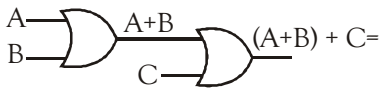
   A.B+C = (A.B) + C

   A+B.C = A + (B.C)

The combinational symbolic equivalent of Associative property of Addition and Multiplication are shown in following Tables:

Table 8.3 Associative property for addition : A + (B + C) = (A + B) + C

Symbolic Equivalent



A	B	C	A+B	(A+B)+C
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

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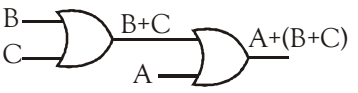


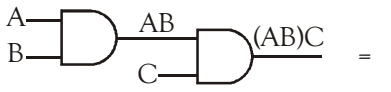
A	B	C	B+C	A+(B+C)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

This law can be extended to any number of variables. For example,

A + (B + C + D) = (A + B + C) + D = (A + B) + (C + D).

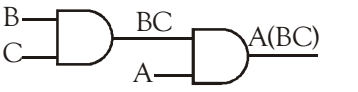
Table 8.4 Associative property for multiplication : A . (B . C) = (A . B) . C

Symbolic Equivalent



A	B	C	AB	(AB)C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

=



A	B	C	BC	A(BC)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

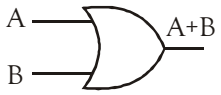
This law can be extended to any number of variables. For example,

A(BCD) = (ABC)D = (AB) (CD)

The combinational symbolic equivalent of Commutative property of Addition and Multiplication are shown in following Tables:

Table 8.5 Commutative property for addition : A + B = B + A

Symbolic Equivalent



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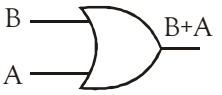


A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

=

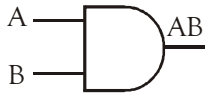
B	A	B+A
0	0	0
0	1	1
1	0	1
1	1	1

This law can be extended to any number of variables. For example,

A+B+C = B+C+A = C+A+B = B + A + C

Table 8.6 Commutative property for multiplication : A . B = B . A

Symbolic Equivalent



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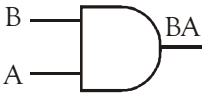


A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

=

B	A	B.A
0	0	0
0	1	0
1	0	0
1	1	1

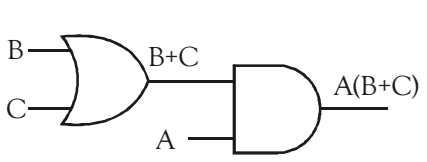
This law can be extended to any number of variables. For example,

A.B.C = B.C.A= C.A.B = B.A.C

The combinational symbolic equivalent of Distributive property of Addition and Multiplication are shown in following Tables:

Table 8.7 Distributive property for addition : A (B + C) = AB + AC

Symbolic Equivalent



A	B	C	A+B	A(B+C)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

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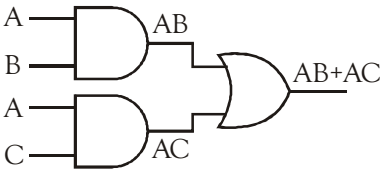


A	B	C	AB	AC	AB+AC
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

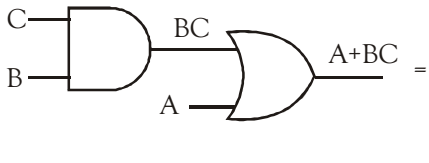
This law applies to single variables as well as combinations of variables. For example,

ABC(D + E) = ABCD + ABCE

AB(CD + EF) = ABCD + ABEF

Table 8.8 Distributive property for multiplication: A + (B . C) = (A + B) . (A + C)

Symbolic Equivalent



A	B	C	BC	A+BC
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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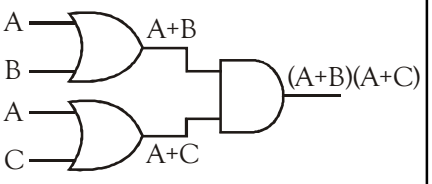


A	B	C	A+B	A+C	(A+B)(A+C)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

8.2.4 Boolean Rules for Simplification

The following rules are used for simplification of Boolean expressions:

(1) $A + AB = A$ ..(8.1)

Proof:

$A + AB = A(1 + B) = A(1) = A$

(2) $A(A + B) = A$ ...(8.2)

Proof:

$A(A + B) = AA + AB = A + AB = A(1 + B) = A.\ 1 = A$

(3) $A + \overline{A}B = A + B$ ...(8.3)

Proof:

$A + \overline{A}B = A + AB + \overline{A}B = A + B(A + \overline{A}) = A + B(1) = A + B$

(4) $(A + B)(A + C) = A + BC$ ...(8.4)

Proof:

$(A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC = A + AB + BC = A + BC$

Example 1: Using Boolean algebra and simplification rules simplify following expressions:

(i) $AB + BC(B + C)$

↓ Distributing terms

$AB + BBC + BCC$

↓ Using identity $AA = A$

$AB + BC + BC$

↓ Using identity $A + A = A$

$AB + BC$

↓ Factoring B out of terms

$(A + C)B$

(ii) $A + B(A + C) + AC$

↓ Distributing terms

$A + AB + BC + AC$

↓ Using rule $A + AB = A$

$A + BC + AC$

↓ Using rule $A + AB = A$

$A + BC$

Example 2: Prove the Boolean identity : (A + B)(A + C) = A + BC

$Y = (A + B)(A + C)$

$= AA + AC + AB + BC$

$= A + AC + AB + BC$

$= A + AB + AC + BC = A(1 + B) + AC + BC$

$= A + AC + BC$

$= A(1 + C) + BC = A + BC$

$\therefore \quad (A + B)(A + C) = A + BC$

Example 3: Prove the Boolean identity : $A + \overline{A}B = A + B$

$Y = A + \overline{A}B = A.1 + \overline{A}B$

$= A(1 + B) + \overline{A}B$

$= A.1 + AB + \overline{A}B$

$= A + BA + B\overline{A}$

$= A + B(A + \overline{A})$

$= A + B.1$

$= A + B$

$\therefore \quad \mathbf{A + \hat{A}B = A + B}$

8.2.5 De-Morgan's Theorems

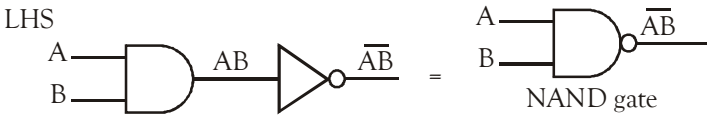
A mathematician named De-Morgan developed two important rules related to the group complementation in Boolean Algebra.

De-Morgan's Theorem 1 : $\overline{A \cdot B} = \overline{A} + \overline{B}$ **(NAND function)** **...(8.5)**

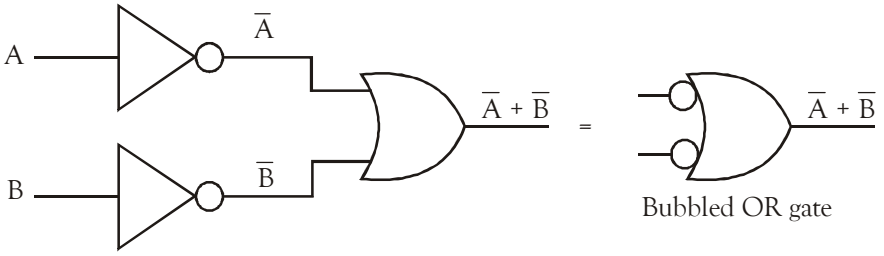
De-Morgan's Theorem 2 : $\overline{A + B} = \overline{A} \cdot \overline{B}$ **(NOR function)** **...(8.6)**

De-Morgan's theorems can be used to break long bars in Boolean expressions. While breaking a long bar, the operation directly under the break changes from addition to multiplication or vice-versa and broken bar pieces remain over individual variables.

(i) Proof of De-Morgan's Theorem 1: $\overline{A \cdot B} = \overline{A} + \overline{B}$ **:**



RHS



A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

=

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

It shows that the NAND gate is equivalent to a bubbled OR gate.

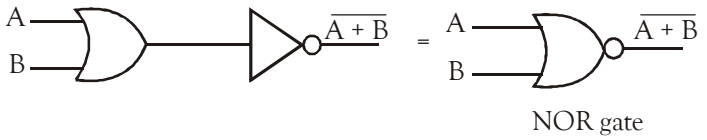
This law can be extended to any number of variables or combinations of variables. For example,

$$\overline{ABCD\ldots} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \ldots$$

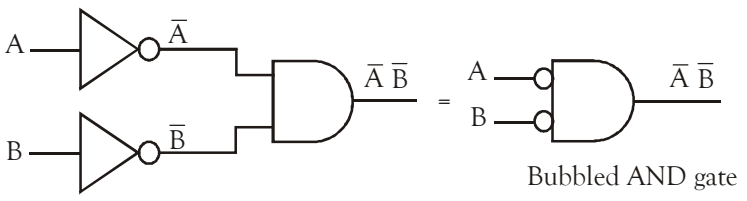
$$\overline{(AB)\,(CD)\,(EFG)\ldots} = \overline{AB} + \overline{CD} + \overline{(EFG)} + \ldots$$

(ii) Proof of De-Morgan's Theorem 2 : $\overline{(A+B)} = \overline{A}.\overline{B}$:

LHS



RHS



A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

=

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

This law can be extended to any number of variables or combinations of variables. For example,

$$\overline{A + B + C + D + \ldots} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\ \ldots$$

$$\overline{AB + CD + EFG + \ldots} = \overline{AB}\ \overline{CD}\ \overline{EFG}\ \ldots$$

Example 4: Simplifications of Boolean expressions using De-Morgan's Theorem

(i) $\overline{A + \overline{B.C}}$ **Method I**

↓ Breaking longest bar (Addition changes Multiplication)

$\overline{A}.\ \overline{\overline{B.C}}$

↓ Applying identity $\overline{\overline{A}} = A$

$\overline{A}.\ BC$

(ii) $\overline{A + \overline{BC}}$ **Method II**

↓ Breaking shortest bar first (Multiplication changes to Addition)

$\overline{A + (\overline{B} + \overline{C})}$

↓ Breaking bar in two place

$\overline{A}.\ \overline{\overline{B}}.\ \overline{\overline{C}}$

↓ Applying $\overline{\overline{A}} = A$

$\overline{A}.\ B.\ C$

(iii) $\overline{AB + CD}$

↓ Breaking bar in the middle

$\overline{AB}.\ \overline{CD}$

↓ Breaking both bars in the middle

$\overline{A} + \overline{B}\,.\,\overline{C} + \overline{D}$

(iv) $\overline{\overline{A + BC} + \overline{A\overline{B}}}$

$\downarrow$ Breaking largest bar

$\overline{\overline{A + BC}} \cdot \overline{\overline{A\overline{B}}}$

$\downarrow$ Using identity $\overline{\overline{A}} = A$

$(A + BC)(A\overline{B})$

$\downarrow$ Using distributive property

$AA\overline{B} + BCA\overline{B}$

$\downarrow$ Using identity $AA = A$ & $A\overline{A} = 0$

$A\overline{B} + 0$

$\downarrow$ Using identity $A + 0 = A$

$A\overline{B}$

(v) Apply De-morgan's theorem to the expression

$$\overline{\overline{AB}\left(CD + \overline{E}F\right)\left(\overline{AB} + \overline{CD}\right)}$$

Solution:

The given expression is

$$= \overline{\overline{AB}\left(CD + \overline{E}F\right)\left(\overline{AB} + \overline{CD}\right)}$$

$$= \overline{\overline{AB}} + \overline{CD + \overline{E}F} + \left(\overline{\overline{AB} + \overline{CD}}\right)$$

$$= AB + \left(\overline{CD} \cdot \overline{\overline{E}F}\right) + \left(\overline{\overline{AB}} \cdot \overline{\overline{CD}}\right)$$

$$= AB + \left(\overline{C} + \overline{D}\right)\left(E + \overline{F}\right) + ABCD$$

Example 5: Reduce the expression

$$A + B[AC + (B + \overline{C})D]$$

Solution:

$$A + B[AC + (B + \overline{C})D]$$

$$= A + B(AC + BD + \overline{C}D)$$

$$= A + BAC + BBD + B\overline{C}D$$

$$= A + ABC + BD + BD\overline{C}$$

$= A(1 + BC) + BD(1 + \overline{C})$

$= A \cdot 1 + BD \cdot 1$

$= A + BD$

8.3 LOGIC GATES

A 'gate' is defined as a multi-input (≥ 2) hardware device that has a two-level output. The output level (1 or H/0 or L) of the gate is a strict and repeatable function of the two-level (1 or H/0 or L) combinations applied to its inputs. Fig. 8.2 shows a general model of a gate. The term "logic" is usually used to refer to a decision making process. A logic gate, then, is a circuit that can decide to say yes or no at the output based upon inputs.

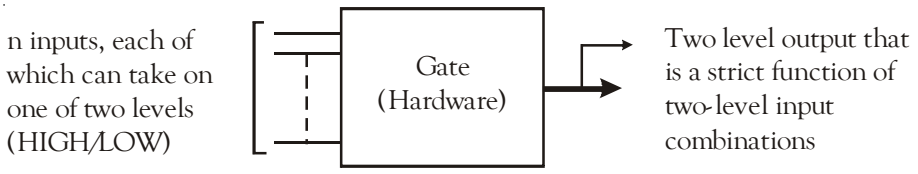


Figure 8.2 *The general model of a gate*

8.3.1 OR Gate

The OR gate is sometimes called the "any or all gate". To show the OR gate we use the logical symbol in Fig. 8.3.

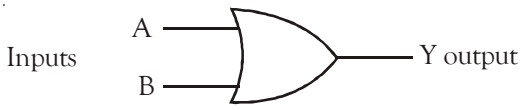
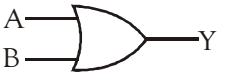


Figure 8.3 *Logic symbol of OR gate*

Boolean Expression	OR Symbol ↑ A + B = Y
Logic Symbol	
Truth Table	

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

OR gate using Diodes:

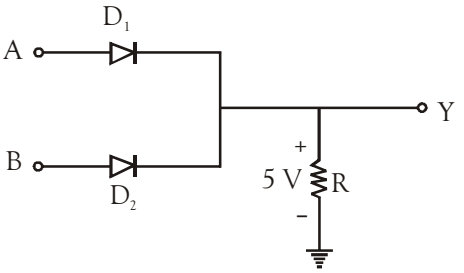


Figure 8.4 *OR gate using diodes*

OR gate using Diodes is shown in Fig. 8.4. The circuit consisting of two ideal diodes D_1 and D_2 connected in parallel across the output Y.

1. When A is at +5 V, D_1 is forward-biased and hence conducts. The circuit current flows via R dropping 5 V across it. In this way, point Y achieves potential of +5 V.
2. When + 5 V is applied to B, D_2 conducts causing point Y to go to +5 V.
3. When both A and B are +5 V, the drop across R is 5 V because voltages of A and B are in parallel. Again, point Y is driven to +5 V.
4. When there is no voltage either at *A* or *B*, output Y remains 0.

8.3.2 AND Gate

The AND gate is also called the "all or nothing gate". To show the AND gate we use the logic symbol in Fig. 8.5. This is the standard symbol to memorize and used for AND gates.

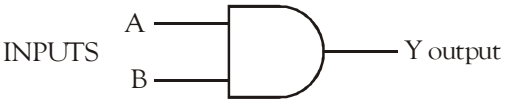
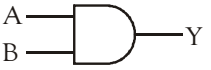
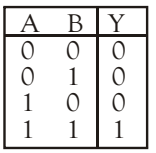


Figure 8.5 *Logic symbol of AND gate*

Boolean Expression	AND Symbol ↑ A . B = Y
Logic Symbol	
Truth Table	

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND gate using Diodes:

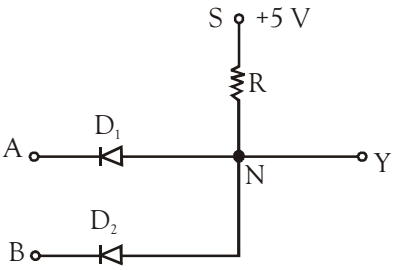


Figure 8.6 *AND gate using diodes*

AND gate using Diodes is shown in Fig. 8.6. The circuit functions as explained below:

1. When A is at 0 V, diode D_1 conducts and the supply voltage of +5 V drops across R. Consequently, point N and hence point Y is driven to 0 V. Therefore, the output Y is 0.
2. Similarly, when B is at 0 V_1 D_2 conducts thereby driving N and hence Y to ground.
3. When both A and B are at 0 V, both diodes conduct and, again, the output Y is 0.
4. When both A and B are at +5 V, there is no supply current through the diodes and hence no voltage drop across R and hence the output Y goes to supply voltage of +5 V.

8.3.3 NOT Gate

The NOT circuit performs the basic logical function called inversion or complementation. That is why, it is also known as Inverter. The NOT circuit has only one input and one ouput. The purpose of this gate is to give an output that is not the same as the input. When a HIGH level is applied to an inverter, a LOW level appears at its output and vice versa. The logic symbol for the inverter is shown in Fig. 8.7.

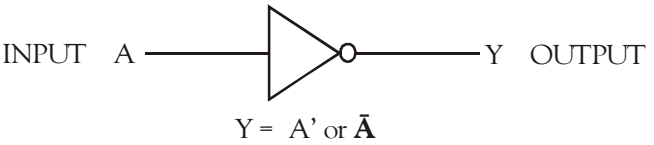
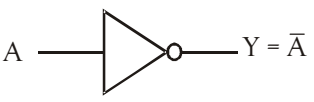


Figure 8.7 *Logic symbol of NOT gate*



Input A	Output Y
0	1
1	0

SYMBOL | TRUTH TABLE

NOT gate using Transistor:

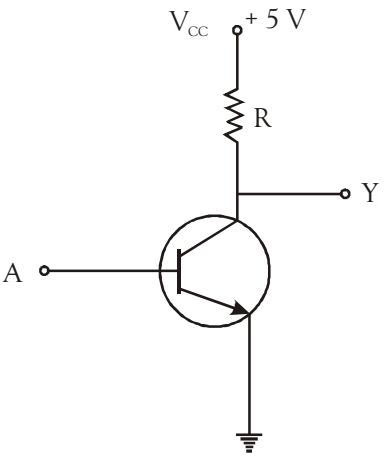


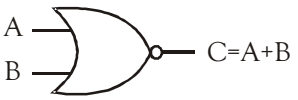
Figure 8.8 *NOT gate using transistor*

The circuit functions as explained below:

1. When +5 V is applied to A, the transistor will be fully turned ON, drawing maximum collector current. Hence, entire of V_{CC} = 5 V will drop across R thereby sending Y to 0 V.
2. With 0 V applied at A, the transistor will be cut OFF and the output Y, therefore, will go to V_{CC} i.e., +5 V. Obviously, in each case, output is the opposite of input.

8.3.4 NOR Gate

This is an OR gate with the output inverted, as shown by the 'o' (bubble) on the output. The output C is true if NOT inputs A OR B are true: C = NOT (A OR B). A NOR gate can have two or more inputs, its output is true if no inputs are true.



Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	0

SYMBOL | TRUTH TABLE

NOR gate using Transistors:

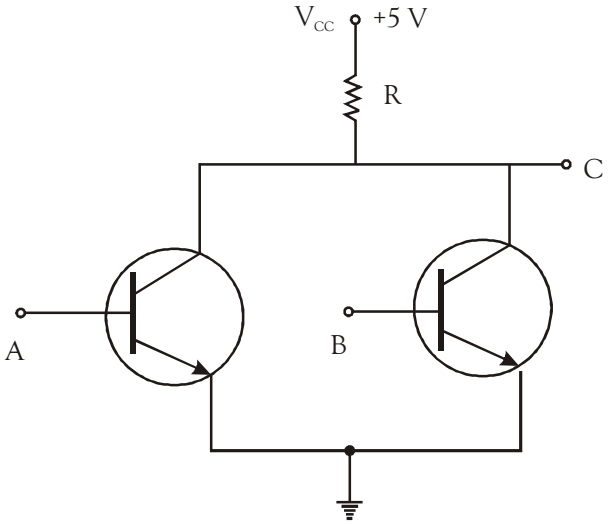
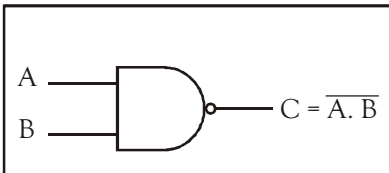


Figure 8.9 *NOR gate using transistors*

The transistor equivalent of the NOR gate is shown in Fig. 8.9. As seen, output C is 1 only when both transistors are cut-off *i.e.*, when *A* = 0 and *B* = 0. For any other input condition like 01, 10 and 11, one or both transistors saturate forcing point C to go to 0 or ground.

8.3.5 NAND Gate

This is an AND gate with the output inverted, as shown by the 'o' on the output. The output is true if input A AND input B are NOT both true: **C = NOT (A AND B)**. A NAND gate can have two or more inputs, its output is true if NOT all inputs are true.



Input A	Input B	Output C
0	0	1
0	1	1
1	0	1
1	1	0

SYMBOL | TRUTH TABLE

NAND gate using Transistors:

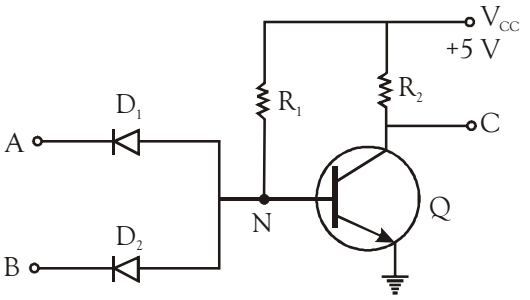


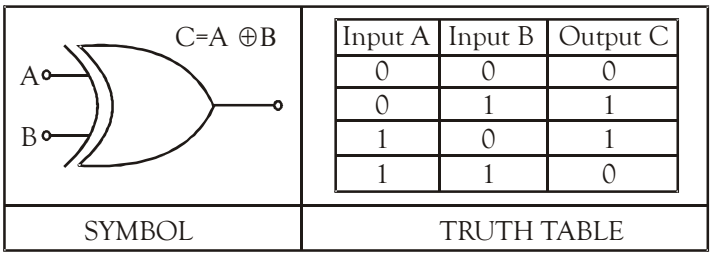
Figure 8.10 *NAND gate using diodes & transistors*

The diode-transistor equivalent of a NAND gate is shown in Fig. 8.10. It is seen that point N would be driven to ground when either D_1 or D_2 or both D_1 and D_2 conduct. It represents input conditions of 10, 01 and 11. Under such conditions, point C is cut-off and hence C goes to V_{CC} meaning logic 1 state. When A = 1 and B = 1 (i.e., input voltages at A and B are +5 V), the point N is +5 V and C is saturated and hence output becomes logic 0 state.

8.3.6 XOR Gate

The output C is true if either input A is true OR input B is true, **but not when both of them are true**: **C = (A AND NOT B) OR (B AND NOT A)**.

This is like an OR gate but excluding both inputs being true. The output is true if inputs A and B are **DIFFERENT**. EX-OR gates can only have 2 inputs. Logic circuit of XOR gate is shown in Fig. 8.11.



Input A	Input B	Output C
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE

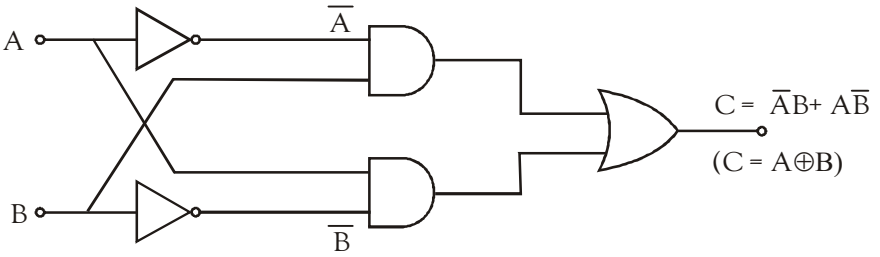
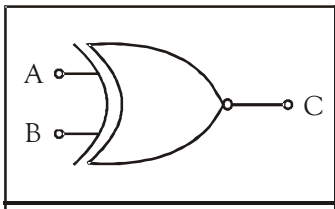


Figure 8.11 *Logic circuit connection of exclusive OR gate (XOR)*

8.3.7 XNOR Gate

The following symbol shows an X-OR gate with the output inverted, as shown by the 'o' on the output. The output C is true if inputs A and B are the **SAME** (both true or both false): **C = (A AND B) OR (NOT A AND NOT B)**. X-NOR gates can only have 2 inputs.



Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	1

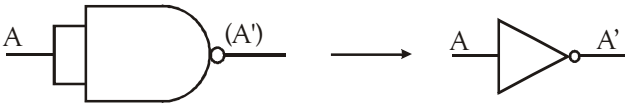
SYMBOL | TRUTH TABLE

8.3.8 Universal Gate

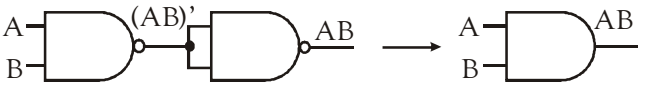
A logic gate is called **universal logic gate** if it can be used (either alone or combination of itself) to realize all basic logic operations like OR, AND and NOT operations. NAND gate and NOR gate are universal logic gates.

(1) NAND gate as Universal Gate:

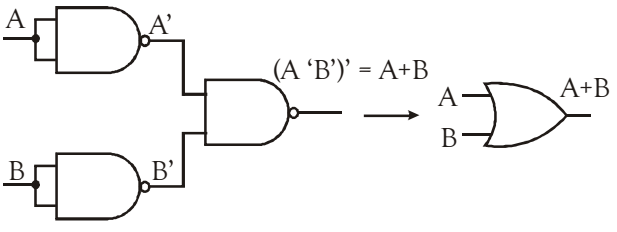
(a) NOT gate using NAND gate:



(b) AND gate using NAND gate:

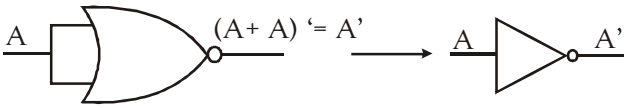


(c) OR gate using NAND gate:

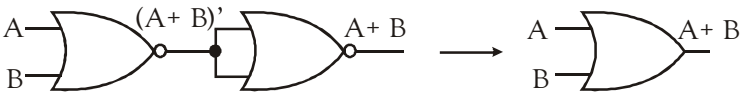


(2) **NOR gate as Universal Gate:**

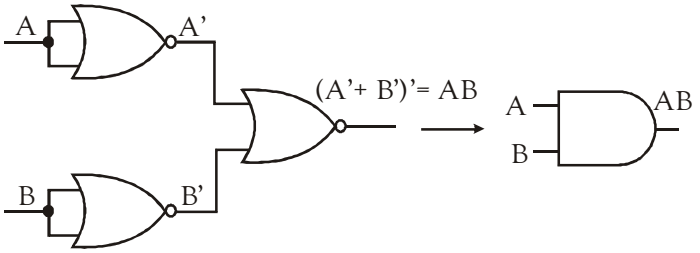
(a) NOT gate using NOR gate:



(b) AND gate using NOR gate:



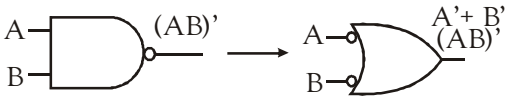
(c) OR gate using NOR gate:



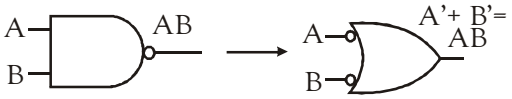
8.3.9 Equivalent Gate

By means of complimenting inputs or outputs using bubbles (NOT gates), we can demonstrate equivalence gates as shown below :

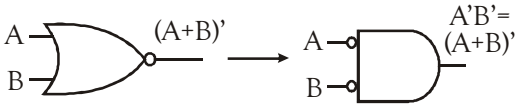
(i) NAND Gate:



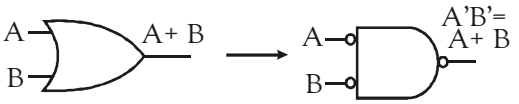
(ii) AND Gate:



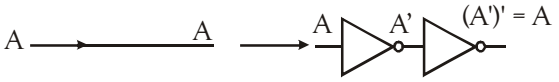
(iii) NOR Gate:



(iv) OR Gate:



(v) Complement of NOT Gate:



8.4 BINARY ADDERS

The digital system consists of two types of circuits, namely

(*i*) Combinational circuits and

(*ii*) Sequential circuits

A combinational circuit consists of logic gates, where outputs at any instant and are determined only by the present combination of inputs without regard to previous inputs or previous state of outputs. A combinational circuit performs a specific information-processing operation assigned logically by a set of Boolean functions. Sequential circuits contain logic gates as well as memory cells. Their outputs depend on the present inputs and also on the states of memory elements. Since the outputs of sequential circuits depend not only on the present inputs but also on past inputs, the circuit behavior must be specified by a time sequence of inputs and memory states.

8.4.1 Half-Adder

A *half-adder* is an arithmetic circuit block that can be used to add two bits. Such a circuit thus has two inputs that represent the two bits to be added and two outputs, with one producing the SUM (S) output and the other producing the CARRY (C). Fig. 8.12 shows the truth table of a half-adder, showing all possible input combinations and the corresponding outputs.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

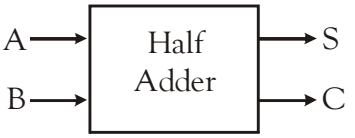


Figure 8.12 *Truth table of a half-adder*

The Boolean expressions for the SUM and CARRY outputs are given by the equations

$$\text{SUM } S = A.\overline{B} + \overline{A}.B$$

$$\text{CARRY } C = A.B$$

An examination of the two expressions tells that there is no scope for further simplification. While the first one representing the SUM output is that of an EX-OR gate, the second one representing the CARRY output is that of an AND gate. The simplest way to construct a half-adder would be to use a two-input EX-OR gate for the SUM output and a two-input AND gate for the CARRY output, as shown in Fig. 8.13. Half-adder can also be implemented by using an appropriate arrangement of either NAND or NOR gates.

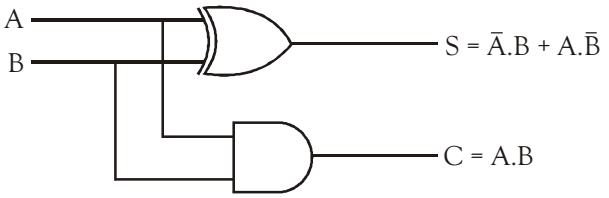


Figure 8.13 *Logic implementation of a half-adder*

(1) Half Adder using NAND gates:

Figure 8.14 (a) shows the implementation of a half-adder with NAND gates only. A close look at the logic diagram of Fig. 8.14 (a) reveals that one part of the circuit implements a two-input EX-OR gate with two-input NAND gates. The AND gate required to generate CARRY output is implemented by complementing an already available NAND output of the input variables.

$$S = A\overline{B} + \overline{A}B = A\overline{B} + A\overline{A} + \overline{A}B + B\overline{B}$$

$$= A(\overline{A} + \overline{B}) + B(\overline{A} + \overline{B})$$

$$= A \,.\, \overline{AB} + B \,.\, \overline{AB}$$

$$= \overline{\overline{A \,.\, \overline{AB}} \,.\, \overline{B \,.\, \overline{AB}}}$$

$$C = AB = \overline{\overline{AB}}$$

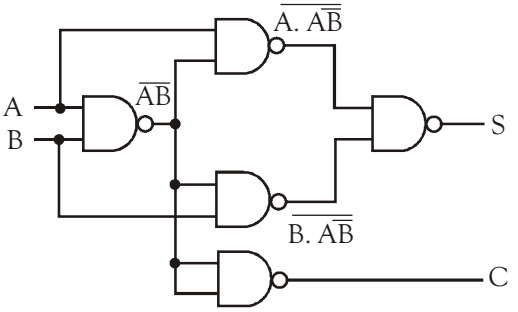


Figure 8.14 ***(a)*** *Half-adder implementation using NAND gates*

(2) Half Adder using NOR gates:

Figure 8.14 (b) shows the implementation of a half-adder with NOR gates only.

$$S = A\overline{B} + \overline{A}B = A\overline{B} + A\overline{A} + \overline{A}B + B\overline{B}$$

$$= A(\overline{A} + \overline{B}) + B(\overline{A} + \overline{B})$$

$$= (A + B)(\overline{A} + \overline{B})$$

$$= \overline{\overline{A + B} + \overline{\overline{A} \cdot \overline{B}}}$$

$$C = AB = \overline{\overline{AB}} = \overline{\overline{A} + \overline{B}}$$

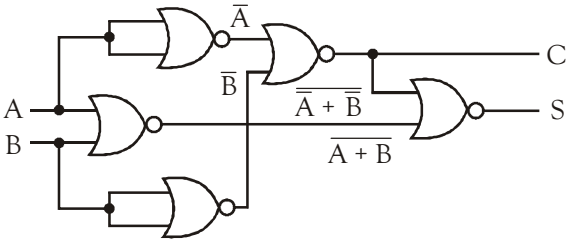
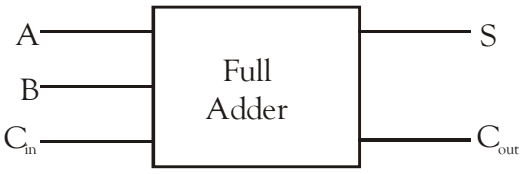


Figure 8.14 (b) *Half-adder implementation using NOR gates*

8.4.2 Full-Adder

A *full adder* circuit is an arithmetic circuit block that can be used to add three bits to produce a SUM and a CARRY output. Such a building block becomes a necessity when it comes to adding binary numbers with a large number of bits. The full adder circuit overcomes the limitation of the half-adder, which can be used to add two bits only. Let us recall the procedure for adding larger binary numbers. We begin with the addition of LSBs of the two numbers. We record the sum under the LSB column and take the carry, if any, forward to the next higher column bits. As a result, when we add the next adjacent higher column bits, we would be required to add three bits if there were a carry from the previous addition. We have a similar situation for the other higher column bits also until we reach the MSB. A full adder is therefore essential for the hardware implementation of an adder circuit capable of adding larger binary numbers. A half-adder can be used for addition of LSBs only.



A	B	C_{in}	SUM(S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 8.15 *Truth table of a full adder*

Figure 8.15 shows the truth table of a full adder circuit showing all possible input combinations and corresponding outputs. In order to arrive at the logic circuit for hardware implementation of a full adder, we will firstly write the Boolean expressions for the two output variables, that is, the SUM and CARRY outputs, in terms of input variables. The full adder circuit using two half adders is shown in Fig. 8.16. The Boolean expressions for the two output variables are given in Eqn. (8.7) for the SUM output (S) and in Eqn. (8.8) for the CARRY output (C_{out}):

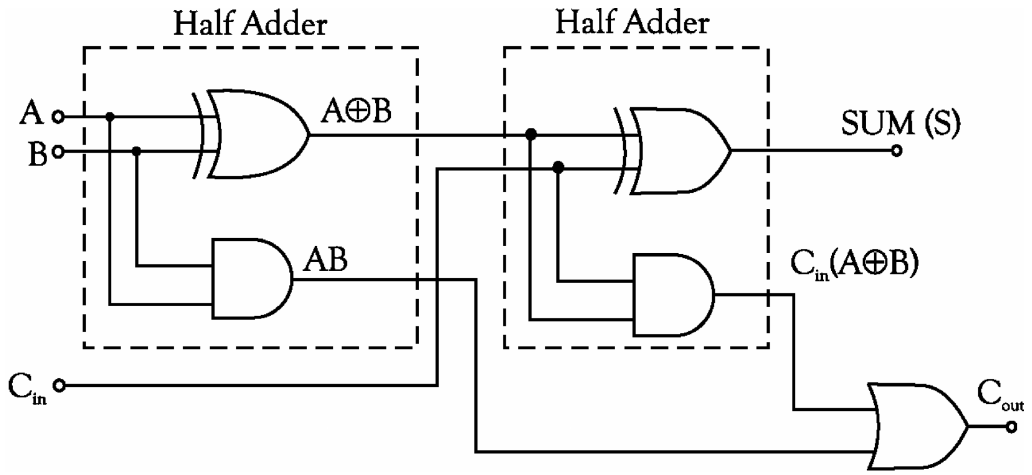


Figure 8.16 *Full adder using two half adders*

$$\text{SUM (S)} = C_{in} \oplus (A \oplus B)$$

$$= C_{in} \oplus \left(A\overline{B} + \overline{A}B\right)$$

$$= C_{in} \left(\overline{A\overline{B} + \overline{A}B}\right) + \overline{C_{in}} \left(A\overline{B} + \overline{A}B\right)$$

$$= C_{in}\ \overline{A\overline{B}} . \left(\overline{\overline{A}B}\right) + \overline{C_{in}} \left(A\overline{B} + \overline{A}B\right)$$

$$= C_{in} \left[\left(\overline{A} + \overline{\overline{B}}\right) . \left(\overline{\overline{A}} + \overline{B}\right)\right] + \overline{C_{in}} \left(A\overline{B} + \overline{A}B\right)$$

$$= C_{in} \left[\left(\overline{A} + B\right) . \left(A + \overline{B}\right)\right] + \overline{C_{in}} \left(A\overline{B} + \overline{A}B\right)$$

$$= C_{in} \left(\overline{A}\overline{B} + AB\right) + \overline{C_{in}} \left(A\overline{B} + \overline{A}B\right)$$

$$= \overline{A}\,\overline{B}C_{in} + ABC_{in} + A\overline{B}\,\overline{C_{in}} + \overline{A}\,B\,\overline{C_{in}} \qquad \text{...(8.7)}$$

The output of the OR gate is given by:

$$C_{out} = AB + C_{in} (A \oplus B)$$

$$= AB + C_{in} \left(A\overline{B} + \overline{A}B\right)$$

$$= AB + A\overline{B}C_{in} + \overline{A}BC_{in}$$

$$= AB + (C_{in} + 1) + A\overline{B}C_{in} + \overline{A}BC_{in} \quad [\because \ (C_{in} + 1) = 1]$$

$$= ABC_{in} + AB + A\overline{B}C_{in} + \overline{A}BC_{in}$$

$$= AB + AC_{in} + (B + \overline{B}) + \overline{A}BC_{in}$$

$$= AB + AC_{in} + \overline{A}BC_{in}$$

$$= AB(C_{in} + 1) + AC_{in} + \overline{A}BC_{in} \quad [\because \ (C_{in} + 1) = 1]$$

$$= ABC_{in} + AB + AC_{in} + \overline{A}BC_{in}$$

$$= AB + AC_{in} + BC_{in}(A + \overline{A})$$

$$= AB + AC_{in} + BC_{in} \qquad ...(8.8)$$

Using Eqn. (8.7) and Eqn. (8.8), we can redraw the circuit of full adder as shown in Fig. 8.17.

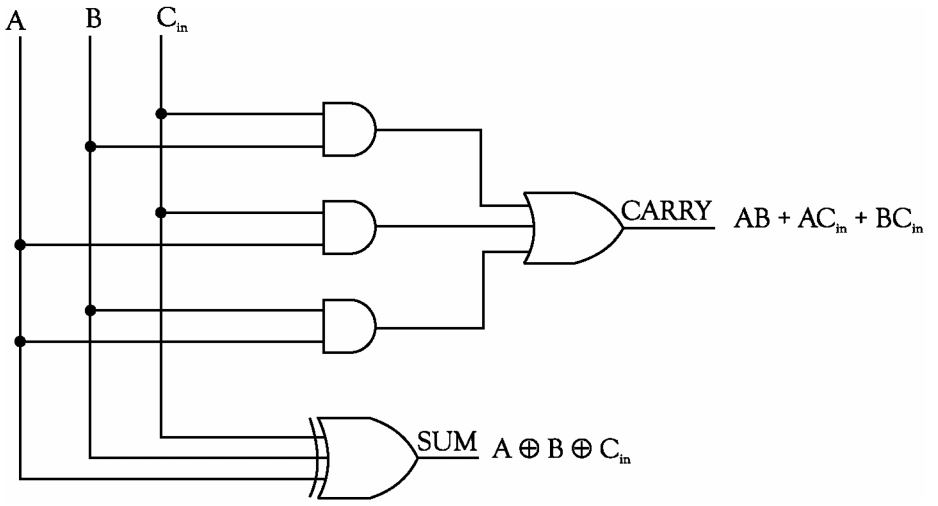


Figure 8.17 *Logic circuit of full adder*

(1) Full Adder using NAND gates:

Let $A \oplus B = \overline{\overline{A} \cdot \overline{AB} \cdot B \cdot \overline{AB}} = X$. Then

$$S = A \oplus B \oplus C_{in} = \overline{\overline{X} \cdot \overline{XC_{in}} \cdot C_{in} \cdot \overline{XC_{in}}} = X \oplus C_{in}$$

$$C_{out} = C_{in}(A \oplus B) + AB = \overline{\overline{C_{in}(A \oplus B)} \cdot \overline{AB}}$$

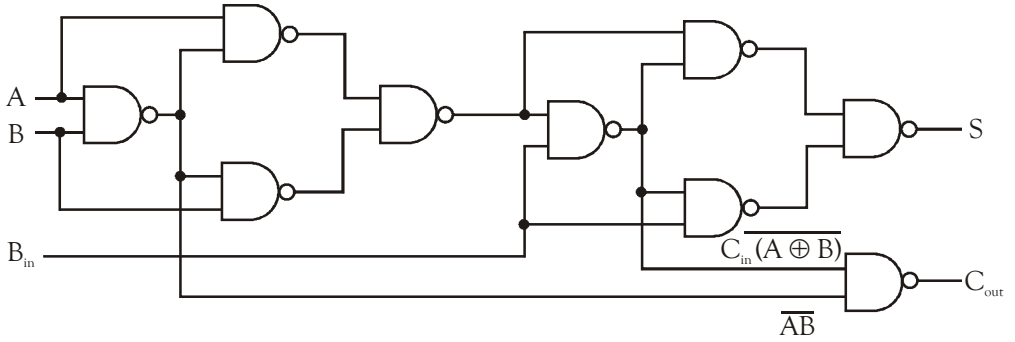


Figure 8.18 *Full adder using NAND gates*

(2) Full Adder using NOR gates:

Let $A \oplus B = X = \overline{(\overline{A + B}) + \overline{\overline{A} + \overline{B}}}$

$$S = A \oplus B \oplus C_{in} = X \oplus C_{in} = \overline{\overline{X + C_{in}} + \overline{\overline{X} + \overline{C_{in}}}}$$

$$C_{out} = AB + C_{in}(A \oplus B) = \overline{\overline{A} + \overline{B}} + \overline{\overline{C_{in}} + \overline{A \oplus B}}$$

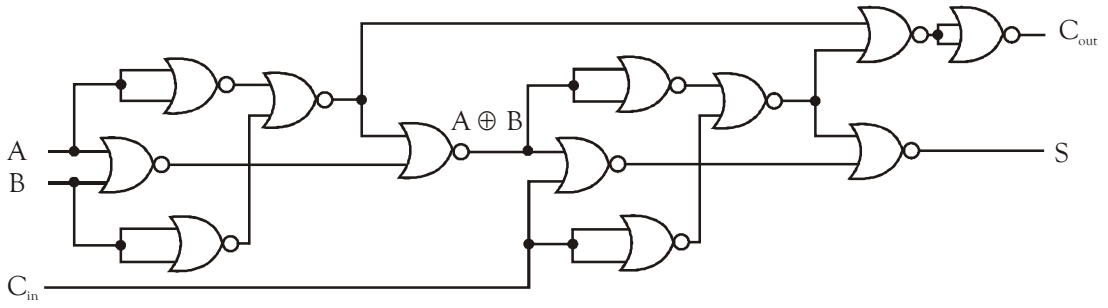


Figure 8.19 *Full adder using NOR gates*

8.4.3 Parallel Binary Adder

The four-bit binary adder called parallel binary adder can be used to add two four-bit binary numbers. Multiple numbers of such adders are used to perform addition operations on larger-bit binary numbers. Each of the adders is composed of four full adders (FAs) connected in cascade. The 4-bit adder using full adder circuit is capable of adding two 4-bit numbers resulting in a 4-bit sum and a carry output as shown in Fig. 8.20 (a). This type of adder is also called a parallel binary adder because all the bits of the augend and addend are present and are fed to the full adder blocks simultaneously. Fig 8.20 (b) shows the logic diagram of a full adder. Here, C_i and C_{i+1} are the input and output CARRY; P_i and G_i are two new binary variables called CARRY PROPAGATE and CARRY GENERATE. For i=1, the diagram in Fig. 8.20 (b) is that of the LSB full adder of Fig. 8.20 (a) with $C_{in} = 0$.

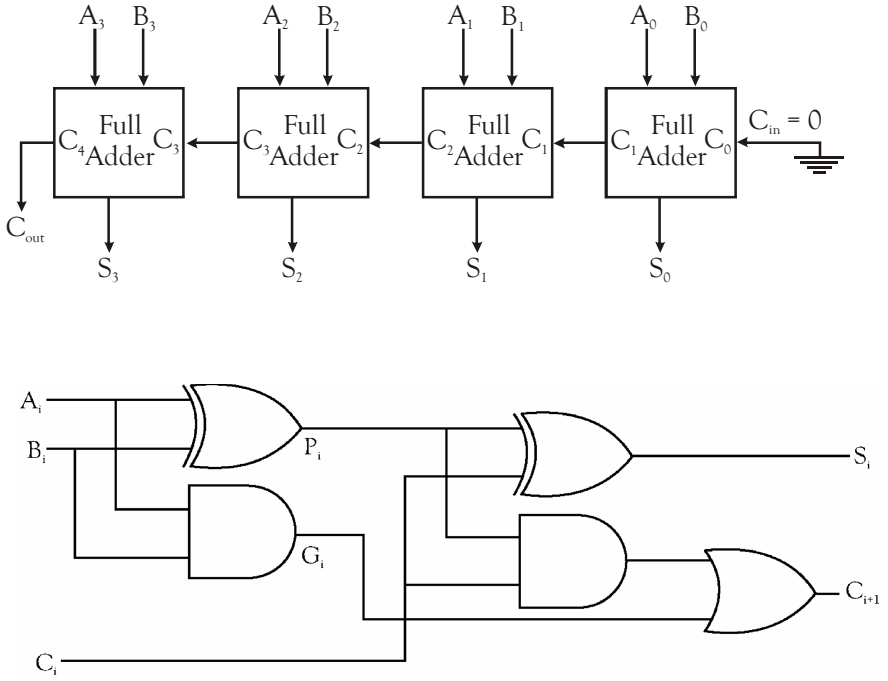


Figure 8.20 *(a) Four-bit binary adder, (b) Logic diagram of each full adder*

To add two n-bit numbers, the parallel method uses n full adder circuits and all bits of addend and augend bits are applied simultaneously. The output carry from one full adder is connected to the input carry of the full adder one position to its left.

The addition operation is illustrated in the following example. Let the 4-bit words to be added be represented by $A_3\ A_2\ A_1\ A_0 = 1\ 0\ 1\ 0$ and $B_3\ B_2\ B_1\ B_0 = 0\ 0\ 1\ 1$.

Subscript i	**3**	**2**	**1**	**0**
Input carry C_i	0	1	0	0
Augend A_i	1	0	1	0
Addend B_i	0	0	1	1
Sum S_i	1	1	0	1
Output carry C_{i+1}	0	0	1	0

← Significant place.

In a 4-bit parallel adder, the input to each full adder will be A_i, B_i and C_i, and the outputs will be S_i and C_{i+1}, where *i* varies from 0 to 3.

In the least significant stage, A_0, B_0 and C_0 (which is 0) are added resulting in sum S_0 and carry C_1. This carry C_1 becomes the carry input to the second stage. Similarly, in the second stage, A, B, and C are added resulting in S_1 and C_2; in the third stage, A_2 B_2 and C_2 are added resulting in S_2 and C_3; in the fourth stage A_3, B_3 and C_3 are added resulting in S_3 and C_4 which is the output carry. Thus the circuit results in a sum (S_3, S_2, S_1, S_0) and a carry output (C_{out}).

Example 6: Add the binary numbers 1001 and 1011 in a parallel binary adder, and show the process by means of a block diagram.

Solution:

$$A_3\ A_2\ A_1\ A_0 = 1\ 0\ 0\ 1$$
$$B_3\ B_2\ B_1\ B_0 = 1\ 0\ 1\ 1$$

(i) A_0, B_0 i.e., 1 and 1 are the inputs to the first full-adder with CARRY 0.

$1 + 1 = 0 = S_0$ and CARRY 1 is generated.

(ii) 0 (A_1) and 1 (B_1) and CARRY 1 are the inputs to the second full adder

$0 + 1 + 1 = 0 = S_1$ and a CARRY 1 is generated.

(iii) 0 (A_2) and 0 (B_2) and CARRY 1 are the inputs to the third full adder

$0 + 0 + 1 = 1 = S_2$ and CARRY 0 is generated

(iv) 1 (A_3) and 1 (B_3) and a CARRY 0 are the inputs to the final full adder.

$1 + 1 + 0 = 0 = S_3$ and a CARRY 1 (S_4) is generated

Hence the final output is

S_4	S_3	S_2	S_1	S_0
1	0	1	0	0

Block diagram for this process is given in Fig. 8.21.

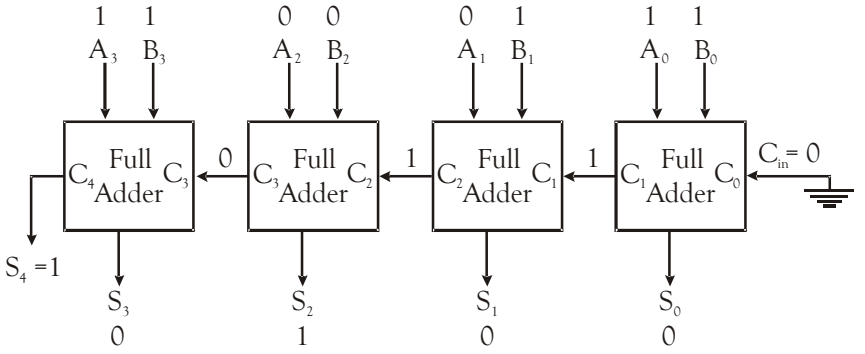


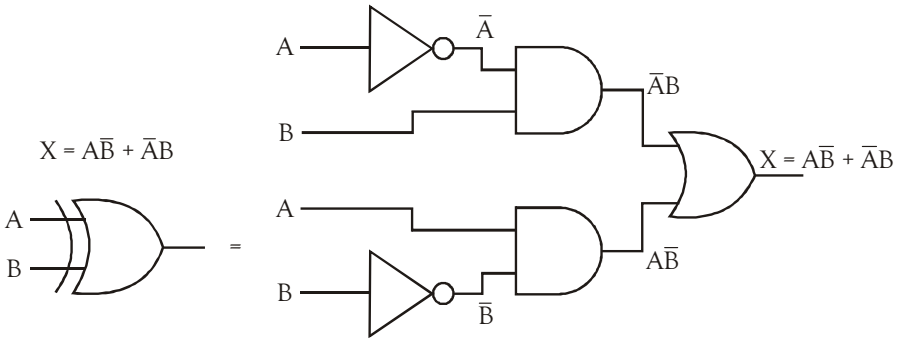
Figure 8.21 *Parallel binary adder for given example*

SOLVED PROBLEMS

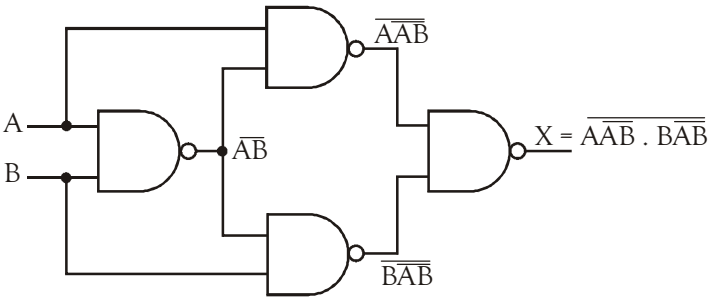
1. *Realize the X-OR function using (a) AOI logic, (b) NAND logic, and (c) NOR logic.*

Solution:

(a) Using AOI logic:



(b) Using NAND logic:



$$X = A\overline{B} + \overline{A}B$$

$$= A\overline{A} + A\overline{B} + \overline{A}B + B\overline{B}$$

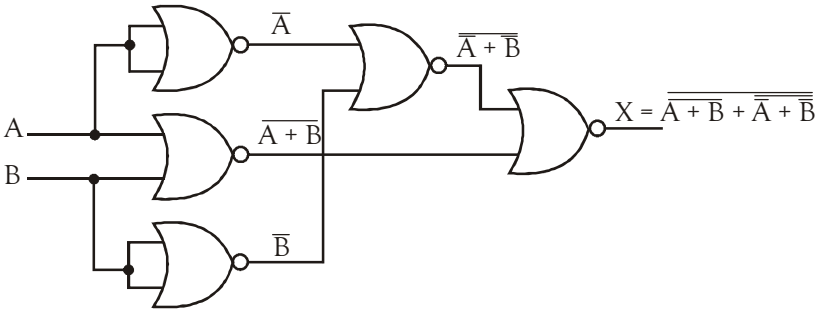
$$= A(\overline{A} + \overline{B}) + B(\overline{A} + \overline{B})$$

$$= A\overline{AB} + B\overline{AB}$$

$$= \overline{A\overline{AB} + B\overline{AB}}$$

$$= \overline{\overline{A\overline{AB}} \cdot \overline{B\overline{AB}}}$$

(c) Using NOR logic:



$$X = A\overline{B} + \overline{A}B$$

$$= A\overline{A} + A\overline{B} + \overline{A}B + B\overline{B}$$

$$= A(\overline{A} + \overline{B}) + B(\overline{A} + \overline{B})$$

$$= (A + B)(\overline{A} + \overline{B})$$

$$= \overline{(A + B)(\overline{A} + \overline{B})}$$

$$= \overline{(\overline{A + B}) + (\overline{\overline{A} + \overline{B}})}$$

2. *Reduce the expression*

$$A[B + \overline{C}(AB + A\overline{C})]$$

Solution:

The given expression is

$$= A\,[B + \overline{C}\,(\overline{AB}\;\overline{A\overline{C}})]$$

$$= A[B + \overline{C}(\overline{A} + \overline{B})\,(\overline{A} + C)]$$

$$= A[B + \overline{C}\,(\overline{A}\,\overline{A} + \overline{A}C + \overline{B}\overline{A} + \overline{B}C)]$$

$$= A(B + \overline{C}\,\overline{A} + \overline{C}\,\overline{A}\,C + \overline{C}\,\overline{B}\,\overline{A} + \overline{C}\,\overline{B}\,C)$$

$$= A(B + \overrightarrow{C}\,\overline{A} + 0 + \overline{C}\,\overline{B}\,\overline{A} + 0)$$

$$= AB + A\,\overline{C}\,\overline{A} + A\,\overline{C}\,\overline{B}\,\overline{A}$$

$$= AB + 0 + 0$$

$$= AB$$

3. *Reduce the expression:*

$$A + B[AC + (B + \overline{C})D]$$

Solution:

The given expression is

$$A + B[AC + (B + \overline{C})D]$$

$$= A + B(AC + BD + \overline{C}D)$$

$$= A + BAC + BBD + B\overline{C}D$$

$$= A + ABC + BD + BD\overline{C}$$

$$= A\,(1 + BC) + BD(1 + \overline{C})$$

$$= A\,.\,1 + BD\,.\,1$$

$$= A + BD$$

4. *Reduce the expression*

$$\overline{(A + \overline{BC})}\,(A\overline{B} + ABC)$$

Solution:

The given expression is

$$\overline{(A + \overline{BC})}\,(A\overline{B} + ABC)$$

$$= (\overline{A}\,\overline{BC})\,(A\,\overline{B} + ABC)$$

$$= (\overline{A}\,BC)\,(A\,\overline{B} + ABC)$$

$$= \overline{A}\,BC\;\; A\,\overline{B} + \overline{A}BC\;\; ABC$$

$$= A\,\overline{A}\,B\,\overline{B}C + A\overline{A}BBCC$$

$$= 0 + 0 = 0$$

5. *Reduce the expression*

$$(B + BC)\,(B + \overline{B}C)\,(B + D)$$

Solution:

The given expression is

$$(B + BC)\,(B + \overline{B}C)\,(B + D)$$

$$= (BB + BCB + B\overline{B}C + BC\overline{B}C)\,(B + D)$$

$$= (B + BC + 0 + 0)\,(B + D)$$

$$= B(1 + C)\,(B + D)$$

$$= B(B + D)$$

$$= BB + BD$$

$$= B(1 + D) = B$$

6. *Show that*

$$AB + A\overline{B}C + B\overline{C} = AC + B\overline{C}$$

Solution:

The given expression is

$$AB + A\overline{B}C + B\overline{C} = A(B + \overline{B}C) + B\overline{C}$$

$$= A(B + \overline{B})\,(B + C) + B\overline{C}$$

$$= AB + AC + B\overline{C}$$

$$= AB\,(C + \overline{C}) + AC + B\overline{C}$$

$$= ABC + AB\overline{C} + AC + B\overline{C}$$

$$= AC(1 + B) + B\overline{C}(1 + A)$$

$$= AC + B\overline{C}$$

7. ***Show that***

$$A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C = B + C$$

Solution:

The given expression is

$$A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C$$

$$= A\overline{B}C + \overline{A}C + B(1 + \overline{D} + A\overline{D})$$

$$= C(\overline{A} + A\overline{B}) + B$$

$$= C(\overline{A} + A)(\overline{A} + \overline{B}) + B$$

$$= C\overline{A} + C\overline{B} + B$$

$$= (B + C)(B + \overline{B}) + C\overline{A}$$

$$= B + C + C\overline{A}$$

$$= B + C(1 + \overline{A})$$

$$= B + C$$

EXERCISES

I. Descriptive Type Questions

1. Write the truth table of an OR function and realize an OR gate using diodes.
2. Simplify and realize the following using NAND gates A B C + A B C + A B + A C.
3. Realize a half adder using AND, OR and inverter logic gates. Write the truth table.
4. Realize a full adder using two half adders.
5. Draw the logic circuit for Full Adder and write its truth table.
6. Explain how AND, OR and NOT gates can be obtained using only NOR gates.
7. Realize full adder using two half adders and OR gate.
8. Realize AND gate using diodes.
9. Implement XNOR using only NOR gate.
10. List the properties of Boolean Algebra with an example.
11. Draw a full adder circuit with the truth table.
12. Implement OR and AND gates using NOR gates.
13. Realize full adder using (i) NAND gates and (ii) NOR gates
14. Realize half adder using (i) NAND gates and (ii) NOR gates

II. Multiple Choice Questions

1. The Boolean expression Y = A.B represents _____

   (a) OR gate (b) XNOR gate

   (c) AND gate (d) NOT gate

2. To add two m-bit number, the number of required half adders is _____

   (a) 2m-1 (b) 2m

   (c) 2^m-1 (d) 2m+1

3. The decimal number 37 is represented in BCD by _____

   (a) 100111 (b) 00111011

   (d) 00110111 (d) 111100

4. A NOT circuit can be built by using _____

   (a) MOSFET (b) Diode

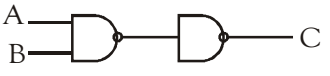
   (c) Zener Code (d) BJT

5. De-Morgan theorem states that A + B =_____
   (a) $\overline{A}+\overline{B}$ (b) $\overline{A}.\overline{B}$
   (c) $\overline{AB}$ (d) None
6. Universal gates are _____and_____
   (a) NOT and NOR (b) AND and OR
   (c) NAND and NOR (d) EXOR and EX-NOR
7. A + AB + A = _____
   (a) AB (c) A + B
   (c) A (d) 0
8. The output is High only when all the inputs are high, such a gate is called.
   (a) NAND (b) NOR
   (c) AND (d) OR
9. A + AB =_____
   (a) AB (b) A
   (c) B (d) 1+A
10. Universal gate is _____
    (a) NOT (b) AND
    (c) OR (d) NAND
11. If x + 1= 1 and x. 1 = 0, then x is _____
    (a) 0 (b) 1
    (c) Could be 0 or 1 (d) Situation can never be true
12. The output is high only when both inputs are zero to a gate. The gate is _____
    (a) AND (b) NOR
    (c) OR (d) NAND.
13. A logic gate is an electronic circuit which _____
    (a) makes logic decisions (b) allows electron flow only in one direction
    (c) works on binary algebra (d) alternates between 0 and 1 values
14. In positive logic, logic state 1 corresponds to _____
    (a) positive voltage (b) higher voltage level
    (c) zero voltage level (d) lower voltage level
15. In negative logic, logic state 1 corresponds to _____
    (a) negative voltage (b) zero voltage
    (c) more negative voltage (d) lower voltage level

16. The output of a 2-input OR gate is zero only when its _____
    (a) both inputs are 0 (b) either input is 1
    (c) both inputs are 1 (d) either input is 0
17. An XOR gate produces zero output only when its two inputs are _____
    (a) high (b) low
    (c) different (d) same
18. An AND gate _____
    (a) implements logic addition (b) is equivalent to a series switching circuit
    (c) is an any-or-all gate (d) is equivalent to a parallel switching circuit
19. When an input electrical signal A=10100 is applied to a NOT gate, the output is.....
    (a) 01011 (b) 10101
    (c) 10100 (d) 00101
20. The only function of a NOT gate is to _____
    (a) stop a signal (b) recomplement a signal
    (c) invert an input signal (d) act as a universal gate
21. A NOR gate is ON only when all its inputs are _____
    (a) ON (b) positive
    (c) high (d) OFF
22. The truth table shown in following figure is for a/an _____ gate.
    (a) XNOR (b) OR
    (c) AND (d) NAND

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

23. For getting high output from an XNOR gate, its both inputs must be _____
    (a) high (b) low
    (c) at the same logic level (d) at the opposite logic levels
24. The arrangement shown in fig. performs the logic function of a/an _____ gate.
    (a) AND (b) NAND
    (c) OR (d) XOR

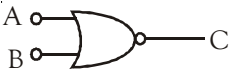


25. In a certain 2-input logic gate, when A=0, B=0, then C=1 and when A=0, B=1, then C=1. It must be _____ gate

(a) XOR (b) AND

(c) NAND (d) NOR

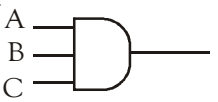
26. The logic symbol shown in Fig. represents _____



(a) single-output AND gate (b) NAND gate

(c) NAND gate used as NOT gate (d) NOR gate

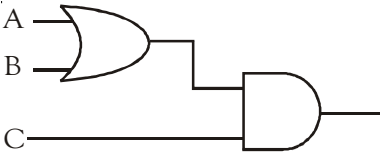
27. The output from the logic gate shown in following figure will be available when inputs _____ are present.



(a) A and C (b) B and C

(c) A, B and C (d) A and B

28. To get an output 1 from following circuit, the input A B C must be.....



(a) 010 (b) 100

(c) 101 (d) 110

III. Numerical Problems

1. Simplify the following Boolean expressions

(i) $Y = \left(\overline{AB} + \overline{A} + AB\right)$ (ii) Y = AB + A(B + C) + B(B + C)

2. Realize the following expressions using only NAND gates.

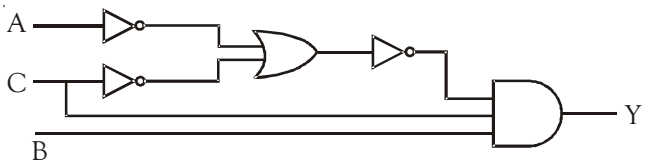
(i) $Y = \overline{ab} + \overline{a}b$ (ii) $Y = \left(A + \overline{B} + C\right).\left(\overline{A} + B + C\right)$ (06 marks)

3. Prove that AB+A+AB=0

4. Simplify

$\overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y} + \overline{X}\,\overline{Y}$

5. Write the boolean expression for output Y, for the following logic circuit.



6. Realize the following expression using NOR gates Y=A $\left(\overline{B}+C\right)$

7. Simplify using De-Morgan's theorem.

$$\overline{\overline{\overline{A}BCD}}$$

8. Prove that $\overline{\overline{AB}+\overline{A}+AB}=0$

9. Simplify $ABC+AB\overline{C}+\overline{A}BC$

Answers to Multiple Choice Questions

1. (c)	2. (a)	3. (c)	4. (d)	5. (d)	6. (c)	7. (c)	8. (c)	9. (b)	10. (d)	11. (a)
12 (b)	13. (a)	14. (b)	15. (d)	16. (a)	17. (d)	18. (d)	19. (a)	20. (c)	21. (d)	22. (b)
23. (c)	24. (a)	25. (c).	26. (d)	27. (c)	28. (c)					

MODEL QUESTION PAPER

MODEL QUESTION PAPER-I

Time : 3 Hrs. **Max. Marks : 100**

Note : 1. Answer any FIVE full questions, selecting at least TWO questions from each part.
2. Standard notations are used & Missing data may be suitably assumed.
3. Answer all objective type questions only on OMR sheet, page 5 of answer book.
4. Objective type questions, if answered on other than OMR sheet, will not be valued.

PART – A

1. (a) (i) The barrier potential silicon diode is approximately _____
(a) 0.3 V (b) 0.1 V
(c) 0.7 V (d) 1.2 V

(ii) Zener diode is _____ doped compared to semiconductor P-N Junction diode.
(a) Lightly (b) Heavily
(c) Equally (d) Un-doped

(iii) The conventional current in P-N junction diode flows _____
(a) From positive to negative (b) From negative to positive
(c) In the direction opposite to the electron flow
(d) Both A & C

(iv) Ripple voltage of Half-wave rectifier is _____
(a) 0.482 (b) 1.21
(c) Equal to Full-wave rectifier (d) 0.89 *(04 Marks)*

(b) Draw and explain the V-I characteristic of Si and Ge diodes. *(06 Marks)*

(c) Derive an expression for ripple factor and output DC voltage of a full-wave rectifier with C filter. *(06 Marks)*

(d) Design a Zener regulator for the following specifications: Output voltage V_O = 5 V, Input voltage V_i = 12 ± 3 V, Load current I_L = 20 mA, Zener wattage P_Z = 500 mW. *(04 Marks)*

2. (a) (i) If α = 0.95, then the value of β of the transistor is _____
(a) 190 (b) 19
(c) 0.05 (d) 25

(ii) In saturation region, the collector – base and emitter-base junctions are _____

(a) Forward (b) Reverse
(c) Unbiased (d) None of these

(iii) The stability factor S is the rate of change of collector current with respect to _____

(a) Reverse Saturation current (b) Collector current
(c) Emitter current (d) Base current

(iv) For keeping Q-point of a transistor fixed, the value of Stability factor should be _____

(a) Higher than Unity (b) Zero
(c) Unity (d) Lower than Unity *(04 Marks)*

(b) Explain the transistor common-emitter configuration and draw a circuit for drawing the common-emitter characteristics. Draw the common-emitter input and output characteristics and explain their shapes. *(06 Marks)*

(c) Why NPN transistors are commonly used in amplifiers. *(04 Marks)*

(d) Calculate α_{dc} and β_{dc} for the transistor if I_C is measured as 1 mA and I_B is 25 μA. Also determine new base current to give I_C = 5 mA. *(06 Marks)*

3. (a) (i) The self bias arrangement gives a better Q-point stability when _____

(a) R_C is small (b) β is small but R_C is large
(c) Both β and R_C are large (d) None of these

(ii) Even with sinusoidal base current we get non-sinusoidal collector current in common emitter configuration because of _____

(a) Noise introduced in base current
(b) Large resistance of the signal source
(c) Large input resistance of transistor
(d) Non parallel output characteristics.

(iii) Which of the following bias is universally used in amplifier circuits _____

(a) Base Bias (b) Collector to base bias
(c) Voltage divider bias (d) None of these

(iv) In an unbiased transistor amplifier, the collector current changes due to _____

(a) Changes in Temperature (b) Changes in device parameters
(c) Changes in the value of dc supply
(d) All of these *(04 Marks)*

(b) Describe the voltage divider method in detail. How stabilization of operating point is achieved by this method ? *(06 Marks)*

(c) Discuss the thermal stability of transistor bias circuit with respect to I_{CBO} and V_{BE}. *(04 Marks)*

(d) Design a voltage divider bias circuit with V_{CC} = 12 V, V_{CE} = 6 V, I_C = 5 mA, and β = 100. *(06 Marks)*

4. (a) (i) SCR is also called _____

(a) Unijunction Transistor (b) Triode

(c) Thyristor (d) MOSFET

(ii) UJT is commonly used in construction of _____ electronic circuits

(a) Amplifiers (b) Oscillators

(c) Saw tooth generators (d) Rectifiers

(iii) FET has _____ regions in its V-I characteristic curve

(a) 2 (b) 3

(c) 4 (d) 5

(iv) The drain and source terminals of a JFET are _____

(a) Interchangeable (b) Not interchangeable

(c) Separated by one p-n junction

(d) Separated by two p-n junction *(04 marks)*

(b) Explain the construction and working of an SCR. Draw the equivalent circuit of an SCR and explain its working from this equivalent circuit. *(08 Marks)*

(c) Draw a circuit diagram to obtain the drain characteristics for an n-channel JFET. Thus draw drain characteristics and explain them. *(08 Marks)*

PART – B

5. (a) (i) The conditions $A\beta$ = 1 for oscillations is known as the _____ criterion

(a) Nyquist's (b) Barkhaular

(c) Routh - Horwitz (d) None of these

(ii) In an Oscillator we use _____ feedback

(a) Positive (b) Negative

(c) Neither (d) Unity Gain

(iii) The overall voltage gain of two stage capacitor coupled CE amplifier is _____ than a single stage CE amplifier.

(a) Greater (b) Less

(c) Equal (d) None

(iv) One decibel represents a power ratio of _____

(a) 1.26 (b) 0.707

(c) 28 % (d) Both (a) & (c) are correct *(04 Marks)*

(b) With principle and neat circuit diagram, explain the working of Colpitt's Oscillator. Obtain an expression for frequency of oscillation ? What are its applications ? *(10 Marks)*

(c) A negative feedback amplifier has an open loop gain of 400 and a feedback factor of 0.1. If the open-loop gain changes by 20% due to temperature, find the percentage change in closed-loop gain. *(06 Marks)*

6. (a) (i) In inverting amplifier, there is _____ Phase shift with input and output

(a) 0° (b) 90°

(c) 180° (d) 360°

(ii) When both inputs of OP-AMP are grounded, the voltage across the output is called _____

(a) Output off set voltage (b) Output grounded voltage

(c) Output bias voltage (d) Output common voltage

(iii) The output of Integrator is _____

(a) Linearly-increasing ramp output

(b) Linearly-increasing square output

(c) Integrated zigzag signal

(d) None of these

(iv) The value of slew rate for ordinary OP-AMP is _____

(a) 0.7 V/μV (b) Offset voltage

(c) 7 V/μV (d) None of these *(04 Marks)*

(b) Explain the application of an OP-AMP as a Voltage Follower. *(04 Marks)*

(c) With the help of circuit diagram explain the working of an integrator. Give the typical input and output waveforms. *(06 Marks)*

(d) Draw the block diagram of CRO and explain its function of each stage? *(06 Marks)*

7. (a) (i) The AM signal that occupies the greatest bandwidths is the one modulated by _____

(a) 1 KHz sine wave (b) 10 KHz sine wave

(c) 1 KHz square wave (d) 5 KHz square wave

(ii) On an FM signal, maximum deviation occurs at _____

(a) Zero crossing point (b) Peak positive amplitude

(c) Peak negative amplitude (d) Both (A) and (B)

(iii) $(25)_{10} = (?)_2$

(a) $(00111)_2$ (b) $(11001)_2$
(c) $(11000)_2$ (d) $(00011)_2$.

(iv) The number 1000_2 is equivalent to decimal number

(a) one thousand (b) eight
(c) four (d) sixteen *(04 Marks)*

(b) With block diagram, explain various stages of FM superhetrodyne receiver *(06 Marks)*

(c) A carrier of 500 W, 1 MHz is amplitude modulated by sinusoidal signal of 1 KHz to a depth of 60%. Calculate bandwidth, power in each side band and total power transmitted. *(05 Marks)*

(d) Convert the following binary numbers to hexadecimal and octal:

(a) 100101010011 (b) 001011101111
(c) 1011.111010101101 *(05 Marks)*

8. (a) (i) The decimal number 37 is represented in BCD by _____

(a) 100111 (b) 00111011
(c) 00110111 (d) 111100

(ii) De-Morgan theorem states that A + B =_____

(a) $\overline{A} + \overline{B}$ (b) $\overline{A} \cdot \overline{B}$
(c) $\overline{AB}$ (d) None

(iii) If x + 1= 1 and x . 1 = 0, then x is

(a) 0 (b) 1
(c) Could be 0 or 1 (d) Situation can never be true

(iv) For getting an output from an output from an XNOR gate, its both inputs must be

(a) high (b) low
(c) at the same logic level (d) at the opposite logic levels *(04 Marks)*

(b) Prove that $\overline{\overline{AB} + \overline{A} + AB} = 0$ *(04 Marks)*

(c) Realize full adder using (i) NAND gates and (ii) NOR gates *(06 Marks)*

(d) Realize the following expressions using only NAND gates.

(i) $y = \overline{ab} + \overline{a}b$ (ii) $y = \left(A + \overline{B} + C\right).(\overline{A} + B + C)$ *(06 Marks)*

MODEL QUESTION PAPER

MODEL QUESTION PAPER-II

Time : 3 Hrs. **Max. Marks : 100**

Note : 1. Answer any FIVE full questions, selecting at least TWO questions from each part.
2. Standard notations are used & Missing data may be suitably assumed.
3. Answer all objective type questions only on OMR sheet, page 5 of answer booklet.
4. Objective type questions, if answered on other than OMR sheet, will not be valued.

PART – A

1. (a) (i) If the P-N junction is heavily doped, breakdown voltage will _____

(a) Increases (b) Decreases
(c) Remains constant (d) None of these

(ii) A half-wave rectifier is fed from secondary of a transformer whose output voltage is 12.6 V. The dc voltage of the rectifier output is _____

(a) 12.6 V (b) 5.66 V
(c) 17.8 V (d) 11.32 V

(iii) Zener diode acts as a _____ device

(a) Constant current (b) Constant voltage
(c) Constant power (d) Variable voltage

(iv) In Full-Wave rectifier, the ripple voltage is _____ Half-wave rectifier.

(a) Double (b) Half
(c) Equal (d) Quarter *(04 Marks)*

(b) With circuit diagram, explain forward bias and reverse bias operations of a semiconductor junction diode. *(06 Marks)*

(c) With the help of a circuit diagram and waveforms explain the working of a capacitive filter. *(05 Marks)*

(d) A full wave bridge rectifier supplies a load of 400 Ω in parallel with a capacitor of 500 μF. If the ac supply voltage is 230 sin 314 t Volts, find the (i) Ripple factor and (ii) DC load current. *(05 Marks)*

2. (a) (i) Stability factor of CE configuration is _____

(a) 1 (b) β
(c) β + 1 (d) None of these

(ii) Thermal runaway leads to _____

(a) Fluctuations in output current

(b) Enhanced temperature of transistor

(c) Damage of transistor

(d) All of these

(iii) Which of the following amplifier has voltage gain less than Unity ?

(a) Common Base (b) Common Emitter
(c) Common Collector (d) Operational Amplifier

(iv) If we reverse bias E/B and C/B junctions, the transistor will be in _____ region

(a) Saturation (b) Active
(c) Cut-off (d) Amplification *(04 Marks)*

(b) Draw a block diagram of an un-biased n-p-n transistor. Identify each part of the device and show the depletion regions and barrier voltages. Briefly explain. *(06 Marks)*

(c) What is dc load line? How to draw it ? *(04 Marks)*

(d) Determine the transistor currents in a fixed bias circuit with V_{BB} = 5 V, V_{CC} = 12 V, R_B = 220 KΩ, R_C = 3.3 KΩ if β = 100. *(06 Marks)*

3. (a) (i) Base bias is also called _____

(a) Fixed bias (b) Self bias
(c) Both (a) & (b) (d) None of these

(ii) Stability factor of Voltage divider bias is _____

(a) Close to 1 (b) Independent on β
(c) Both (a) & (b) (d) None of these

(iii) Reverse saturation current doubles for every _____ ^{O}C rise in temperature.

(a) 50 (b) 40
(c) 30 (d) 10

(iv) When used as a switch the transistor operates in _____

(a) Active region (b) Saturation and cut-off region
(c) Active and saturation region (d) Cut-off region.

(b) Compare base bias, collector to base bias and voltage divider bias with regard to stability of the transistor collector voltage with spread in h_{FE} value. (06 Marks)

(c) Design the Collector-to-Base Bias Circuit so that the supply voltage is 20 V, V_{CE}= 5 V, I_C = 6 mA and the transistor β is 100. *(05 Marks)*

(d) A collector–to–base bias circuit has V_{CC} = 5 V, R_C = 5.6 KΩ, R_B = 82 KΩ, and V_{CE} = 5 V. Determine the transistor h_{FE} value. Calculate new V_{CE} level when a transistor with h_{FE} = 50 is substituted. *(05 Marks)*

4. (a) (i) SCR can be analyzed using _____ transistors

(a) Two transistors (b) Three transistors
(c) Four transistors (d) One transistors and one diode.

(ii) A relaxation oscillator uses _____

(a) MOSFET (b) SCR
(c) UJT (d) BJT

(iii) The gate current of a JFET is

(a) Very large (b) Very small
(c) Significant (d) Depends on input voltage

(iv) The noise level in JFET is _____ as compared to ordinary transistor.

(a) Less (b) more
(c) Equal (d) Zero *(04 Marks)*

(b) Explain the action of an SCR as a switch. What are the advantages of SCR switch over a mechanical or electro-mechanical switch? *(05 Marks)*

(c) What is the difference between a JFET and a bipolar transistor ? *(05 Marks)*

(d) Find the range of R_T for the UJT oscillator that will ensure proper turn ON and OFF of the UJT used. Given : $\eta = 0.33$, $V_V = 0.8$ V, $I_V = 15$ mA, $I_P = 35$ μA, and $V_P = 18$ V. Assume $V_{BB} = 30$ V. *(06 Marks)*

PART – B

5. (a) (i) CE amplifier produces _____

(a) 90° Phase difference between input and output

(b) 180° Phase difference between input and output

(c) 360° Phase difference between input and output

(d) 0° Phase difference between input and output

(ii) In two stage CE amplifier, the total gain is _____

(a) Sum of the gains individual stages

(b) Difference of the gains individual stages

(c) Product of the gains individual stages

(d) Ratio of the gains individual stages

(iii) The output voltage of an amplifier is measured as 1 V at 5 kHz, and as 0.707 V at 20 kHz. The output power change is _____

(a) 1 dB (b) – 1 dB
(c) – 3dB (d) + 3 dB

(iv) Barkhausen Criterion for oscillation is _____

(a) Total phase shift between input signal and feedback signal should be 0° or 360°

(b) $|A\beta| = 1$

(c) Both (a) and (b)

(d) None of these *(04 Marks)*

(b) Explain with neat block diagram, Barkhausen criterion to generate oscillations, with special reference to the condition $A\beta < 1$, $A\beta > 1$, $A\beta = 1$. *(06 Marks)*

(c) Using ac equivalent circuit of CE amplifier, obtain expression for Input impedance, Output impedance, Voltage gain and Current gain of a single stage RC coupled CE amplifier? *(06 Marks)*

(d) Determine the oscillation frequency of a Colpitts Oscillator if the parametric values of its tank circuit are C_1 = 750 pF, C_2 = 2500 pF, L = 40 mH. *(04 Marks)*

6. (a) (i) The maximum rate at which amplifier output can change in volts per micro second (V/μS) is called _____

(a) Over rate (b) Slew rate

(c) Under rate (d) None

(ii) When both inputs of OP-AMP are grounded, the voltage across the output is called _____

(a) Output off set voltage (b) Output grounded voltage

(c) Output bias voltage (d) Output common voltage

(iii) The carbon particles coating in CRT, to remove the electrons along the side walls of the tube is called _____

(a) Aquadag coating (b) Florescent coating

(c) Both of these (d) None of these

(iv) The differential voltage between non-inverting and inverting input of an OP-AMP is always zero, and is called

(a) The virtual ground (b) Real ground

(c) Differentiated output (d) Zero input resistance *(04 Marks)*

(b) List the characteristics of an ideal OP-AMP. *(04 Marks)*

(c) Show how OP-AMP can be used as an inverting amplifier. Derive an expression for the voltage gain. *(06 Marks)*

(d) With a neat diagram, explain the working of an OP-AMP summing amplifier. *(06 Marks)*

7. (a) (i) The binary equivalent of A_{16} is

(a) 1010 (b) 1011

(c) 1000 (d) 1110

(ii) Hexadecimal number system is used as a shorthand language for representing _____ numbers.

(a) decimal (b) binary

(c) octal (d) large

(iii) The expression for channel capacity with band width B and, Signal to Noise Ratio *S/N* is ____

(a) [B $\log_2$ (l + S/N)] bits/sec. (b) [$\log_2$ (B + S/N)] bits/sec.

(c) [B $\log_2$ (l – S/N)] bits/sec. (d) [$\log_2$ (B + S/N)] bits/sec.

(iv) The telephone line has a Band width (BW) of _____

(a) 3 KHz (b) 30 KHz

(c) 3 MHz (d) 30 MHz *(04 Marks)*

(b) Compare AM & FM ? *(05 Marks)*

(c) Obtain an expression for voltage in A.M. signal. What are the side bands and modulation index ? *(06 Marks)*

(d) A carrier of 750 W, 1 MHz is amplitude modulated by sinusoidal signal of 2 KHz to a depth of 50%. Calculate bandwidth, power in each side band and total power transmitted. *(05 Marks)*

8. (a) (i) A logic gate is an electronic circuit which

(a) makes logic decisions (b) allows electron flow only in one direction

(c) works on binary algebra (d) alternates between 0 and 1 values

(ii) In negative logic, logic state 1 corresponds to

(a) negative voltage (b) zero voltage

(c) more negative voltage (d) lower voltage level

(iii) Universal gate is _____

(a) NOT (b) AND

(c) OR (d) NAND

(iv) The Boolean expression Y = A.B represents _____

(a) OR gate (b) XNOR gate

(c) AND gate (d) NOT gate *(04 Marks)*

(b) Draw the logic circuit for Full Adder and write its truth table. *(05 Marks)*

(c) Explain how AND, OR and NOT gates can be obtained using only NOR gates *(5 Marks)*

(d) List the properties of Boolean Algebra with an example *(06 Marks)*

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BASIC ELECTRONICS

This book has been designed to understand the basic concepts and components used in the field of Electronics to cater the need of Science & Engineering students. The book covers both fundamental concepts and practical applications of various electronic components including diodes and transistors in various circuits like rectification, amplification, signal generation, signal communication, analog and digital arithmetic operations, signal switching, and logical operations. It focuses on several important topics including Semiconductor diode and applications, Transistor and Biasing methods, Special devices using, SCR, UIT, and FET, and the processes like amplification, oscillation, communication and signal processing. This book is very useful for the students of B.E./B.Tech., Diploma, and AIME/IETE courses. However, the book is specially designed to cover the latest syllabus of BASIC ELECTRONICS of the First year Engineering students of Visvesvaraya Technological University (VTU), Belgaum, Karnataka State. The emphasis is given on basic concepts & problem solution approach.

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