Cryo-CMOS Charge-Sensitive Amplifier for Quantum-Sensor Readout

Sanjay Selvakumar

Abstract

This paper describes a cryogenic-CMOS charge-sensitive amplifier (CSA) for semiconductor quantum-sensor readout. A five-transistor operational transconductance amplifier (OTA) is tested with an ideal tail source and with an NMOS mirror-tail bias. Using $\pm 1.8\,\mathrm{V}$ supplies, a $10\,\mu\mathrm{A}$-class tail current, $C_f = 10\,\mathrm{fF}$, $R_f = 100\,\mathrm{M}\Omega$, and $C_s = 100\,\mathrm{fF}$, LTspice transient, noise, and AC simulations are used to check charge gain, baseline drift, noise, and bandwidth. The simulated charge gain is 15.4% of the ideal Q/C_f value, mainly because of finite OTA gain and parasitic capacitance.

1 Introduction

Semiconductor quantum sensors produce small charge or current pulses. The readout circuit must therefore be low-noise, stable, low-power, and high enough in gain. A CSA is a good fit because C_f converts input charge to output voltage, and the noise can be reported as equivalent noise charge (ENC) [2, 3].

At cryogenic temperature, the design becomes harder because cooling power is limited and device parameters shift. Cryogenic CMOS is still useful because it can move readout closer to the sensor or quantum processor and reduce wiring complexity [1, 5].

This paper studies a compact differential-input CSA with a PMOS mirror load, capacitive feedback, and two tail-bias choices: an ideal current source and an NMOS current mirror. The temperature sweep runs from room temperature to liquid-nitrogen conditions and also includes $-268\,^{\circ}\mathrm{C}$, about 5 K. The 5 K point is treated as a stress test, not as a calibrated model result [5, 6].

Study scope. Two tail-bias options are compared. The ideal current source gives a clean baseline for the OTA and feedback loop. The NMOS mirror tail is more realistic, but it adds reference-current, headroom, noise, and temperature-stability limits.

2 Circuit Architecture

Fig. 1 shows the two CSA versions. In both cases, input charge is stored on C_f and appears as an output-voltage step [2, 4].

The ideal-tail case in Fig. 1(a) is the baseline. The mirror-tail case in Fig. 1(b) keeps the same signal path but replaces the ideal sink with an NMOS mirror.

2.1 Differential Input Pair

Transistors M_1 and M_2 form the NMOS differential input pair. One gate is tied to the reference, and the other receives the sensor signal.

The shared tail current constrains the total branch current,

$$I_{\mathrm{tail}} = I_{D1} + I_{D2}, \tag{1}$$

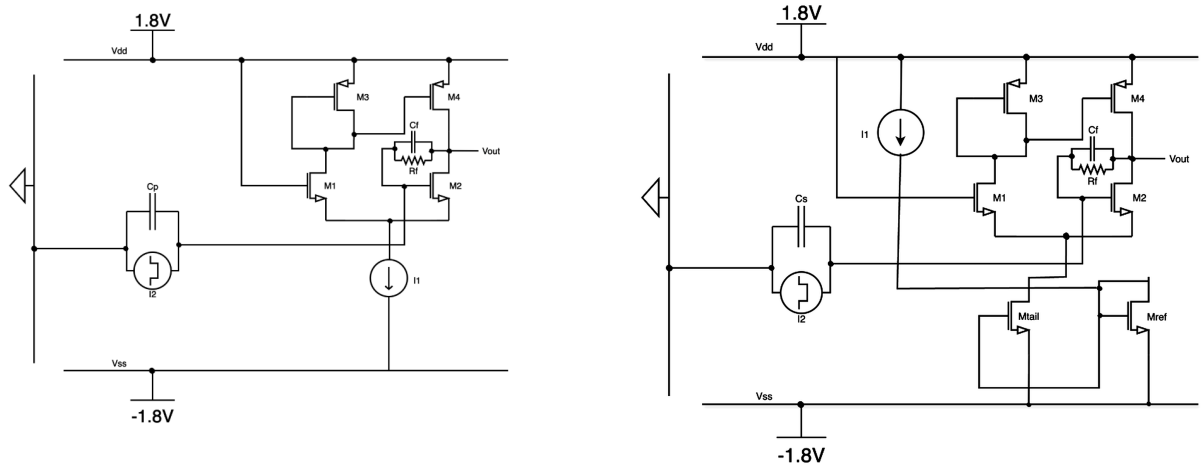
so the input signal shifts current between the two branches. This provides common-mode rejection and supports a near-virtual input node at low current [6].

2.2 Current-Mirror Active Load

PMOS devices M_3 and M_4 form the active mirror load. The diode-connected side sets the mir-

Table 1: Summary of Design Metrics

Metric	Value / Observation	Implication
Injected charge	$Q_{\text{in}} \approx 10\,\text{fC}$	Defines the transient input scale
Ideal charge gain	$1/C_f = 100\,\text{mV/fC}$	Higher gain increases sensitivity to parasitic capacitance
Ideal pulse step	Ideal: 1 V; simulated: 154 mV (15.4%)	Upper bound before finite-gain and capacitance loss
Reset constant	$R_f C_f = 1\,\mu\text{s}$	Exceeds the 100 ns pulse period, producing incomplete recovery
Bias power	36 µW ideal; 73.44 µW mirror	Dedicated reference plus 10.4 µA mirrored tail approximately doubles bias power
AC result	$Z_{t,\max} \approx 99.96\,\text{M}\Omega$, $f_{-3\text{dB}} = 158.6\,\text{kHz}$ at 27 °C	AC response shows feedback transimpedance, not open-loop OTA voltage gain
Noise extraction	$v_{n,\text{out}} = 0.825\,\text{mV}$, ENC $\approx 51.5\ \text{e}^-$ at 300 K; 0.260 mV at 5 K	Integrated noise trend; sampled reset noise remains separate
Temperature sensitivity	greater mirror-tail drift; shared −196 °C step anomaly	Mirror compliance, threshold shift, and model convergence dominate baseline stability



(a) Ideal tail-current baseline. **(b)** NMOS current-mirror tail bias.

Figure 1: CSA schematic variants. Both use the same input pair, PMOS active load, sensor model, feedback capacitor, and reset path; only the tail-bias implementation changes.

ror gate voltage, and the other side turns the differential current change into V_{out}.

The high output resistance helps convert small current changes into voltage swing.

2.3 Current-Mirror Tail-Bias Variant

Fig. 1(b) replaces ideal source I_1 with an NMOS current mirror. In this schematic, M_{tail} is the tail sink and M_{ref} is the diode-connected reference device. The reference branch is driven by a regulated 10 µA current instead of being tied directly to the rail. This avoids an uncontrolled low-impedance path through M_{ref}. The target currents are

$$I_{\text{ref}} = 10\,\mu\text{A}, \qquad I_{\text{tail}} \approx 10.4\,\mu\text{A}. \tag{2}$$

The mirror-current error is

$$\begin{aligned} \epsilon_I &= \frac{I_{\text{tail}} - I_{\text{ref}}}{I_{\text{ref}}} \times 100\% \\ &= \frac{10.4 - 10}{10} \times 100\% = 4\%. \end{aligned} \tag{3}$$

For matched long-channel devices in saturation,

$$I_{\text{tail}} \approx I_{\text{ref}} \frac{(W/L)_{\text{tail}}}{(W/L)_{\text{ref}}} \frac{1 + \lambda V_{DS,\text{tail}}}{1 + \lambda V_{DS,\text{ref}}}. \tag{4}$$

Here M_{tail} and M_{ref} both use $W/L = 5\,\mu\text{m}/1\,\mu\text{m}$, so the ideal geometry ratio is one. The remaining

4% error comes from finite output resistance, compliance, and unequal drain-source voltages.

The tail-sink output resistance is approximated by

$$r_{o,\mathrm{tail}} \approx \frac{1}{\lambda I_{\mathrm{tail}}}, \tag{5}$$

and the source node must satisfy

$$V_{S,\mathrm{pair}} - V_{SS} \gtrsim V_{OV,\mathrm{tail}}. \tag{6}$$

Here V_{OV} is the overdrive voltage. The mirror-tail option is useful because it is closer to an integrated bias circuit, but it also requires checks for reference-current accuracy, M_{tail} saturation, mirror noise, and temperature drift.

2.4 Feedback and Sensor Model

The CSA is set by the feedback capacitor $C_f = 10\,\mathrm{fF}$, reset resistor $R_f = 100\,\mathrm{M\Omega}$, sensor capacitance $C_s = 100\,\mathrm{fF}$, and input pulse source I_2, following standard detector CSA models [2, 3].

The input pulse is $1\,\mu\mathrm{A}$, with 1 ns rise/fall time, 10 ns width, and 100 ns period. Its nominal charge is

$$\begin{aligned} Q_{\mathrm{in}} &= \int_0^{T_{\mathrm{on}}} i_{\mathrm{in}}(t)\,dt \approx I_{\mathrm{pulse}} T_{\mathrm{on}} \\ &= (1\,\mu\mathrm{A})(10\,\mathrm{ns}) = 10\,\mathrm{fC}. \end{aligned} \tag{7}$$

The transient simulation includes finite pulse edges, so (7) is used as the charge scale, not as an exact integral of the source waveform.

The detector network (C_s, I_2) and feedback network $R_f \parallel C_f$ connect to the inverting gate of M_2. The non-inverting gate of M_1 stays at the reference voltage. With the OTA convention

$$v_o = A_v(v_+ - v_-), \tag{8}$$

a positive output change feeds back through $R_f \parallel C_f$ and raises v_-. This reduces $v_+ - v_-$, so the feedback is negative. If the detector node is left open-loop or routed incorrectly, small offsets can drive the output toward a rail. The corrected routing keeps the DC point stable and allows charge-sensitive operation.

For an ideal high-gain CSA, the inverting input stays near virtual ground. Then $Q_{\mathrm{in}} + C_f \Delta V_{\mathrm{out}} \approx 0$, so

$$\Delta V_{\mathrm{out}} \approx -\frac{Q_{\mathrm{in}}}{C_f}. \tag{9}$$

With finite open-loop gain A_v, the input node still moves by about $\Delta v_x \approx -\Delta V_{\mathrm{out}}/(1 + A_v)$. This lets C_s and input capacitance take some of the charge.

Charge balance at the input node gives

$$Q_{\mathrm{in}} \approx -\Delta V_{\mathrm{out}} \left[C_f + \frac{C_s + C_{\mathrm{in}}}{1 + A_v} \right], \tag{10}$$

which gives the finite-gain estimate

$$\Delta V_{\mathrm{out}} \approx -\frac{Q_{\mathrm{in}}}{C_f + (C_s + C_{\mathrm{in}})/(1 + A_v)}. \tag{11}$$

Between pulses, $C_f\, dv_{\mathrm{out}}/dt + v_{\mathrm{out}}/R_f = 0$, so the output decays with

$$\tau_f = R_f C_f = (100\,\mathrm{M\Omega})(10\,\mathrm{fF}) = 1\,\mu\mathrm{s}. \tag{12}$$

This is longer than the 100 ns pulse period, so the output does not fully reset between pulses.

2.5 Small-Signal Gain Model

The OTA open-loop gain mainly depends on input-pair transconductance and output resistance. A simple estimate is

$$A_{v0} \approx g_{m,\mathrm{in}} \left(r_{o,n} \parallel r_{o,p} \right), \tag{13}$$

where $g_{m,\mathrm{in}}$ is the transconductance of the active input branch. The mirror tail reduces this gain indirectly because finite tail resistance lets the source node move. This lowers differential conversion and common-mode rejection compared with an ideal tail source.

Above the reset pole, the CSA feedback factor is mainly capacitive,

$$\beta_C \approx \frac{C_f}{C_f + C_s + C_{\mathrm{in}}}, \tag{14}$$

so the OTA needs enough gain to hold the sensor node near virtual ground. This design uses a small C_f for high charge gain, a large R_f for slow reset, and microampere bias current to limit cold-stage power. The input pair and active load must stay in saturation; otherwise g_m, r_o, and loop gain drop.

3 Design Methodology

3.1 Architecture Choice

The five-transistor OTA is used because it is small, uses one main bias current, and gives a high-impedance output. This keeps the CSA behavior easy to study before adding cascoding, gain boosting, or extra bias loops. Those options can improve gain, but they also need more headroom and add more noise and cryogenic-bias concerns.

3.2 Component-Value Choices

The $C_f = 10\,\mathrm{fF}$ capacitor gives high charge gain and a clear ideal-step calculation. The $100\,\mathrm{M\Omega}$ reset path gives $\tau_f = 1\,\mu\mathrm{s}$, which is longer than the pulse period, so incomplete reset can be seen. The mirror reference is $10\,\mu\mathrm{A}$, and the mirrored tail current is about $10.4\,\mu\mathrm{A}$. The $\pm 1.8\,\mathrm{V}$ rails provide OTA and tail-device headroom.

3.3 Device Sizing and Noise Rationale

The schematic keeps micrometer-wide analog devices for matching and noise control. The input pair uses

$$(W/L)_{M_1,M_2} = 10\,\mu\mathrm{m}/1\,\mu\mathrm{m}, \tag{15}$$

and the PMOS loads and NMOS mirror devices use

$$(W/L)_{M_3,M_4,M_{\mathrm{tail}},M_{\mathrm{ref}}} = 5\,\mu\mathrm{m}/1\,\mu\mathrm{m}. \tag{16}$$

The wider input devices reduce input-referred flicker noise because

$$S_{v,1/f}(f) \propto \frac{K_f}{C_{\mathrm{ox}} W L f}, \tag{17}$$

and input transconductance roughly follows

$$g_m \approx \sqrt{2\mu_n C_{\mathrm{ox}} (W/L) I_D}. \tag{18}$$

Increasing W/L for M_1 and M_2 lowers flicker noise and increases g_m, but it also adds gate capacitance. That capacitance is part of the finite-gain loss in (11). The $5\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ load and mirror sizing keeps the bias devices matched at microampere current levels.

3.4 Bias-Point Checklist

Table 2 lists the main DC checks. The goal is to keep the input pair, PMOS load, and NMOS mirror devices in saturation while keeping enough output swing across temperature. The room-temperature log values in Table 3 back up the bias-current and headroom checks with extracted device data.

4 Simulation Setup

LTspice simulations used the OTA and feedback network listed in Table 4. The two tail-bias cases were an ideal sink and an NMOS current mirror.

The sweep covers 300, 250, 200, 150, 77, and 5 K.

The MOS models use first-order parameters such as V_{TO}, K_P, and λ. Because of that, the cold results are not process-calibrated. The sweep should be read as a topology stress test; final signoff would need a foundry PDK or validated cryogenic model [1, 5, 6].

4.1 Simulation Reproducibility

The LTspice schematic files are:

Ideal tail	`csa-frontend-Ideal.asc`
Mirror tail	`csa-frontend-CM.asc`

To reproduce the figures and tables, run the `.op`, `.tran`, `.noise`, `.ac`, and temperature-step analyses, then export the traces to `figures/`. The exact extraction sequence is repeated for both schematics so that the ideal-tail and current-mirror tables are not affected by analysis-command mismatch.

4.2 Simulation Directives and Generated Graphs

The deck uses five directives.

The `.op` command checks DC bias, pair balance, and active-load saturation.

The `.tran 0 500n 0 1n` command captures the 500 ns large-signal response with a 1 ns maximum step, so the pulse edges are resolved.

The noise directive is

Table 2: Bias-Point Verification Checklist

Node / Device	Required Check	Design Relevance
Output node V_{out}	Stays away from both rails across temperature	Preserves CSA output swing
Differential pair M_1, M_2	$V_{DS} > V_{DSAT}$ and balanced branch currents	Maintains transconductance and gain
PMOS load M_3, M_4	Mirror devices remain in saturation	Prevents output-side gain collapse
Ideal tail source	Delivers 10 µA independent of node voltage	Defines the reference bias condition
Mirror tail M_{tail}	Satisfies $V_{S,\text{pair}} - V_{SS} > V_{OV,\text{tail}}$	Prevents compliance loss and baseline shift
Reference mirror M_{ref}	Tracks M_{tail} over temperature	Limits current mismatch and drift

Table 3: Room-Temperature MOSFET Operating Point

Device	Role	I_D	V_{GS}	Extracted check and relevance
M_1	NMOS input	5.24 µA	0.824 V	$r_o \approx 337.8\,\Omega$; headroom compression lowers one input-branch gain
M_2	NMOS input	5.17 µA	0.771 V	Branch current matches M_1 within $\approx 1.3\%$, confirming near-balanced bias
M_3	PMOS load	5.24 µA	0.000 V	Diode-side load branch sets the PMOS mirror reference
M_4	PMOS load	5.16 µA	−0.769 V	Output-side branch mirrors differential current into V_{out}
M_5	NMOS tail	10.39 µA	0.777 V	$V_{DS} = 2.780$ V, $V_{DSAT} = 21$ mV; margin is 2.759 V

Table 4: Design and Simulation Parameters

Parameter	Value
Supply rails	$V_{DD} = +1.8$ V, $V_{SS} = -1.8$ V
Tail current	10 µA ideal; 10.4 µA mirrored tail
Tail-bias cases	Ideal sink and NMOS mirror ($M_{\text{tail}}, M_{\text{ref}}$)
Feedback capacitor	$C_f = 10$ fF
Reset resistor	$R_f = 100$ MΩ
Sensor capacitance	$C_s = 100$ fF
Input-pair sizing	$(W/L)_{M_1,M_2} = 10\,\mu\text{m}/1\,\mu\text{m}$
Load/mirror sizing	$(W/L)_{M_3,M_4,M_{\text{tail}},M_{\text{ref}}} = 5\,\mu\text{m}/1\,\mu\text{m}$
Input pulse	1 µA, 10 ns, 100 ns period
Transient window	500 ns, 1 ns max step
Temperature sweep	300, 250, 200, 150, 77, 5 K
Celsius equivalent	27, −23, −73, −123, −196, −268 °C

```
.noise V(Vout) I2 dec 20 1 1G
```

It computes output-referred noise from 1 Hz to 1 GHz, using I_2 for the ENC estimate.

The `.ac dec 20 1 1G` command gives transimpedance, bandwidth, phase roll-off, and stability trends.

The temperature step includes room temperature, liquid nitrogen, and an approximate liquid-helium stress point. For every extraction pass, the active sweep is

```
.step temp list 27 -23 -73 -123 -196 -268.
```

Table 5: LTspice Temperature-Sweep Trace Assignment

Step	Temp.	Operating point	Color
Step 1	27 °C	Room temperature	Black
Step 2	−23 °C	Cold sweep point	Blue
Step 3	−73 °C	Cold sweep point	Red
Step 4	−123 °C	Cold sweep point	Cyan
Step 5	−196 °C	Liquid-nitrogen point	Magenta
Step 6	−268 °C	Liquid-helium stress point	Gray

Noise extraction comments out the transient and AC commands, leaves `.noise V(Vout) I2 dec 20 1 1G` active, and adds

```
.meas noise total_noise integ V(onoise).
```

Transient step extraction switches back to `.tran 0 500n 0 1n`, comments out AC/noise, and uses

```
.meas tran v_start find V(vout) at 95n
.meas tran v_end find V(vout) at 150n
.meas tran pulse_step param (v_start -
                v_end).
```

The same noise and transient measurement commands are run on the CM and ideal schematic files. Table 5 lists the trace colors.

Static power comes from the tail current across the supply rails. For the ideal-tail baseline,

$$P_{\mathrm{DC,ideal}} \approx (V_{DD} - V_{SS}) I_{\mathrm{tail}} = (3.6\,\mathrm{V})(10\,\mu\mathrm{A}) = 36\,\mu\mathrm{W}. \tag{19}$$

For the mirror-tail case, the core tail branch alone dissipates

$$P_{\mathrm{tail,mirror}} \approx (3.6\,\mathrm{V})(10.4\,\mu\mathrm{A}) = 37.44\,\mu\mathrm{W}. \tag{20}$$

This is small at room temperature but important at a cold stage. Unless the bias current is reduced, the circuit is more suitable for 77 K or intermediate-temperature readout [1, 5].

If the mirror-reference branch is not shared, it adds another 10 µA:

$$P_{\mathrm{DC,mirror}} \approx (V_{DD} - V_{SS})(I_{\mathrm{tail}} + I_{\mathrm{ref}}) = (3.6\,\mathrm{V})(20.4\,\mu\mathrm{A}) = 73.44\,\mu\mathrm{W}. \tag{21}$$

Sharing the reference would reduce this overhead. The local mirror also adds finite output resistance, headroom limits, and noise.

Table 6 separates ideal estimates from LTspice values.

4.3 Impact of Mirror-Tail Bias on Performance

The mirror-tail implementation is less ideal than the current-source baseline. The 15.4% charge-gain result shows that the practical bias and finite loop gain matter.

The main causes are:

- finite tail output resistance, reducing effective differential gain;
- source-node modulation, degrading virtual-ground behavior;
- additional noise from the mirror branch;
- compliance limitations restricting signal swing.

An ideal high-impedance tail would reduce source-node motion and keep loop gain higher. The mirror tail is more realistic, but it costs gain, noise, and headroom. The room-temperature log also shows direct headroom compression: M_1 has only $r_o \approx 337.8\,\Omega$, so the simple $g_m r_o$ branch-gain picture is far below the earlier textbook upper bound based on $r_o = 100\,\mathrm{k}\Omega$.

5 Results and Analysis

The CSA was checked with transient, noise, and AC simulations at nominal and cold-oriented conditions. The goal was to check charge gain, timing, power, and noise, and to explain where the circuit differs from the ideal model.

5.1 Gain and Linearity

Fig. 2 shows the nominal transient response for repeated charge pulses. The step-like output shows that the CSA is working: input charge becomes an output-voltage step with the expected polarity. A separate charge sweep would be needed to fully prove linearity; here the gain is checked at 10 fC.

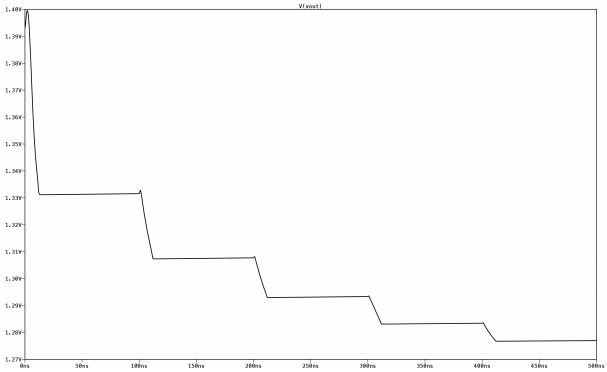


Figure 2: Nominal transient response. The stepped waveform shows charge integration with incomplete reset between 100 ns-spaced pulses.

From the transient waveform, one input pulse gives

$$\Delta V_{\mathrm{sim}} \approx -154\,\mathrm{mV}.$$

Table 6: Extracted and Analytical Performance Metrics

Metric	Value	Interpretation
Charge gain	$1/C_f = 100\,\mathrm{mV/fC}$	Feedback-limited ideal value
Pulse step	$\Delta V_{\mathrm{out}} \approx 1\,\mathrm{V}$ for $Q_{\mathrm{in}} = 10\,\mathrm{fC}$	Upper bound before finite-gain loss
Reset time constant	$\tau_f = 1\,\mu\mathrm{s}$	Ten times the 100 ns pulse period
DC power	$36\,\mu\mathrm{W}$ ideal; $73.44\,\mu\mathrm{W}$ mirror	Mirror reference roughly doubles bias power
Mirror current mismatch	$\epsilon_I \approx 4\%$	Due to finite r_o and unequal V_{DS}
Tail saturation margin	$V_{DS} - V_{DSAT} = 2.759\,\mathrm{V}$ at $27\,^\circ\mathrm{C}$	M_5 remains safely saturated at room temperature
Input-branch compression	$r_{o,M1} \approx 337.8\,\Omega$	Explains why the simple $A_v \approx 20$ estimate is optimistic
Room-temperature transimpedance	$Z_{t,\max} = 159.997\ \mathrm{dB}\Omega \approx 99.96\,\mathrm{M}\Omega$	Extracted from `V(vout)` with I_2 set to AC unity
Room-temperature bandwidth	$f_{-3\mathrm{dB}} = 158.6\,\mathrm{kHz}$	Matches the $R_f C_f$ closed-loop transimpedance pole
Integrated noise	$v_{n,\mathrm{out}} = 0.825\,\mathrm{mV}$, ENC $\approx 51.5\ \mathrm{e}^-$ at 300 K; minimum 0.260 mV at 5 K	Extracted values show the cold extreme has the lowest integrated noise
Reset-noise lower bound	$\mathrm{ENC}_{kT/C} \approx 40\ \mathrm{e}^-$ at 300 K	Separate sampled-reset estimate, not the continuous integrated-noise result
Noise topology comparison	Ideal tail is lower than mirror tail through the cold sweep; values converge at $27\,^\circ\mathrm{C}$	Confirms the current mirror adds a small active-device noise penalty
Pulse-step anomaly	$\approx 34\,\mathrm{mV}$ at $-196\,^\circ\mathrm{C}$ in both tail variants	Shared spike suggests a model/convergence or architecture-level effect
Temperature span	300 K to 5 K	Topology stress test, not PDK signoff

The simulated charge gain is therefore

$$\begin{aligned} A_{Q,\mathrm{sim}} &\equiv \frac{|\Delta V_{\mathrm{sim}}|}{Q_{\mathrm{in}}} \\ &= \frac{0.154\,\mathrm{V}}{10\,\mathrm{fC}} \\ &= 15.4\,\mathrm{mV/fC} \\ &= 1.54 \times 10^{13}\ \mathrm{V/C}. \end{aligned}$$

The ideal CSA gain is

$$A_{Q,\mathrm{ideal}} = \frac{1}{C_f}, \qquad \Delta V_{\mathrm{out,ideal}} = -\frac{Q_{\mathrm{in}}}{C_f}. \quad (22)$$

With $C_f = 10\,\mathrm{fF}$, a 1 fC input would ideally produce $-0.1\,\mathrm{V}$. For the 10 fC pulse used here, the ideal response is

$$\Delta V_{\mathrm{ideal}} = -\frac{Q_{\mathrm{in}}}{C_f} = -1\,\mathrm{V},$$

corresponding to $A_{Q,\mathrm{ideal}} = 100\,\mathrm{mV/fC} = 1.0 \times 10^{14}$ V/C. The simulated charge-gain efficiency is

$$\begin{aligned} \eta_Q &= \frac{|\Delta V_{\mathrm{sim}}|}{|\Delta V_{\mathrm{ideal}}|} \\ &= \frac{0.154}{1.0} = 15.4\%, \end{aligned}$$

so the gain error is 84.6%.

This error is expected, as a simple finite-gain correction is

$$A_{Q,\mathrm{eff}} \approx \frac{1}{C_f}\frac{A_v\beta}{1 + A_v\beta}, \quad (23)$$

where A_v is the OTA open-loop gain and β is the feedback factor. A more useful capacitance-based form is

$$\Delta V_{\mathrm{out}} = -\frac{Q_{\mathrm{in}}}{C_f + (C_s + C_{\mathrm{in}})/(1 + A_v)}. \quad (24)$$

A textbook upper-bound estimate with $g_m \approx 200\,\mu\text{S}$ and $r_o \approx 100\,\text{k}\Omega$ would give $A_v \approx 20$. The extracted room-temperature log is less optimistic: the compressed M_1 branch has $r_o \approx 337.8\,\Omega$, which corresponds to only $g_m r_o \approx 0.068$ if the same g_m scale is used. This confirms that headroom compression, not only capacitance, suppresses loop gain.

Using $C_s = 100\,\text{fF}$, $C_f = 10\,\text{fF}$, and the $A_v \approx 20$ upper-bound gain for a first estimate,

$$\begin{aligned} C_{\text{eff}} &\approx 10\,\text{fF} + \frac{100\,\text{fF}}{1+20} \\ &\approx 14.8\,\text{fF}. \end{aligned}$$

This gives $C_f/C_{\text{eff}} \approx 0.67$. This already shows the problem: with finite loop gain, sensor capacitance takes some of the charge that should go to C_f. The remaining drop to 15.4% comes from extra input/layout capacitance, finite mirror-tail impedance, and bias non-idealities. The CSA is therefore not in the ideal virtual-ground regime. Its main limit is low loop gain,

$$A_v\beta \not\gg 1,$$

which causes input-node motion, charge loss into input capacitance, and gain error.

5.2 Temporal Response and Bandwidth

The transient waveform stays bounded and does not show clear ringing or large overshoot. A separate rise-time extraction was not available, so bandwidth is taken from the AC result instead of estimated from the pulse edges.

The baseline does not fully recover because the reset time constant is

$$\tau_f = R_f C_f = (100\,\text{M}\Omega)(10\,\text{fF}) = 1\,\mu\text{s}.$$

This is ten times longer than the 100 ns pulse period, so the waveform shifts over the pulse train. The timing is mainly limited by input-pair g_m, output/load capacitance, and the feedback network.

Fig. 3 shows the closed-loop AC response.

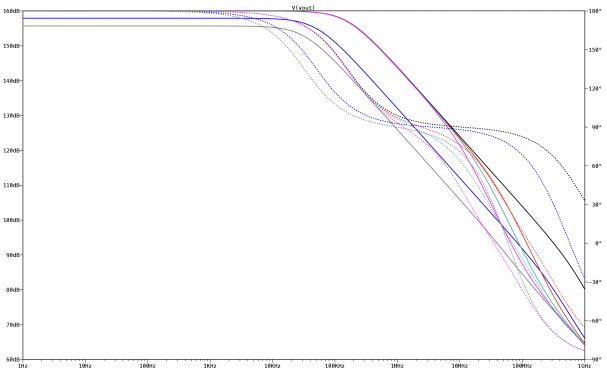


Figure 3: Small-signal AC response. Solid traces show transimpedance magnitude; dashed traces show phase across the temperature sweep.

Since I_2 has unit AC magnitude, `V(vout)` gives the closed-loop transimpedance,

$$Z_t = \frac{V_{\text{out}}}{I_{\text{in}}} \approx R_f. \tag{25}$$

It is not the OTA voltage gain. A value of 159.997 dBΩ equals 99.96 MΩ, close to $R_f = 100\,\text{M}\Omega$. The feedback network is therefore behaving as expected, while finite OTA gain still limits charge gain.

The $-3\,\text{dB}$ bandwidth is defined as

$$|Z_t(j2\pi f_{-3\text{dB}})| = \frac{|Z_{t,\max}|}{\sqrt{2}}, \tag{26}$$

or equivalently

$$\begin{aligned} Z_{t,\text{dB}\Omega}(f_{-3\text{dB}}) &= Z_{t,\max,\text{dB}\Omega} - 20\log_{10}(\sqrt{2}) \\ &\approx Z_{t,\max,\text{dB}\Omega} - 3.010\,\text{dB}. \end{aligned} \tag{27}$$

The room-temperature bandwidth is 158.6 kHz, matching the feedback-pole estimate. Peak Z_t stays near 100 MΩ for most steps. It drops to 155.692 dBΩ, or about 60.90 MΩ, at the 5 K stress point.

Table 7: Closed-Loop Transimpedance and Bandwidth

Step	Temp.	dBΩ	Max. Z_t	$f_{-3\text{dB}}$
1	27 °C	159.997	99.96 MΩ	158.6 kHz
2	−23 °C	157.919	78.69 MΩ	50.8 kHz
3	−73 °C	159.971	99.67 MΩ	154.5 kHz
4	−123 °C	159.976	99.72 MΩ	155.8 kHz
5	−196 °C	159.976	99.72 MΩ	157.0 kHz
6	−268 °C	155.692	60.90 MΩ	32.4 kHz

5.3 Noise Performance

The room-temperature mirror-tail integrated-noise point is

$$\mathrm{ENC}_{\mathrm{sim}} \approx 51.5\ \mathrm{e}^{-}.$$

Output noise is converted to ENC using

$$\mathrm{ENC} \approx \frac{C_f v_{n,\mathrm{out,rms}}}{q_e}, \tag{28}$$

where q_e is the electron charge. The main terms are input thermal noise, flicker noise, load noise, and bias noise. The MOS channel-noise estimate is

$$\overline{i_n^2} \approx 4kT\gamma g_m \Delta f, \tag{29}$$

and the input-referred flicker-noise density is

$$S_{v,1/f}(f) \approx \frac{K_f}{C_{\mathrm{ox}} W L f}. \tag{30}$$

The reset network also has a sampled-noise limit:

$$v_{n,kT/C} \approx \sqrt{\frac{kT}{C_f}}, \qquad \mathrm{ENC}_{kT/C} \approx \frac{C_f v_{n,kT/C}}{q_e}. \tag{31}$$

With $C_f = 10\,\mathrm{fF}$, this gives $v_{n,kT/C} \approx 0.64\,\mathrm{mV}$ and $\mathrm{ENC}_{kT/C} \approx 40\ \mathrm{e}^{-}$ at 300 K. This reset-noise estimate should not be compared directly with the `.noise` result. The `.noise` simulation includes continuous-time amplifier noise, but not sampling or reset action. Thus the room-temperature 51.5 e^{-} integrated-noise value and the lower 16.2 e^{-} value at the 5 K stress point are reasonable within this extraction flow.

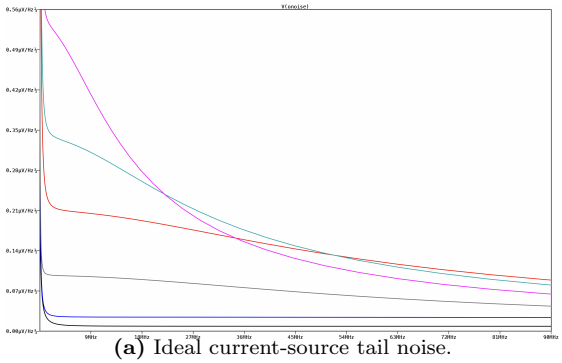
Table 8 compares the extracted current-mirror and ideal-tail values. Both integrated-noise profiles follow the same trend: noise is lowest at the cold extremes, rises toward $-23\,^{\circ}\mathrm{C}$, and then drops at $27\,^{\circ}\mathrm{C}$. The ideal-tail value is slightly lower through the cold sweep, while the two values nearly converge at room temperature. This supports a small current-mirror noise penalty rather than a different noise-temperature trend.

Fig. 4 compares the ideal-tail and mirror-tail output-noise spectra, keeping the visual noise discussion with the extracted ENC table.

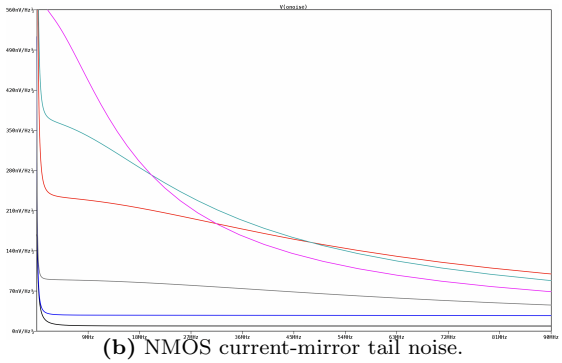
Table 8: Integrated Noise and Step Cross-Check

Temp.	CM v_n	Ideal v_n	CM ENC	CM step	Ideal step
$27\,^{\circ}\mathrm{C}$	0.825	0.828	51.5 e^{-}	24.035	24.465
$-23\,^{\circ}\mathrm{C}$	2.396	2.266	149.6 e^{-}	23.023	23.106
$-73\,^{\circ}\mathrm{C}$	2.209	2.028	137.9 e^{-}	20.095	20.102
$-123\,^{\circ}\mathrm{C}$	1.930	1.738	120.5 e^{-}	13.166	13.107
$-196\,^{\circ}\mathrm{C}$	0.608	0.533	37.9 e^{-}	34.227	33.457
$-268\,^{\circ}\mathrm{C}$	0.260	0.248	16.2 e^{-}	2.279	2.210

Noise and step values are in mV; ENC uses $C_f = 10\,\mathrm{fF}$.



(a) Ideal current-source tail noise.



(b) NMOS current-mirror tail noise.

Figure 4: Output-noise spectral-density comparison. The ideal-source case is the optimistic baseline; the current-mirror case adds low-frequency noise and temperature-dependent roll-off from explicit bias devices.

5.4 Power Consumption

The ideal-tail CSA dissipates

$$P_{\mathrm{DC,ideal}} \approx 36\,\mu\mathrm{W},$$

as given by (19). For the mirror-tail implementation, the core tail branch alone dissipates 37.44 µW, while an unshared 10 µA reference branch raises the total to

$$P_{\mathrm{DC,mirror}} \approx 73.44\,\mu\mathrm{W}.$$

This power is modest at room temperature, but it matters for cold stages and large detector

arrays. It shows the main noise–power trade-off: more bias current can improve g_m and noise, but it also increases cooling load.

5.5 Cryogenic Behavior

At cryogenic temperature, CMOS devices do not behave the same as at room temperature. Mobility can increase and improve g_m, threshold voltage can shift the bias point, and thermal noise falls with kT. These effects can improve gain and noise, but they also make biasing harder.

The cold simulations are qualitative. The models are not calibrated cryogenic compact models, and only first-order parameters such as V_{TO}, K_P, and λ are changed. The sweep therefore shows topology robustness, not absolute low-temperature accuracy.

Fig. 5 and Table 9 show nonmonotonic cold behavior. From room temperature to the 5 K stress point, output excursion falls from 0.771 V to 0.123 V, mean pulse step falls from −154.2 mV to −23.2 mV, and AC bandwidth falls from 158.6 kHz to 32.4 kHz. In this first-order model, bias-point movement and mirror compliance dominate over any simple mobility or thermal-noise benefit.

The extracted step metric in Table 8 also flags a shared transient anomaly. Both bias variants spike near 34 mV at −196 °C, while the other temperatures stay between about 2 mV and 24 mV. Since the spike appears in both circuits, it is more likely a system-level response or model-convergence feature near the liquid-nitrogen point than a current-mirror-only defect.

Table 9: Extracted Transient Compression Across Temperature

Temp.	V_i	V_f	Exc.	Step
27 °C	1.747 V	0.976 V	0.771 V	−154.2 mV
−23 °C	1.674 V	0.874 V	0.800 V	−161.2 mV
−73 °C	1.606 V	0.953 V	0.654 V	−131.2 mV
−123 °C	1.535 V	1.057 V	0.481 V	−96.1 mV
−196 °C	1.456 V	1.165 V	0.296 V	−58.5 mV
−268 °C	1.393 V	1.277 V	0.123 V	−23.2 mV

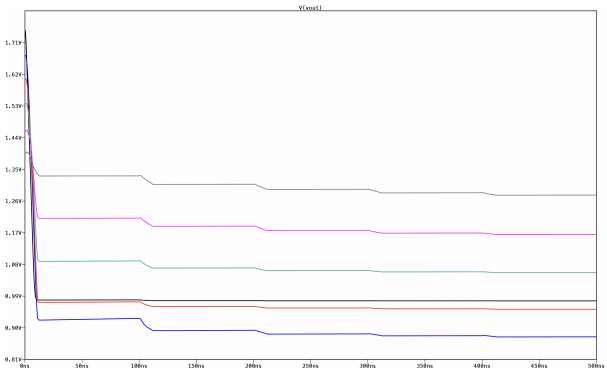


Figure 5: Temperature-swept transient response. The separated traces show baseline movement and pulse-step compression across the sweep.

5.6 Design Trade-offs

The design has four main trade-offs:

- **Gain vs. bandwidth:** smaller C_f gives higher charge gain but is more sensitive to parasitics and finite loop gain; larger C_f is more robust but gives lower gain.
- **Noise vs. power:** higher bias current can lower input-referred noise through larger g_m, but it increases cold-stage power.
- **Accuracy vs. complexity:** higher loop gain would reduce charge-gain error, but cascoding, gain boosting, or regulated biasing make the circuit harder to bias.
- **Integration vs. ideal biasing:** the NMOS mirror tail is easier to integrate, but it adds noise, finite output resistance, compliance limits, and temperature sensitivity.

Table 10 summarizes the ideal-tail and mirror-tail trade-off.

6 Conclusion

A CSA was designed and simulated using a five-transistor OTA, 10 fF feedback capacitor, 100 MΩ reset path, and ±1.8 V supplies. The circuit works as expected: input charge gives repeatable output steps, and the AC response gives about 100 MΩ transimpedance. The

Table 10: Tail-Bias Comparison

Aspect	Ideal tail	NMOS mirror tail
Bias	Ideal sink isolates OTA and feedback	Integrated M_{ref}–M_{tail} bias
Transient	Stepped response with slow reset	Similar integration with baseline shift
Temperature	Intrinsic OTA/feedback drift	Adds current, threshold, and headroom drift
Noise	Optimistic tail-noise baseline	Adds mirror noise and source coupling
Power	36 µW from (19)	73.44 µW from (21)
Role	Topology validation	Bias-assessment before cryogenic PDK modeling

room-temperature mirror-tail ENC from the integrated noise extraction is about 51.5 e^-.

The extracted charge gain is 15.4 mV/fC, while the ideal value is 100 mV/fC. This is 15.4% of ideal. The main reason is finite OTA loop gain with large sensor/input capacitance, so the design is loop-gain limited. The circuit also shows bounded transient behavior, incomplete reset for the 100 ns pulse train, and 158.6 kHz room-temperature bandwidth.

The ideal-tail case dissipates about 36 µW. The mirror-tail case rises to about 73.44 µW when the reference branch is included. The mirror tail is more realistic for integration, but it adds noise, headroom, compliance, and temperature-stability limits. The ideal-tail and current-mirror noise profiles have the same temperature trend, with the ideal tail slightly lower through the cold sweep and nearly convergent at room temperature.

Cryogenic behavior was checked only qualitatively. Low temperature can increase mobility, shift threshold voltage, and reduce thermal noise. In this first-order sweep, it also moves the bias point, compresses the main pulse step, and produces a shared −196 °C small-step anomaly in both bias variants. Full cryogenic models are needed before claiming exact low-temperature performance.

Overall, the results support the CSA topology and show its main limits. Future work should use calibrated cryogenic models, improve bias stability, increase OTA loop gain, replace the ideal reset resistor with an integrated reset element, and reduce noise in the input and bias networks.

References

[1] B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018, doi: 10.1109/JSSC.2017.2737549.

[2] C. Arnaboldi and G. Pessina, "A simple charge sensitive preamplifiers for experiments with a small number of detector channels," in *2007 IEEE Nuclear Science Symposium Conference Record*, Honolulu, HI, USA, 2007, pp. 333–337.

[3] W. M. C. Sansen and Z. Y. Chang, "Limits of low noise performance of detector readout front ends in CMOS technology," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 11, pp. 1375–1382, Nov. 1990, doi: 10.1109/31.62412.

[4] T. J. Paulus, "Charge sensitive preamplifier with capacitive matching," *IEEE Transactions on Nuclear Science*, vol. 32, no. 1, pp. 417–423, Feb. 1985, doi: 10.1109/TNS.1985.4336850.

[5] A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 1007–1018, 2018, doi: 10.1109/JEDS.2018.2817458.

[6] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, Jul. 1995.