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Design and Implementation of Low Power Ring and Johnson Counter using Transistor Resizing Technology by VHDL

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Abstract

In SOC's (System on Chip), numerous systems have been utilized to decrease the dynamic power of by and the large circuit which forces physical limitations or depends intensely on rationale capacity of the circuit. Dynamic power is primarily devoured by clock organize. So methods to lessen the power in clock arrange really limit the dynamic power altogether.There is a prerequisite of supplanting the flip-flop with a more proficient circuit which has same usefulness while accomplishing low power, zone, and vigor to PVT varieties. The pulsed latch system is a standout amongst the most doable answers for this issue. In this work, the execution of the ring counter is enhanced utilizing a pulsed latch method. In rapid and low power VLSI applications where overwhelming pipelining is utilized, there is a necessity of low power edge activated flip-flops. The relocation from flip-flop to pulsed latch has turned out to be an incredible accomplishment in low power VLSI application.The design will be replicated and blended in Xilinx 14.1i ISE.

Keywords: *Counters, Pulsed Latch Technique, VHDL, Xilinx*

INTRODUCTION

Diminishing power dissemination has now turned into a basic plan worry in every electronic framework. The decrease in the supply voltage is the hugest strategy for diminishing the power dissipation due to the quadratic connection between the supply voltage and the dynamic power dissemination. To make up for the execution misfortune because of a lower supply voltage, limit voltage of MOS transistors is additionally lessened. Be that as it may, this causes an expansion in the spillage current. Among all spillage flows, sub edge spillage current is the most predominant. This leakage current will turn into a huge part in the aggregate power dissemination with further downscaling in innovation. Thusly, today a critical research zone in accomplishing low power dissipation is to create successful circuit methods to diminish this spillage ebb and flow that is principally caused by the decrease in the limit voltage of MOS transistors and downscaling in innovation. Innovation scaling has permitted more capacities per unit region, and lower dynamic power dispersal, yet has additionally expanded the spillage control dissemination exponentially. An investigation of patterns dependent on the International Technology Roadmap for Semiconductors (ITRS) demonstrates that the spillage control dissemination is starting to surpass the dynamic power dispersal with the downscaling in innovation age, which is appeared in Fig. 1. Previously, circuit structure strategies and designs overlooked the impacts of spillage control dispersal since it was immaterial in the examination with the dynamic power scattering. Notwithstanding, in subthreshold advances, the job of sub limit spillage control dissemination can't be disregarded and now it has turned out to be

predominant in the general power dispersal in profound submicron and Nano-scale innovations.

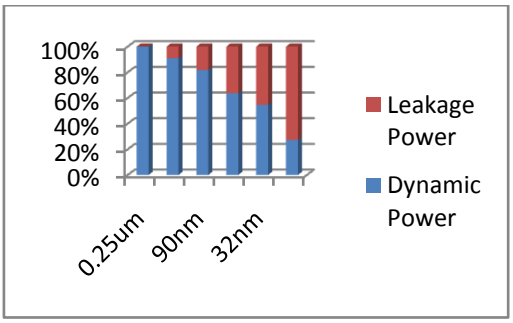


Fig: 1.*Leakage versus dynamic power dissipation trends with technology scaling*

Although add up to control dispersal (dynamic and spillage) the dynamic mode is reduced with the scaling in the supply voltage, further power scattering must be lessened if backup leakage control distribution is controlled, since this spillage power will make up a bigger rate in the general power dispersal with further downsizing in innovation. Low power circuit configuration has developed as an important topic in the present electronics industry. Previously, real worries among designers and researchers for structuring incorporated circuits were on the area, speed, and cost; while optional significance was paid to power dispersal. As of late, notwithstanding, this situation has changed and now creating of various circuit procedures for low power circuit configuration is an imperative research region. For long, low power circuit configuration was just utilized by circuit creators in an explicit area, for example, medical electronic embed where low power scattering was an urgent factor. Low power circuit configuration has now turned into a subject of intrigue, which is apparent from the flood of related exercises in the building and research network. A few elements have added to this pattern. The essential driving variable behind low power circuit configuration is the amazing development and accomplishment of versatile frameworks that are driven by batteries. In these frameworks, low power dissemination is a basic structure concern. Restricted measures of vitality put away inconvenient batteries require broad power the board methods to build their lifetime. Battery life is turning into an item differentiator in battery worked versatile electronic frameworks.

LITERATURE REVIEW

Tanushree Doi and Vandana Niranjan, "Low power and high performance ring counter using pulsed latch technique", 2016 [1], reducing power consumption is a crucial task for any circuits.

Guang-Ping Xiang, Ji-Zhong Shen, Xue-Xiang Wu and Liang Geng, "Design of a Low-Power Pulse Triggered Flip-Flop with Conditional Clock Technique", 2013 [3], flip-flops are basic sequential elements in digitalcircuits and they have a deep impact on the performance of thecircuits. In order to reduce the redundant transitions at internalnodes of the flip-flop, a conditional clock technique is proposed, and afterward, a restrictive clock pulse-triggered flip-flop (CCFF) in light of this strategy is structured. In CCFF, the clock is blocked when the info stays unaltered so the interior hubs won't switch with the clock, which decreases the power utilization viably. In light of the TSMC 0.18µm innovation, the post-format reenactment results demonstrate that the proposed CCFF has a conspicuous favorable position in power utilization when the information exchanging movement factor is underneath half as contrasted and other best in class beat activated flip-flops, and the power savingis more than 50% when the activity factor is 10%.SandeepSriram, Arun Ramnath Ramani, Haiqing Nan, Hojoon Lee, Ken Choi, "A Novel Dual Edge Triggered Near-Threshold State Retentive Latch Design", 2011 [4], this paper proposes

another double edge activated close edge state-retentive hook for low-control applications. The proposed circuit utilizes control gating amid the rest or inactive mode consequently evading spillage yet at the same time holding its state. It utilizes a double edge activated heartbeat which is a heartbeat trigger at both the rising and falling edges of the clock. The circuit utilized low Vth Devices just and henceforth can work at a Vdd as low as 0.5 V. The circuit was reproduced utilizing HSPICE at 45nm innovation.

IMPLEMENTED METHODOLOGY

There are various methods to reduce power dissipation from the circuit, these are explained as below:

Transistor Sizing: To lessen the dynamic power, the widths of transistors are diminished utilizing low dimension models that relate the power utilization to width [6-8]. Yet, lessening the width builds the deferral. The coherent exertion of the entryway additionally increments. The coherent exertion is the proportion of the info capacitance of an offered entryway to that of an inverter fit for conveying a similar yield current. It is liked to have gates with low sensible effort since these will be quicker and subsequently suitable widths must be decided for the P and N transistors. Subsequently, just transistors that lie far from basic ways of the circuit are the best possibility for transistor measuring strategy. For the most part, with every transistor, an average postponement is related which changes relying upon how to shut that transistor is to the basic way and after that calculation are connected that attempt to scale every transistor to be as little as conceivable delay.

Transistor Reordering: The arrangement of transistors in a circuit influences energy utilization. In transistor reordering procedure transistors are revamped to limit their exchanging movement. One of the core values here is to put transistors closer to circuit's yield on the off chance that they switch much of the time with the end goal to keep a domino impact where the changing action from one transistor triggers numerous different transistors that reason across the board control dispersal. However, this requires effective procedures to decide how every now and again unique transistor is probably going to switch.

Half Frequency and Half Swing Clocks: Customarily, hardware occasions, for example, enlist document composes happen at the rising edge of the clock. Half recurrence clocks synchronize occasions utilizing the two edges and in this way switch at a large portion of the speed of normal tickers along these lines lessening the clock exchanging power considerably. Diminished swing clocks utilize a lessened voltage swing along these lines decreasing the power quadratically.

Logic Gate Restructuring: A circuit can be worked with rationale gates from multiple points of view. The course of action of gates and info signals influence the power utilization. For instance, a 4-information AND gate can be actualized utilizing a chain usage and a tree execution. For this situation, an anchor execution may prompt diminished unique power because of lessened exchanging likelihood thana tree implementation. However, chain implementations do not necessarily save more energy than tree implementations because of the increased propagation delay. Additionally, glitches or misleading changes that happen when a gate does not get the inputs of its contributions in the meantime are more typical in chain executions than tree usage. This is on the grounds that, distinctive signals travel along various ways with generally changing way delays. One answer for decrease glitches is to change

the topology so the ways have comparative delays. This arrangement known as path adjusting regularly transformschain implementations into tree implementations. Another solution known as retiming involves inserting flip flops or registers to slow down and thereby synchronize the signals that pass along different paths but reconverted to the same gate.

4-bit Ring Counter: Ring counter is a kind of counter composed of a sort of roundabout shift enroll. The output of the last shift enroll is fed to the contribution of the principal enlist. 4-bit ring counter is comprised of four flip slump (D-FF).

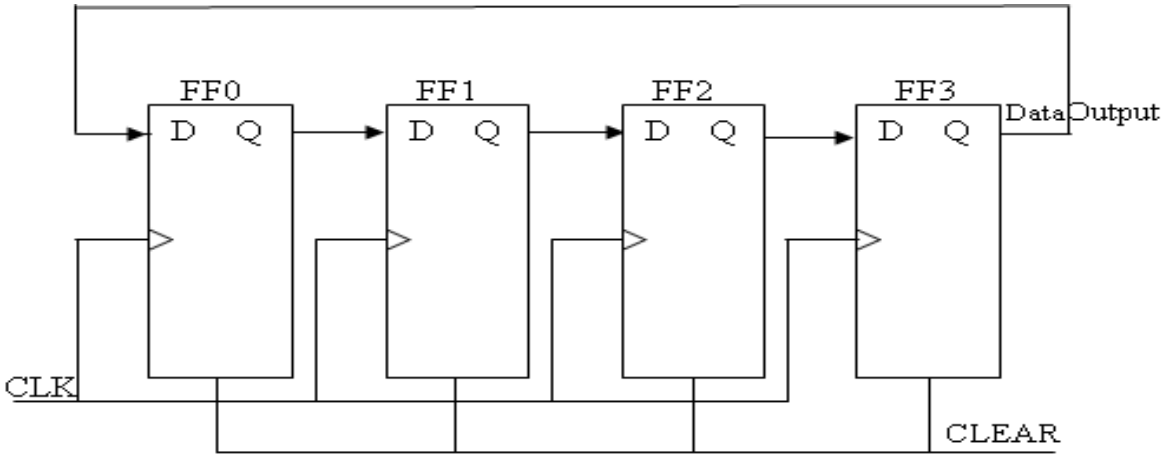


Fig: 2.*Block Diagram of 4-bit Ring Counter*

4-bit Johnson Counter: A twisted ring counter, likewise called switch-tail ring counter, strolling ring counter, Johnson counter associates the supplement of the yield of the last shift register to the contribution of the principal register and courses a flood of ones pursued by zeros around the ring. For instance, in a 4-register counter, with introductory enlist estimations of 0000, the rehashing design is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000...

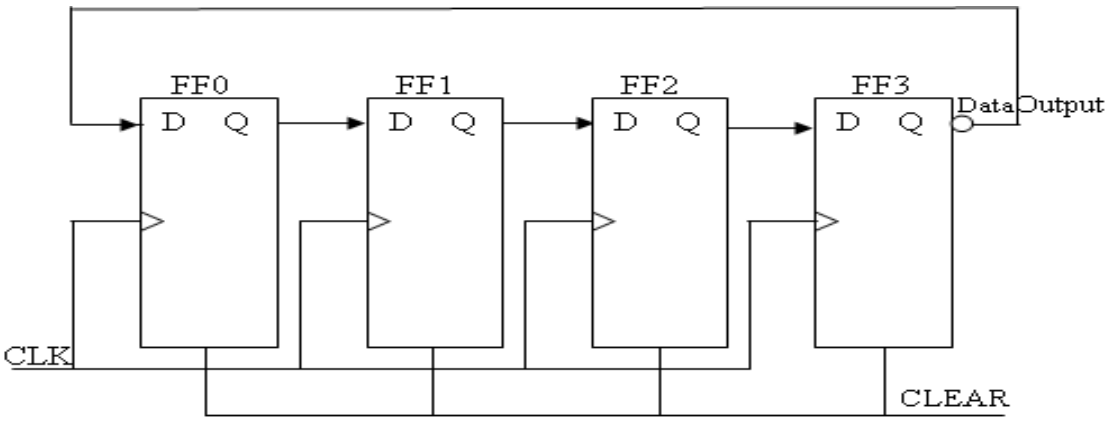
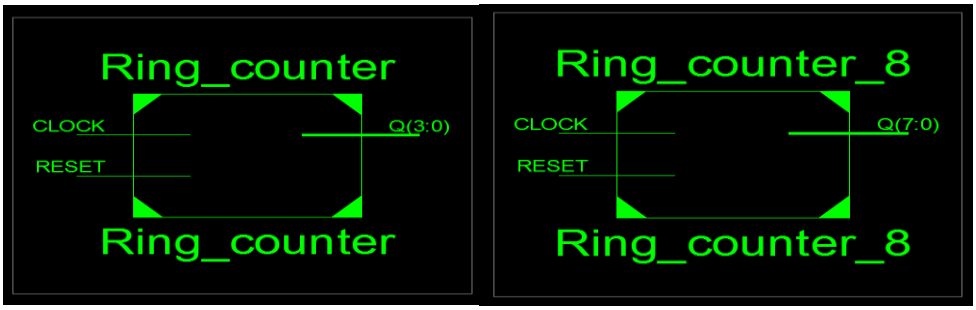


Fig: 3.*Block Diagram of 4-bit Johnson Counter*

SIMULATION AND RESULT

All types of counter i.e. ring counter and Johnson counter are simulated on Xilinx software with different parameter i.e. resistor transfer level (RTL), test bench waveform, synthesis result and timing summary.



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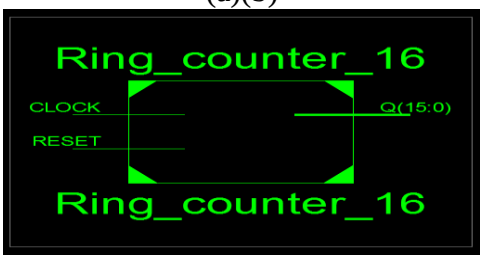


(c)

Fig: 4. (a,b,c)*RTL of 4, 8 and 16 bit Ring Counter*

Table: 1.*Device Utilization Summary of Ring Counter*

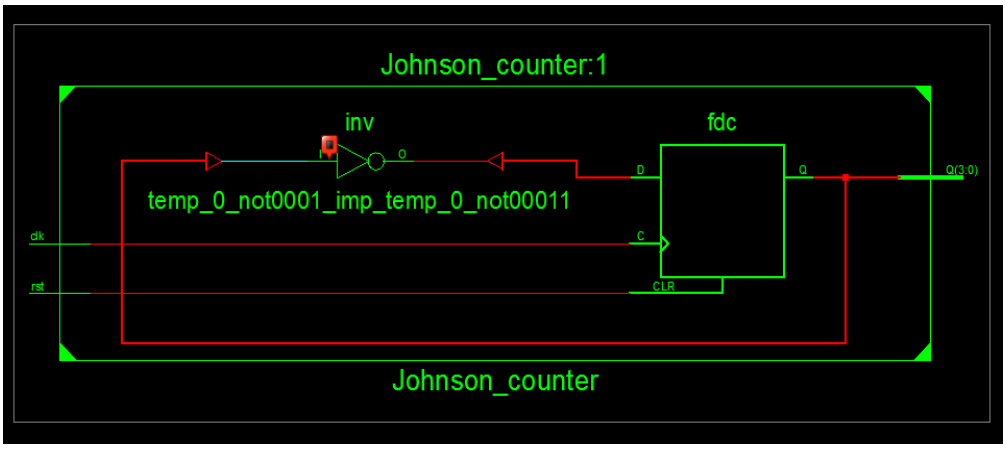
Number of Bits	Number of Slice	Slice Flip Flop	IOBs	GCLKs	Average Fan-Out	Memory Usage (KB)
4-bit	4	2	6	1	2.40	200036
8-bit	8	4	10	1	3.73	200420
16-bit	16	9	18	1	2.48	200356

Table: 2.*Delay Summary of Ring Counter for Various FPGA*

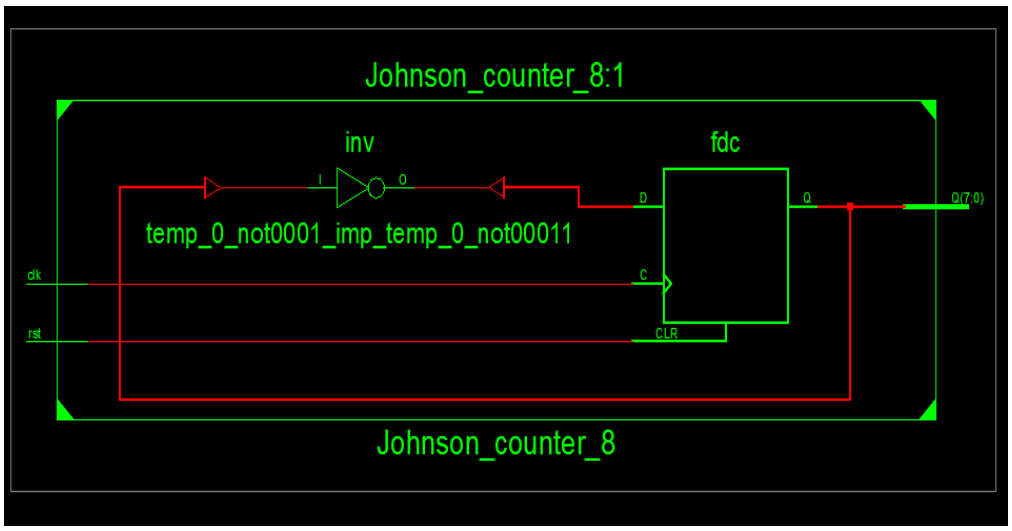
Number of Bits	Delay (nSec) (Existing Method) [10]	Delay (nSec)			
		Spartan 3	Virtex 4	Spartan 6	Virtex 6
4	6.641	**0.538**	1.893	1.147	0.781
8	-	**0.614**	1.90	2.071	1.132
16	-	1.743	1.930	1.657	**1.016**

Table: 3.*Power Dissipation Summary of Ring Counter for Various FPGA*

Number of Bits	Power Dissipation (W)			
	Spartan 3	Virtex 4	Spartan 6	Virtex 6
4	0.027	0.171	**0.017**	1.294



(a)



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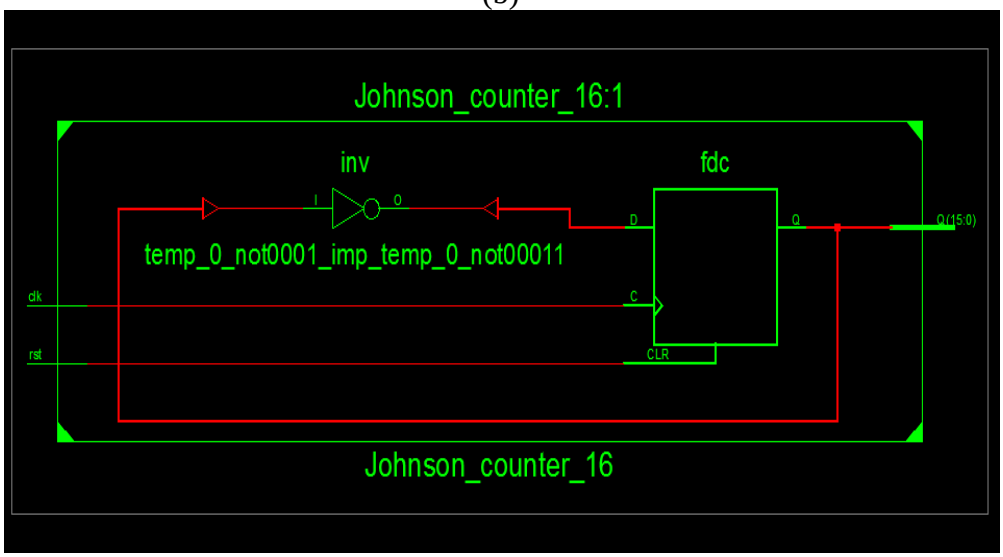

(c)

Fig: 5. (a,b,c)*RTL of 4, 8 and 16 bit Johnson Counter*

Table: 4.*Device Utilization Summary of Johnson Counter*

Number of Bits	Number of Slice	Slice Flip Flop	IOBs	GCLKs	Average Fan-Out	Memory Usage (KB)
4-bit	4	2	6	1	2.40	200100
8-bit	8	4	10	1	2.67	200356
16-bit	16	8	18	1	2.82	200740

Table: 5.*Delay Summary of Johnson Counter for Various FPGA*

Number of Bits	Delay (nSec) (Existing Method) [10]	Delay (nSec)			
		Spartan 3	Virtex 4	Spartan 6	Virtex 6
4	6.236	**0.538**	1.893	1.311	0.781
8	-	**0.614**	1.900	1.697	0.826
16	-	1.793	1.933	1.316	**0.810**

Table:6.*Power Dissipation Summary of Johnson Counter for Various FPGA*

Number of Bits	Power Dissipation (W)			
	Spartan 3	Virtex 4	Spartan 6	Virtex 6
4	0.028	0.165	**0.016**	1.130

CONCLUSION

From the analysis and synthesis of ring and Johnson counters it is clear that the design with self-made transistors is more effective as far as zone.So this design can be implemented in the applications where area reduction is the main consideration. A comparative analysis of counters shows that in terms of number of slices flip flop, occupied flip flops, input output buffer, gate clock, average fan-out and memory used for implementation.

In this paper, an optimized 4-bit, 8-bit, and 16-bit ring counter and Johnson counter using D flip flop is implemented. It is made efficient in terms of maximum combinational path delay (MCPD). The proposed design show the superior performance in its speed as the propagation delay in proposed counter is found lowest0.538 nanoseconds for Spartan 3. Power dissipation for both counters is lowest for Spartan 6 FPGA which uses 45 nm low power copper process technologies that delivers optimal balance of cost, power and performance. By using this type of FPGA (Spartan 6), we can reduce the power consumption and dissipation as the transistor size is reduced in this technology.

Same counters can be implemented by transistor reordering and reducing the frequency of gate clock switching power by half. Another method to reduce the power can be implemented i.e. by using multiple supply voltage design.

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