A 100-140 GHz SiGe-BiCMOS Sub-Harmonic Down-Converter Mixer

Neda Seyedhosseinzadeh[1,2], Abdolreza Nabavi[2], Sona Carpenter[1], Zhongxia Simon He[1],
Mingquan Bao[3], Herbert Zirath[1,3]

[1]*MC2 Department, Chalmers University of Technology, Göteborg SE-412 96, Sweden*
[2]*ECE Department, Tarbiat Modares University, Tehran 14115-139, Iran*
[3]*Ericsson Research, Ericsson AB, Göteborg SE-417 56, Sweden*
Email: n.seyedhosseinzadeh@modares.ac.ir

***Abstract*— This paper demonstrates a wideband, sub-harmonic down converting mixer using a commercial 130-nm SiGe-BiCMOS technology. The mixer adopts a frequency doubling LO-stage, a differential switched-transconductance RF-stage, on-chip LO and RF baluns, and two emitter-follower buffer-stages. The measured results exhibit a maximum conversion gain up to 2.6 dB over the frequency range of 100 to 140 GHz with a LO power of 5 dBm. The mixer achieves an input referred 1-dB compression point of -7.2 dBm, with a DC power of 46.3 mW, including 26.7 mW for buffer-stages. It demonstrates also up to 12 GHz 3-dB IF bandwidth, which to the authors' best knowledge, is the highest obtained among active sub-harmonic mixers operating above 100 GHz. The chip occupies 0.4 mm^2, including pads.**

Keywords*— *SiGe MMICs, millimeter-wave, above 100 GHz, sub-harmonic mixer (SHM), down-converter, broadband circuits.

I. Introduction

The sub-harmonic mixer (SHM) is an attractive candidate for frequency conversion in micro-wave and millimeter-wave transceivers [1]. It requires only a fraction of the local oscillator (LO) frequency compared to a fundamental mixer and increases the LO-to-RF isolation significantly. Unfortunately, most of the high frequency SHMs above 100 GHz have relatively conversion loss, which imposes severe noise figure (NF), gain and linearity requirements on the low noise amplifier and following building blocks of receiver chain [2], [3], [4]. On the other hand, to realize a high gain amplifier at the RF or IF side, usually three to five stages are utilized, where it burdens the power budget of a low power system. Therefore, implementing a millimeter-wave down-converter SHM is challenging with respect to conversion gain, bandwidth, NF and linearity requirements.

Recently, several efforts have been done in literature to develop millimeter-wave SHMs with improved performance. In [5], a transformer-based gm-boosting SHM is presented operating at 79 GHz, where a conversion gain of 1.6 dB and NF of 13 dB is achieved with a LO power of -5 dBm. This technique boosts the RF transconductance without additional power consumption. However, it is not appropriate for operating frequencies above 100 GHz due to the additional loss of transformer network. In [6], a modified Gilbert-cell based on two stacked switching quads is reported for 122 GHz. This topology shows better conversion gain compared to a Gilbert-cell configuration with parallel transistor pairs, which is adopted in [7] due to its higher operating frequency. However, as the frequency goes up, the maximum conversion gain and accordingly minimum NF occurs by non-quadrature LO signals due to the delay produced in RF path from the emitter to the collector of the switching stage [8]. Hence, a novel hybrid with an arbitrary phase shift is needed in order to provide an optimum LO phase distribution. Furthermore, owing to the several stacked transistors, a larger supply voltage is required to avoid the compression of the output voltage amplitude, which inevitably influences the power consumption of whole circuit. In [4], [9] a two-stage sub-harmonically base-pumped transconducance mixer is introduced that reaches to a maximum -1 dB and 9 dB conversion gain at D-band and V-band using a -1 dBm and 2 dBm LO power, respectively. This type of mixer utilizes the internal mixing of RF signal with the second- or higher-order harmonics of the LO signal, generated by nonlinearities of transistor itself. It features a better gain performance compared to a passive SHM [10], and a decent NF, however it has rather high conversion loss in sub-harmonic operation and requires a lower base bias along with a typically large driving LO power to fulfil the optimum conduction duty cycle [4]. Therefore, a power hungry IF buffer amplifier is usually exploited at the output, which correspondingly leads to a high power consumption, e.g. 120 mW [4] and 262 mW [9].

This paper presents a high conversion gain and a broadband transconductance SHM based on a bottom-LO frequency doubler to operate at 100 to 140 GHz frequency range. The aim of this work is to benchmark the performance of this topology above 100 GHz in a 130-nm SiGe-BiCMOS technology for the first time. To improve the gain-bandwidth and linearity characteristics of mixer, several techniques and approaches have been employed and followed from different publications.

II. Circuit Topology and Realization

The idea of a transconductace SHM with a bottom-LO frequency doubler was first demonstrated at 930 MHz [11] and is well described in [12]. Unlike a standard Gilbert-cell topology which implements the mixer function by a trans-

This work was supported by the EU's Horizon 2020 research and innovation programme (M3TERA)(644039).

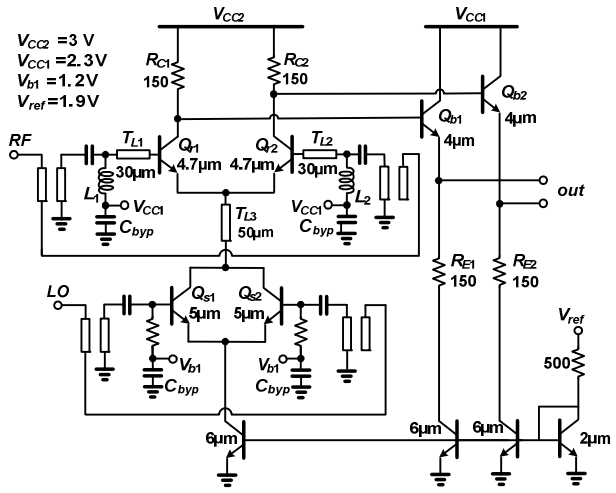

Fig. 1. Simplified circuit schematic of the single-balanced broadband SHM.

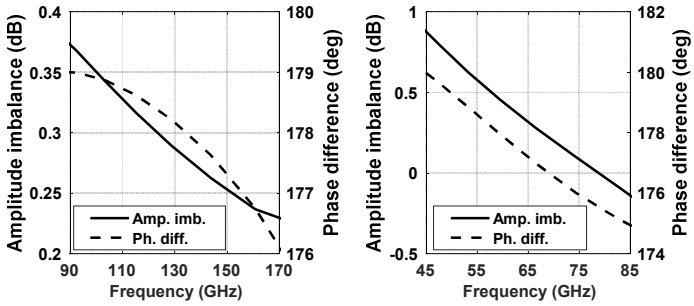

Fig. 2. Simulated amplitude imbalance and phase difference of (a) RF (b) LO Marchand baluns.

conductance device followed by current commutating switching; this scheme achieves the same functionality by the switched transconductors. One of the main advantages of this structure is the high LO-to-RF and high LO-to-IF isolation. This is because the LO signal appears in common-mode at both RF and IF ports.

Fig. 1 depicts the simplified schematic diagram of the designed wideband SHM along with the emitter follower buffer-stages. The SHM is implemented in a single balanced topology, driven by a differential LO- and RF-scheme. It consists of a push-push frequency doubler at LO-stage (Q_{s1}/Q_{s2}) and a differential switched-transconductance RF-stage (Q_{r1}/Q_{r2}). The LO-stage converts input differential LO voltage into current, which controls the transconductances of the RF-stage efficiently at twice the LO frequency. Consequently, two out-of-phase subharmonic IF components (f_{IF}=f_{RF}-2f_{LO}) are produced and conveyed to the output through resistive loads. It is worthy to note that the mixing core operates in a fundamental mode, where it has a better conversion gain than that in a sub-harmonic mode [4].

The output buffer-stage provides a 50 Ω matching over a broad bandwidth and also forms a low-pass filter to enhance the RF-to-IF isolation at the output ports.

Both mixer core and buffers are biased with current sources, regulated by a reference current. Subsequently, a high current or a low current can be injected into the circuit, which accordingly offers a high linearity or moderate linearity operation. Regarding low break-down voltage, two series resistors (R_{E1}/R_{E2}) are also placed at the collector of output current sources to prevent transistor damage under high current levels.

In order to achieve a wideband RF operation, Marchand baluns with broadside coupled lines are applied at both RF and LO ports [13]. A further improvement is done on baluns by removing the ground layer (M4) under the signal lines resulting to more compact layout and lower insertion loss [14]. Fig. 2 exhibits the simulated performance of each balun in terms of phase and amplitude imbalance, while the minimum loss is -1.3 dB and -2 dB, for RF and LO signals, respectively.

The high frequency RF signal is applied through a shunt spiral inductor (L_1/L_2) accompanied by a series line (TL_1/TL_2) to transform the low input impedance of transistor base to a higher value [3]. To do this, custom inductors are designed with one-turn symmetric structure on M6, where the simulated value of each inductor is about 20 pH with the maximum quality factor of 12.9 at 173 GHz, and the self-resonance frequency of 355 GHz.

To increase the LO swing across the emitter terminal of the RF transistors, a tuning-out series line (TL_3) is adopted between RF and LO stages, implementing a π-network [15]. This network provides a higher conversion gain at lower LO powers and slightly enhances the RF-bandwidth of the mixer.

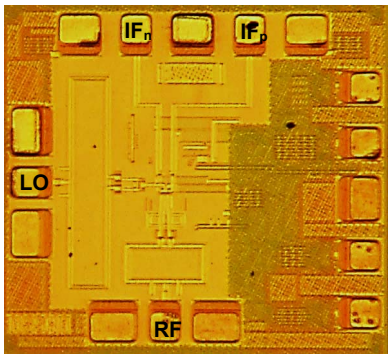

Fig. 3. chip photograph, active area: 0.215 mm^2, total area: 0.4 mm^2.

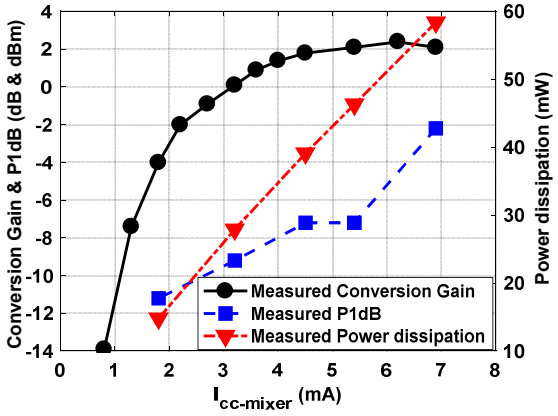

Fig. 4. Measured conversion gain, input P1dB and total power dissipation versus collector current of mixer core, I_{cc_mixer} (f_{LO}=57.5 GHz, f_{RF}=113 GHz).

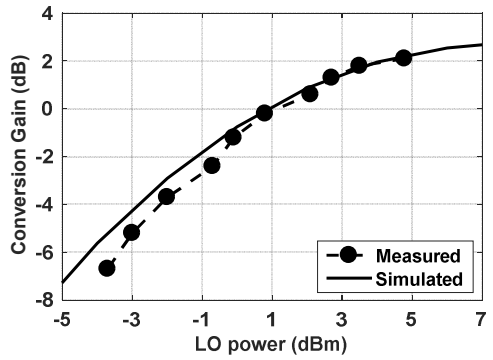

Fig. 5. Measured and simulated conversion gain as a function of LO-power with a fixed LO and RF frequency of 57.5 GHz and 113 GHz, respectively.

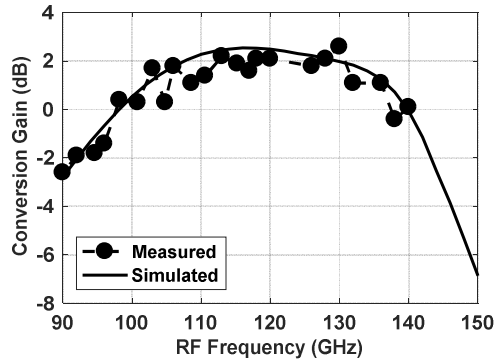

Fig. 6. Measured and simulated conversion gain versus RF frequency at a fixed IF frequency of 2 GHz.

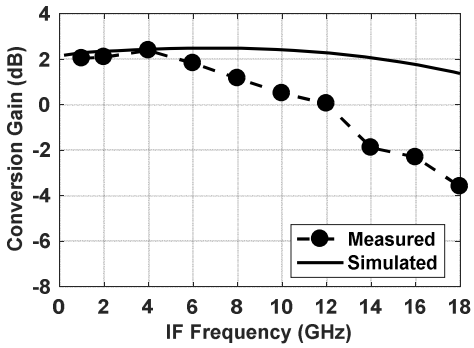

Fig. 7. Measured and simulated conversion gain versus IF frequency. The LO is fixed at 61 GHz and RF is swept from 102 to 121 GHz.

Finally, the collector loads (R_{C1}/R_{C2}) incorporate 150 Ω resistors to provide a broadband IF response under a low supply voltage.

All passive components are simulated with a 2.5D planar EM-simulator using Sonnet/Cadence interface. In both RF and LO ports, the signal pads are shielded from the substrate by a grounded layer and its capacitance is also included in the simulation results.

III. Mixer Measurement

A SHM circuit is designed and fabricated in a 130-nm SiGe-BiCMOS process. This technology features high speed npn HBTs with maximum f_t/f_{max} of 250 GHz/370 GHz and BV_{CEO} = 1.5 V. The chip photograph is shown in Fig. 3. It occupies 600 µm × 670 µm, while the active chip area including RF and LO baluns is only 500 µm × 430 µm. To characterize the mixer performance, on-wafer measurements are carried out. The RF signal is generated and calibrated using a Keysight N5242A microwave network analyzer from 10 MHz to 26.5 GHz and a N5262BW08, WR 8.0 based frequency converter to extend the frequency range from 90 to 140 GHz. The LO signal is provided from an Agilent E8257D, 250 KHz to 67 GHz PSG signal generator. A Rohde and Schwartz spectrum analyzer is used to measure the IF signal.

Fig. 4 shows the measured conversion gain, input referred P1dB, and the total power consumption of circuit as a function of collector current in the mixer core ($I_{cc\text{-}mixer}$), while the LO-power is fixed at 5 dBm. As can be seen, the conversion gain enhances with increasing the collector current of mixer core, which is controlled by a reference voltage (V_{ref}) until it reaches to maximum value of 2.4 dB at $I_{cc\text{-}mixer}$ = 6.2 mA. Consequently, the input P1dB also improves and the total power consumption rapidly growths due to the high current levels of buffer-stages, where a -2.2 dBm input power at a 1-dB compression point is achieved with a power dissipation of 58.4 mW.

The variation of mixer conversion gain versus LO power is shown in Fig. 5 at a LO frequency of 57.5 GHz, RF frequency of 113 GHz and IF frequency of 2 GHz. A good agreement is obtained between simulation and measurement results. It demonstrates a positive gain from LO input power of +1 dBm. The LO frequency is swept from 46 to 68 GHz with an input power of 5 dBm, while the IF frequency is fixed at 2 GHz. As shown in Fig. 6, an RF frequency range from 98 to 140 GHz is achieved with a conversion gain of -0.4 to 2.6 dB, which represents more than 40 GHz 3-dB bandwidth. The 2LO-to-RF isolation is better than 45 dB over the entire bandwidth.

The measured IF response at LO frequency equal to 61 GHz is shown in Fig. 7. The results indicate a flat conversion gain, and 3-dB IF bandwidth is 12 GHz from 1 to 13 GHz. This is the widest IF bandwidth among silicon-based active sub-harmonic mixers operating above 100 GHz.

Finally, Fig. 8 describes the output power at 2 GHz versus

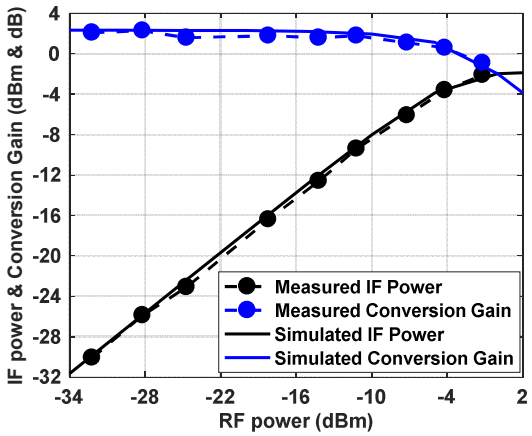

Fig. 8. Measured IF output power and conversion gain as a function of the RF input power at a fixed RF and IF frequency of 113 GHz and 2 GHz, respectively.

TABLE I. PERFORMANCE SUMMARY OF 2X SHMS

Ref.	Topology	Process	RF (GHz)	CG_p (dB)	IF (GHz)	P_{1dB} (dBm)	OP_{1dB} (dBm)	2LO-RF Iso. (dB)	P_{LO} (dBm)	P_{DC} (mW)	Area (mm^2)
[2]	leveled Gilbert	90nm CMOS	30-100	0	0.1	-8.6	-9.6	47	10	58	0.35
[3]	resist.+ IF Amp.	32 nm SOI CMOS	158-182	+8**	1-6	-	-	-	4	74	0.75
[4]	trans.+ IF Amp.	250 nm InP DHBT	110-170	-1	5	-	-	40	-1	262	0.825
[5]	gm-boost Gilbert	65 nm CMOS	75-81	3.4	0.5	-16.2	-15.6	38	-5	12	0.31
[6]	stacked Gilbert	130 nm SiGe:C	125-129	4	-	-	-	-	9	89.1	-
[9]	trans.+ IF Amp.	250 nm InP DHBT	55-67	6	0.25-3	-2	3	40	5	120	0.63
[16]	Amp. + APDP	90 nm CMOS	33-103	-0.5	1	-3	-5++	60	10	24.5	0.49
This Work	**bottom-LO trans.**	**130 nm SiGe**	**98-140**	**2.6**	**1-13**	**-7.2**	**-6**	**45**	**5**	**46.3**	**0.4**

CG_p = peak conversion gain, **simulated stand-alone mixer gain is -23 dB, ++ by estimated mixer loss, resist=resistive, Amp=amplifier trans=transconductance, APDP = anti-parallel diode pair

input power at RF frequency of 113 GHz. It can be seen, the circuit has a 1-dB compression at –7.2 dBm input power. The total power consumption is only 46.3 mW.

The simulated single-side band NF of the mixer is below 16 dB over the entire IF bandwidth, which is decent enough to be preceded by an LNA with a moderate NF.

In Table I, the performance of the presented SHM and other published results in the literature are listed. It can be seen that our SHM achieves competitive conversion gain, and record IF bandwidth with a good linearity.

IV. CONCLUSIONS

An F-band bottom-LO down-converter transconductance SHM is designed and fabricated in a 130-nm SiGe-BiCMOS process for broadband applications. This mixer features a high conversion gain and good linearity among the above 100 GHz active mixers without any amplifier. It demonstrates a wide IF bandwidth. In addition, the SHM has a good port-to-port isolation and a relatively small chip size.

ACKNOWLEDGMENT

The authors would like to thank K. Aufinger and F. Dielacher at Infineon for their support.

REFERENCES

[1] H. Zirath, "A subharmonically pumped resistive dual-HEMT-mixer", *IEEE MTT-S Int. Microw. Symp. (IMS) Dig*., pp. 875-878, Jul. 1991.

[2] K. J. Tsai, H. Yang, T. Huang, and H. Wang, "A 30–100 GHz wideband sub-harmonic active mixer in 90 nm CMOS technology," *IEEE Microwave and Components Letters*, vol. 18, no. 8, pp. 554–556, Aug. 2008.

[3] Dristy Parveg, Mikko Varonen, Pekka Kangaslahti, Amirreza Safaripour, Ali Hajimiri, Tero Tikka, Todd Gaier, and Kari A. I. Halonen, "CMOS I/Q subharmonic mixer for millimeter-wave atmospheric remote sensing," *IEEE Microwave and Components Letters*, vol. 26, no. 4, pp. 285–288, Apr. 2016.

[4] Y. Yan, M. Bao, S. E. Gunnarsson, V. Vassilev and H. Zirath, "A 110-170-GHz multi-mode transconductance mixer in 250 nm InP DHBT technology," *IEEE Trans. Microw. Theory Techn*., vol. 63, no. 9, pp. 2897–2904, Sep. 2015.

[5] J. Jang, J.T. Oh and S. Hong, "A 79 GHz gm-boosted sub-harmonic mixer with high conversion gain in 65nm CMOS," in *Proc. IEEE Symp. Radio Freq. Integr. Circuits*, pp. 11-14, May 2015.

[6] K. Schmalz, W. Winkler, J. Borngraber, W. Debski, B. Heinemann, and C. Scheytt, "A subharmonic receiver in SiGe technology for 122 GHz sensor applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1644–1656, Sep. 2010.

[7] Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, M. Urteaga, R. Pierson, and H. Zirath, "340 GHz integrated receiver in 250 nm InP DHBT technology," *IEEE Trans. THz Sci. Technol.*, vol. 2, no. 3, pp. 306–314, May 2012.

[8] Y. Zhao, E. Öjefors, K. Aufinger, T. F. Meister, U. R. Pfeiffer, "A 160-GHz subharmonic transmitter and receiver chipset in an SiGe HBT technology, " *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3286-3299, Oct. 2012.

[9] M. Bao, Y. Li, and H. Zirath, "A V-band high linearity two-stage subharmonically pumped mixer," in *Proc. IEEE Eur. Microw. Integr. Circuits*, pp. 162–165, Oct. 2014.

[10] Y. Mao, K. Schmalz, J. Borngraber, J. C. Scheytt, "245-GHz LNA, mixer, and subharmonic receiver in SiGe technology, " *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 3823-3833, Dec. 2012

[11] Z. Zhang, Z. Chen, L. Tsui and J. Lau, "A 930 MHz CMOS DC-offset-free direct-conversion 4-FSK receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig.*, pp.290-291, Feb. 2001.

[12] K. Nimmagadda and G. M. Rebeiz, "A 1.9 GHz double-balanced subharmonic mixer for direct conversion receivers," in *Proc. IEEE Symp. Radio Freq. Integr. Circuits*, pp. 253–256, May 2001

[13] S. Carpenter, M. Abbasi, and H. Zirath, "Fully integrated D-Band direct carrier quadrature (I/Q) modulator and demodulator circuits in InP DHBT technology," *IEEE Trans. Microw. Theory Techn*., vol. 63, no. 5, pp. 1666–1674, May. 2015.

[14] I. Song, R. L. Schmid, D. C. Howard, S. Jung, and J. D. Cressler, "A 34-110 GHz wideband, asymmetric, aroadside-couple marchand Balun in 180 nm SiGe BiCMOS technology," *IEEE MTT-S Int. Microw. Symp. (IMS) Dig.,* pp. 1-4, Jun 2014.

[15] B. R. Jackson and C. E. Saavedra, "A CMOS Ku band 4x subharmonic mixer," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1351–1359, Jun 2008.

[16] S. H. Hung, K. W. Cheng, and Y. H. Wang, "An ultra-broadband subharmonic mixer with distributed amplifier using 90-nm CMOS technology", *IEEE Trans. Microwave Theory & Tech*., vol. 61, no. 10, pp. 3650-3657, Oct. 2013.