INTERDIGITATED BACK CONTACT SILICON HETEROJUNCTION SOLAR CELLS FEATURING AN INTERBAND TUNNEL JUNCTION ENABLING SIMPLIFIED PROCESSING

B. Paviet-Salomon[1,*], A. Tomasi[2], D. Lachenal[3], N. Badel[1], G. Christmann[1], L. Barraud[1], A. Descoeudres[1], J. Geissbühler[1], A. Faes[1], Q. Jeangros[2], J. P. Seif[2], S. Nicolay[1], B. Strahm[3], S. De Wolf[2,**], C. Ballif[1,2] and M. Despeisse[1]

[1]CSEM, PV-Center, Rue Jaquet-Droz 1, CH-2002 Neuchâtel, Switzerland

[2]Photovoltaics and Thin-Film Electronics Laboratory, IMT, EPFL, Maladière 71B, CH-2000 Neuchâtel, Switzerland

[3]Meyer Burger Research SA, Rouges-Terres 61, CH-2022 Hauterive, Switzerland

[*]Corresponding author: Bertrand Paviet-Salomon, CSEM PV-Center, Rue Jaquet-Droz 1, CH-2002 Neuchâtel, Switzerland; E-mail: bertrand.paviet-salomon@csem.ch; Tel: +41 32 720 54 71

[**]Now with King Abdullah University of Science and Technology (KAUST), KAUST Solar Center (KSC), Thuwal, 23955-6900, Saudi Arabia

Abstract – This paper reports on the development of an innovative back-contacted crystalline silicon solar cell with passivating contacts featuring an interband tunnel junction at its electron-collecting contacts. In this novel architecture, named "tunnel-IBC", both the hole collector patterning and its alignment to the electron collector are eliminated, thus drastically simplifying the process flow. However, two prerequisites have to be fulfilled for such devices to work efficiently, namely (i) lossless carrier transport through the tunnel junction and (ii) low lateral conductance within the hole collector in order to avoid shunts with the neighboring electron-collecting regions. We meet these two contrasting requirements by exploiting the anisotropic and substrate-dependent growth mechanism of n- and p-type hydrogenated nano-crystalline silicon layers. We investigate the influence of the deposition temperature and the doping gas concentration on the structural and the selectivity properties of these layers. Eventually, tunnel-IBC devices integrating hydrogenated nano-crystalline silicon layers have been processed and demonstrate up to 23.9 % conversion efficiency.

Keywords: passivating contacts; interdigitated back contact; tunnel junction; silicon solar cells.

1. INTRODUCTION

As the efficiency of single junction crystalline silicon-based solar cells steadily approaches their theoretical limit (Richter et al., 2013), establishing new records increasingly requires to diligently identify and mitigate the remaining optical and electrical loss mechanisms. Along these lines, the combination of a back-contacted design with passivating contacts has been anticipated in the last couple of years to be the ideal solar cell structure, as it combines a shadow loss-free front side – hence a high short-circuit current density – together with a high

open-circuit voltage enabled by well-passivated contacts. In this context, Panasonic, Japan, reported in 2014 on a 25.6 %-efficient back-contacted crystalline silicon solar cell using an amorphous/crystalline silicon heterojunction (SHJ) as passivating contact materials (Masuko et al., 2014), hence breaking the long lasting record of the UNSW PERC solar cell (Zhao et al., 1998) and convincingly demonstrating the potential of back-contacted devices with passivating contacts. Soon afterwards, still using hydrogenated amorphous silicon (*a*-Si:H) as passivating materials, Kaneka, Japan, successively released in 2016 and 2017 three back-contacted devices, all with efficiencies beyond 26.0 % (Yoshikawa et al., 2016, 2017a, 2017b). This race to record efficiency culminated with the demonstration by Kaneka, Japan, of an impressive 26.7 %-efficient back-contacted solar cell (Green et al., 2017). Equally interesting, ISFH, Germany (Krügener et al., 2017), and SunPower, USA (Green et al., 2016), recently broke the 25.0 % efficiency barrier with back-contacted devices, but using a silicon oxide and polysilicon stack as passivating contact materials.

In spite of these outstanding results, it is commonly accepted that back-contacted devices suffer from complex processing, which is unfavorable for mass production. This increased process complexity stems from the need to individually pattern and accurately align the electron- and the hole-collecting regions (usually in the form of two interdigitated combs), their respective electrode, as well as opened regions ("gaps") to prevent shunts between the two polarities. Important efforts have thus been devoted to develop industry-compatible patterning techniques, such as direct laser ablation (Harrison et al., 2016), dry etching (Kim et al., 2017; Tucci et al., 2008), and their combination (Xu et al., 2017), as well as shadow masking (Tomasi et al., 2014a, 2014b). These methods aim at replacing the photolithography still used (sometimes allegedly) for best-in-class back-contacted devices (Krügener et al., 2017; Masuko et al., 2014; Yoshikawa et al., 2017a).

Regardless of the chosen patterning technique, an important part of the process complexity is a consequence of the accurate alignments required at several stages of a back-contacted device fabrication, namely the alignment of the electron- *vs* the hole-collecting fingers and of their respective electrode. Consequently, a dramatic alleviation of the process complexity can be expected from a simplification of the device architecture itself. Several papers already pointed out that a gap between the electron- and the hole-collecting regions is not needed, already relaxing the alignment constraints (Noge et al., 2015; Stang et al., 2017; Tomasi et al.,

2014b). Going even further, we proposed recently (Tomasi et al., 2017) a disruptive back-contacted device architecture featuring an interband silicon tunnel junction at the electron-collecting regions. This innovative approach, named "tunnel-IBC", dramatically simplifies the process flow of back-contacted devices as it eliminates the patterning of the hole collector as well as its alignment to the electron collector, and might thus be a major leap towards their cost-effective production.

In this contribution, we provide further insights into the tunnel-IBC architecture, and especially focus on the development of efficient tunnel junctions and hole collectors using hydrogenated nano-crystalline silicon (*nc*-Si:H) layers.

2. THE TUNNEL-IBC DEVICE: ARCHITECTURE AND CHALLENGES

Figure 1 compares the architecture of a conventional interdigitated back contact silicon heterojunction (IBC-SHJ) device and the tunnel-IBC concept. In a conventional IBC-SHJ device, both the electron and the hole collectors are patterned and must be aligned one with respect to the other. In contrast, in the tunnel-IBC device, only the electron collector is patterned, whereas the hole collector covers the entire rear surface, including the electron-collecting fingers, hence forming a tunnel junction (TJ) at these locations.

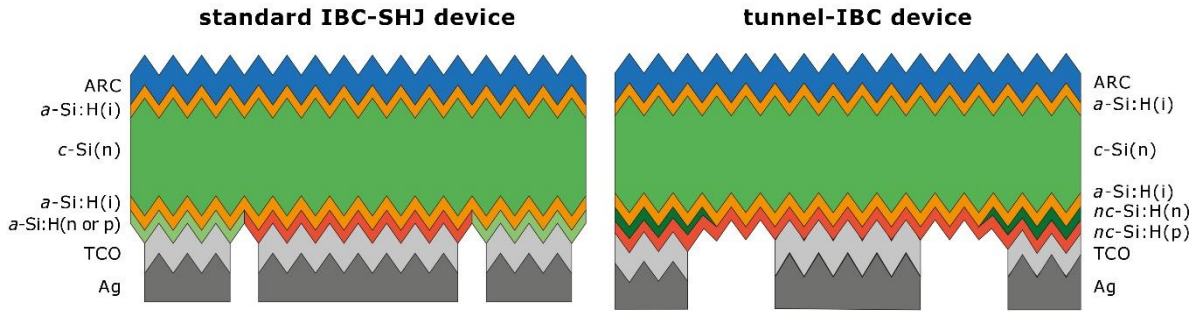

Figure 1. Cross-section view of a conventional IBC-SHJ device (left) and the tunnel-IBC concept (right). Pictures adapted from (Tomasi et al., 2017).

Compared to conventional IBC-SHJ devices, the tunnel-IBC relies on a drastically simplified process flow. Indeed, it simultaneously eliminates the requirement of any patterning step for the hole-collecting regions, as well as any alignment between the hole- and the electron-collecting regions. Consequently, only two patterning steps and one alignment step are required, namely (i) the patterning of the electron-collecting fingers, (ii) the patterning of the

TCO/metal electrode, and (iii) the alignment of the patterned TCO/metal electrode on the electron- and the hole-collecting regions. This very lean process flow is thus an important progress towards the successful implementation of the IBC-SHJ technology at industrial level.

However, in order to work efficiently, the tunnel-IBC device must overcome some challenges. First, the TJ located at the electron-collecting regions must offer a good electron selectivity and not impede the carrier transport to the back electrode. A well-known possibility to do so is to use highly-doped materials in order to narrow the TJ depletion width, and hence facilitate the tunneling of the carriers (Esaki, 1958). Second, as the hole collector covers the entire rear surface, the hole- and the electron-collecting regions are electrically connected. To prevent lateral carrier transport – and hence short-circuits – the hole collector materials must feature a low lateral conductance. Importantly, this second requirement is in apparent contrast with the first one, where a high doping – and hence a high conductivity – is required. As already developed in (Tomasi et al., 2017), we exploited the anisotropic growth mechanism of *nc*-Si:H layers to fulfil these two competing requirements. In section 4 below, additional insights into the required properties of the *nc*-Si:H layers will be provided and discussed.

3. EXPERIMENTAL

3.1 *a*-Si:H and *nc*-Si:H layers characterization

The thickness of the *a*-Si:H and the *nc*-Si:H layers was measured on glass samples by spectroscopic ellipsometry using a J.A. Woolam α-SE™ tool. The crystallinity of the *nc*-Si:H layers was determined by Raman spectroscopy using a Renishaw inVia tool operated with a 515 nm laser. Again, glass samples, coated either with a single 10-nm-thick intrinsic *a*-Si:H substrate layer or with a stack comprising the former 10-nm-thick *a*-Si:H(i) layer capped with an additional 50-nm-thick n-type *nc*-Si:H layer, were used. The Raman spectra were fitted using three Gaussian peaks centered at 480 cm^{-1}, 510 cm^{-1} and 520 cm^{-1}. The Raman crystallinity (χ_c) was then calculated as $\chi_c = (A_{510} + A_{520})/(A_{480} + A_{510} + A_{520})$ where A_{480} (resp. A_{510} and A_{520}) represents the area below the Gaussian peak at a wavenumber of 480 nm^{-1} (resp. 510 nm^{-1} and 520 nm^{-1}), as proposed by (Vallat-Sauvain et al., 2006). Note that the penetration depth of the 515 nm laser used here in *nc*-Si:H is of about 50 nm (Carpenter et al., 2017), which is comparable to the typical thickness of the *nc*-Si:H layers under investigation. Consequently, the Raman crystallinity calculated in this contribution is an average value over

the whole layer thickness. To obtain more details on the crystallinity of our *nc*-Si:H layers along their depth, transmission electron microscopy pictures of various *a*-Si:H and *nc*-Si:H stacks were performed on a FEI Titan Themis tool.

3.2 Device processing

Three kinds of devices were considered in this paper. First, to conduct the preliminary developments of the *nc*-Si:H layers, 4-cm^2 two side-contacted silicon heterojunction solar cells with front hole collector (FHC, sometimes still referred to as "front emitter") were processed. Two arrangements of these FHC devices were investigated. In a first arrangement ("FHC type I" devices, see Figure 2), the devices featured an intrinsic/p-type *a*-Si:H stack at the front, whereas different full area TJ materials were investigated at the back, namely *a*-Si:H(n)/*a*-Si:H(p), *nc*-Si:H(n)/*a*-Si:H(p) and *nc*-Si:H(n)/*nc*-Si:H(p) stacks. These devices aimed at investigating the electron selectivity and transport properties of the TJ itself. In another arrangement ("FHC type II" devices, see again Figure 2), the solar cells featured an intrinsic/n-type *a*-Si:H stack at the back, whereas p-type *nc*-Si:H layers with a varying doping gas concentration were deposited at the front. The doping gas concentration is defined as the ratio of the doping gas flow (here trimethylboron for our p-type layers) to the silane flow, and ranges from 1 to 5 % in this contribution. Once efficiently working in both types of FHC devices, the *nc*-Si:H layers were used in the third kind of device under investigation in this paper, namely tunnel-IBC devices (see Figure 1, right).

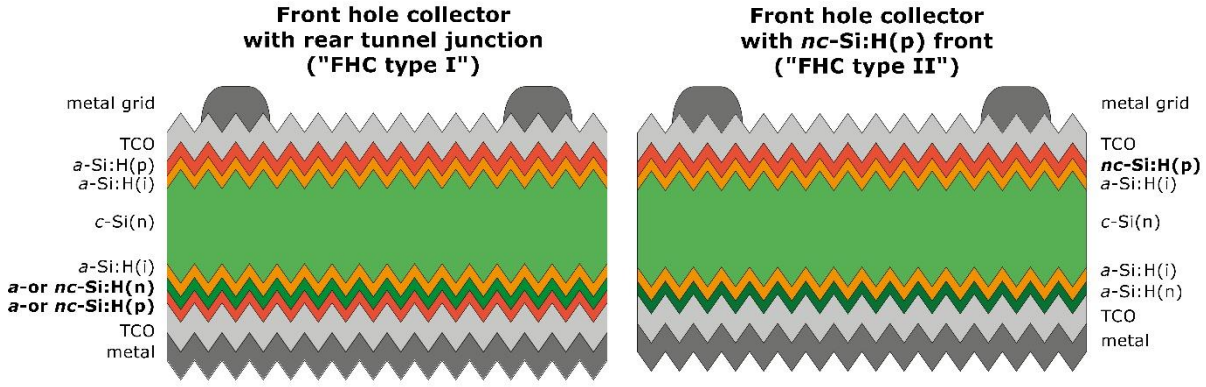

Figure 2. Cross-section view of the two kinds of two side-contacted silicon heterojunction devices used as test structures to develop the *nc*-Si:H layers. Left: front hole collector with various tunnel junction configurations at the rear. Right: front hole collector with various p-type *nc*-Si:H layer at the front.

All FHC and tunnel-IBC devices were fabricated on 4-inch n-type float-zone wafers, with a thickness of 260 µm and a resistivity of 3 Ω·cm. After saw-damage removal, alkaline texturing and subsequent cleaning, the wafers were immersed for 60 seconds in a 5 % hydrofluoric acid solution to remove the native oxide. They were then loaded into our Octopus II PECVD-PVD cluster reactor from INDEOtec SA. The *a*-Si:H and *nc*-Si:H layers were deposited using a mixture of silane, hydrogen, phosphine and trimethylboron. All layers were full area-deposited, at the notable exception of the electron-collecting fingers of the tunnel-IBC devices which were patterned using a shadow mask. Details on the in-situ shadow mask technique can be found in (Tomasi et al., 2014a, 2014b). Moreover, all *a*-Si:H layers were deposited at 200°C, whereas two deposition temperatures were investigated for the *nc*-Si:H layers, namely 180°C and 200°C. The FHC devices then received a 75-nm-thick transparent conductive oxide (TCO) layer at the front, and a full area rear reflector composed of TCO and sputtered Ag at the back. The front side of these devices was eventually completed by a screen-printed grid, and the devices were cured in a belt oven. In contrast, the tunnel-IBC devices received a 75-nm-thick silicon nitride layer at the front, and a blanket TCO layer at the back. An interdigitated grid was then screen-printed on the devices rear side and cured. Eventually, the TCO layer was locally opened using a dilute acidic solution, the screen-printed fingers acting as hard mask.

3.3 Device characterization and modeling

The current-voltage (*I*-*V*) characteristics of the FHC and the tunnel-IBC devices were measured in-house on a Wacom WXS-90S-L2 system using standard test conditions at 25 °C under 1-sun AM1.5G equivalent illumination. For the FHC devices, a shadow mask with 3.99-cm^2 certified designated area was used. For the tunnel-IBC, a 5 cm × 5 cm designated area was defined using a shadow mask, excluding the busbar area. A temperature-regulated, aluminum-anodized black chuck specifically designed to provide an alignment accuracy of ±50 µm between the tunnel-IBC device under test and the shadow mask was used. From the 1-sun *I*-*V* curve, the values of the short-circuit current density (J_{sc}), the open-circuit voltage (V_{oc}), the fill factor (FF), and the conversion efficiency (Eff.) of the device under test were extracted. All devices were subsequently measured at three additional illumination intensities (0.5 sun, 0.15 sun and 0.07 sun) in order to extract the series resistance (R_{series}) from the *I*-*V* curves according to the method provided in (Bowden and Rohatgi, 2001). The R_{series} of the tunnel-IBC devices was also calculated with the model we already used in (Tomasi et al., 2014a).

4. RESULTS AND DISCUSSION

4.1 Selective crystalline growth of *nc*-Si:H layers

To fulfil the two competing requirements necessary to obtain efficient tunnel-IBC devices as presented in section 2, we exploit the anisotropic growth mechanism of *nc*-Si:H layers. It is indeed well known from the literature that the crystallinity of such layers strongly depends on the substrate on which they are deposited (Roca i Cabarrocas et al., 1995; Vallat-Sauvain et al., 2005). If grown on an amorphous substrate, an amorphous nucleation layer, usually 5 to 10-nm-thick, will form before the crystalline growth sets in. In contrast, if the substrate has already some crystallinity, the *nc*-Si:H layer will present large crystallites spanning over its entire thickness.

The high-resolution scanning transmission electron (STEM) micrographs and corresponding inverse Fourier transforms of selected reflections presented in Figure 3 illustrate this spatial differentiation. At the TJ location (see Figure 3a-c), single grains are found to span across the *nc*-Si:H(n)/*nc*-Si:H(p) interface as well as over the entire thickness of the p-type *nc*-Si:H layer. This is explained by the fact that this layer is grown on top of the patterned n-type *nc*-Si:H fingers, which are crystalline in their upper part and hence act as a nucleation layer. This effect promotes the epitaxial growth of some *nc*-Si:H(p) crystals on the *nc*-Si:H(n) ones (see the arrow in Figure 3), hence increasing the overall crystallinity of the top *nc*-Si:H(p) layer. Consequently, the materials forming the TJ are highly doped, which is a prerequisite for an efficient TJ. In contrast, between the electron-collecting fingers, the p-type *nc*-Si:H layer is directly grown on the fully amorphous intrinsic *a*-Si:H buffer layer (see Figure 3d-f). There, the p-type *nc*-Si:H layer appears less crystalline, with amorphous regions covering not only the first few nanometers of the layer in some regions but also regions between the conical grains due the proto-crystalline growth regime. Due to these amorphous regions, the p-type *nc*-Si:H layer exhibits a lower lateral conductance over the hole-collecting fingers, hence preventing any shunt with the electron-collecting ones. Remarkably, with a single layer, we are thus able to fulfill the two competing requirements of the tunnel-IBC by exploiting the influence of the underlying layer on the growth mechanism of the p-type *nc*-Si:H layer.

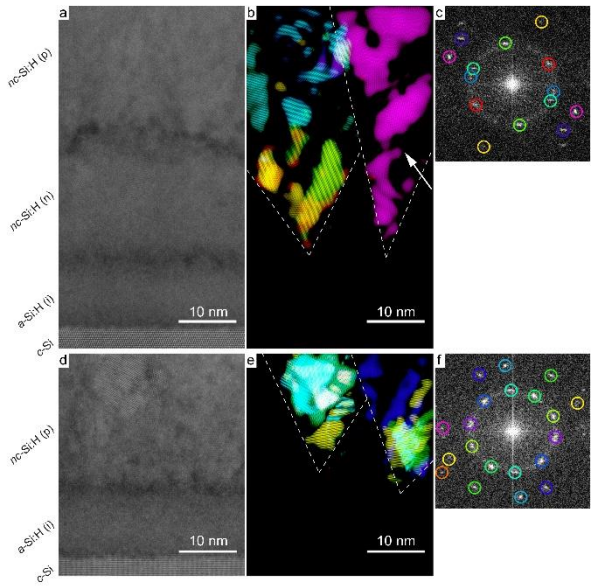

Figure 3. STEM high-angle annular dark-field (HAADF) micrographs of the *nc*-Si:H layers microstructure: at the TJ location (a) and in the middle of the hole collector (d), with the corresponding coloured inverse Fourier transform of selected reflections (b and e) obtained from the Fourier transform (c and f). Coloured regions show individual grains. The arrow in Figure 3b shows the epitaxial growth of some *nc*-Si:H(p) crystals on the *nc*-Si:H(n) ones. All pictures adapted from (Tomasi et al., 2017).

Figure 4 plots χ_c of several p-type *nc*-Si:H layers whether they are grown on an intrinsic *a*-Si:H substrate or on an n-type *nc*-Si:H substrate. χ_c of the p-type *nc*-Si:H layer is found to be always higher when grown on the n-type *nc*-Si:H substrate than on the intrinsic *a*-Si:H one. It is also worth noticing that the crystallinity of the *nc*-Si:H(n)/*nc*-Si:H(p) stack is always higher than the crystallinity of the n-type *nc*-Si:H layer itself (see the grey area in Figure 4), validating that the increased crystallinity actually owes to the more crystalline p-type *nc*-Si:H layer and is not a measurement artifact. Overall, the outcome of the Raman analysis are fully consistent with the TEM images, and validate that the use of *nc*-Si:H layers allows to simultaneously obtain an highly-doped n/p interface at the TJ and a low lateral conductivity of the p-type *nc*-Si:H layer.

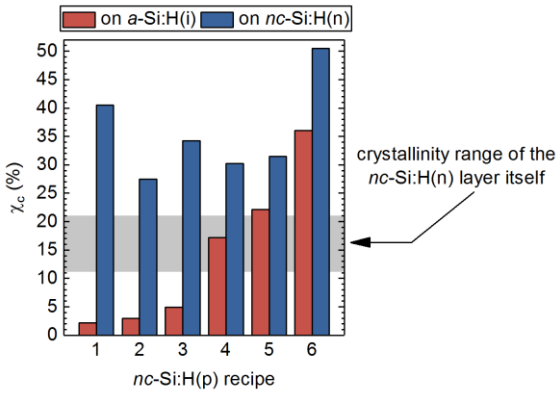

Figure 4. Crystallinity (χ_c) of various p-type *nc*-Si:H layers when grown on an intrinsic *a*-Si:H susbtrate (red bars) or on a n-type *nc*-Si:H layer (blue bars). The grey area indicates the crystallinity range of the n-type *nc*-Si:H substrate itself.

4.2. Development of *nc*-Si:H-based tunnel junction

nc-Si:H-based TJs were evaluated as electron collector at the rear of 4-cm^2 two side-contacted SHJ devices (see "FHC type I" in Figure 2, section 3.2), and compared to *a*-Si:H-based ones. The *I-V* curves of the best devices obtained at a deposition temperature of 180°C are presented in Figure 5, while the mean electrical parameters (averaged over 6 devices) are gathered in Table I. Using an *a*-Si:H(n)/*a*-Si:H(p) TJ, a mean V_{oc} of 711 mV and a mean FF of 70.5 % are obtained. Moreover, devices using this TJ configuration feature s-shaped *I-V* curves (see exemplarily curve ① in Figure 5). These results hence point towards impaired carrier transport and a reduced selectivity of the tunneling electron contact when solely *a*-Si:H materials are used. In contrast, replacing the *a*-Si:H(n) layer with a *nc*-Si:H(n) one, the mean V_{oc} and FF increase to 718 mV and 77.0 % with no s-shape visible (curve ② in Figure 5). Eventually, using a *nc*-Si:H(n)/*nc*-Si:H(p) TJ, a mean V_{oc} and FF of 722 mV and 79.4 % are obtained. The best device for this particular batch reaches 22.3 % efficiency, with a V_{oc} of 726 mV and a FF of 80.6 %. *I-V* curves of devices with *nc*-Si:H-based TJ do not feature any parasitic effect indicating charge-carrier transport losses (curve ③ in Figure 5). This confirms the potential of n- and p-type *nc*-Si:H layers to form efficient TJs.

Table I. *I-V* parameters of 4-cm^2 two side-contacted SHJ devices featuring a TJ as rear electron collector (values averaged over 6 devices).

TJ configuration	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff. (%)
a-Si:H(n)/a-Si:H(p)	37.6 ± 0.3	711 ± 6	70.5 ± 3.4	18.8 ± 1.0
nc-Si:H(n)/a-Si:H(p)	37.4 ± 0.2	718 ± 4	77.0 ± 1.2	20.7 ± 0.4
nc-Si:H(n)/nc-Si:H(p)	38.0 ± 0.2	722 ± 7	79.4 ± 2.3	21.8 ± 0.9

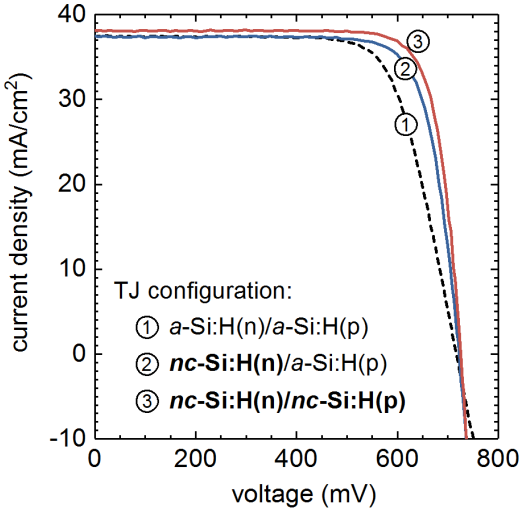

Figure 5. *I-V* curves of two side-contacted SHJ devices featuring a TJ as electron collector at the rear.

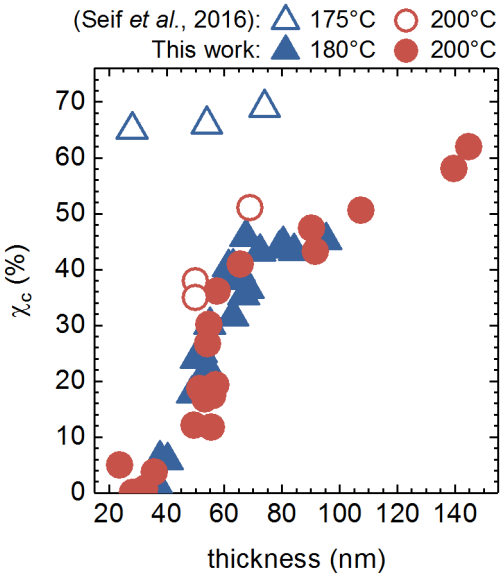

Figure 6. Crystallinity (χ_c) as a function of the *nc*-Si:H layer thickness for different deposition temperatures.

Deposition temperature has been shown to have a significant impact on the crystallinity and the quality of *nc*-Si:H layers (Mazzarella et al., 2014; Seif et al., 2016). To investigate this effect, type I FHC devices were processed using two different deposition temperatures for the *nc*-Si:H layers, namely 180°C and 200°C. Figure 6 plots the crystallinity of our *nc*-Si:H layers as a function of their thicknesses, for the two above-mentioned deposition temperatures. No noticeable differences were observed, as at both temperatures, similar χ_c values are obtained for a given thickness. Overall, χ_c is mainly driven by the thickness of the *nc*-Si:H layers. This is in contrast with the results obtained by (Seif et al., 2016), where a temperature of 175°C was found to yield higher χ_c for a given thickness. Several process properties can owe for this peculiar result, such as the deposition frequency, the gas dilution, the plasma power, the

process pressure, to name a few. However, once integrated as electron collector in type I FHC devices, the *nc*-Si:H layers deposited at 200°C provide higher V_{oc} and FF compared to the same layers deposited at 180°C, as illustrated in Figure 7. These results point towards a better doping efficiencies of the *nc*-Si:H layers when deposited at 200°C, although further experiments are required to validate this hypothesis.

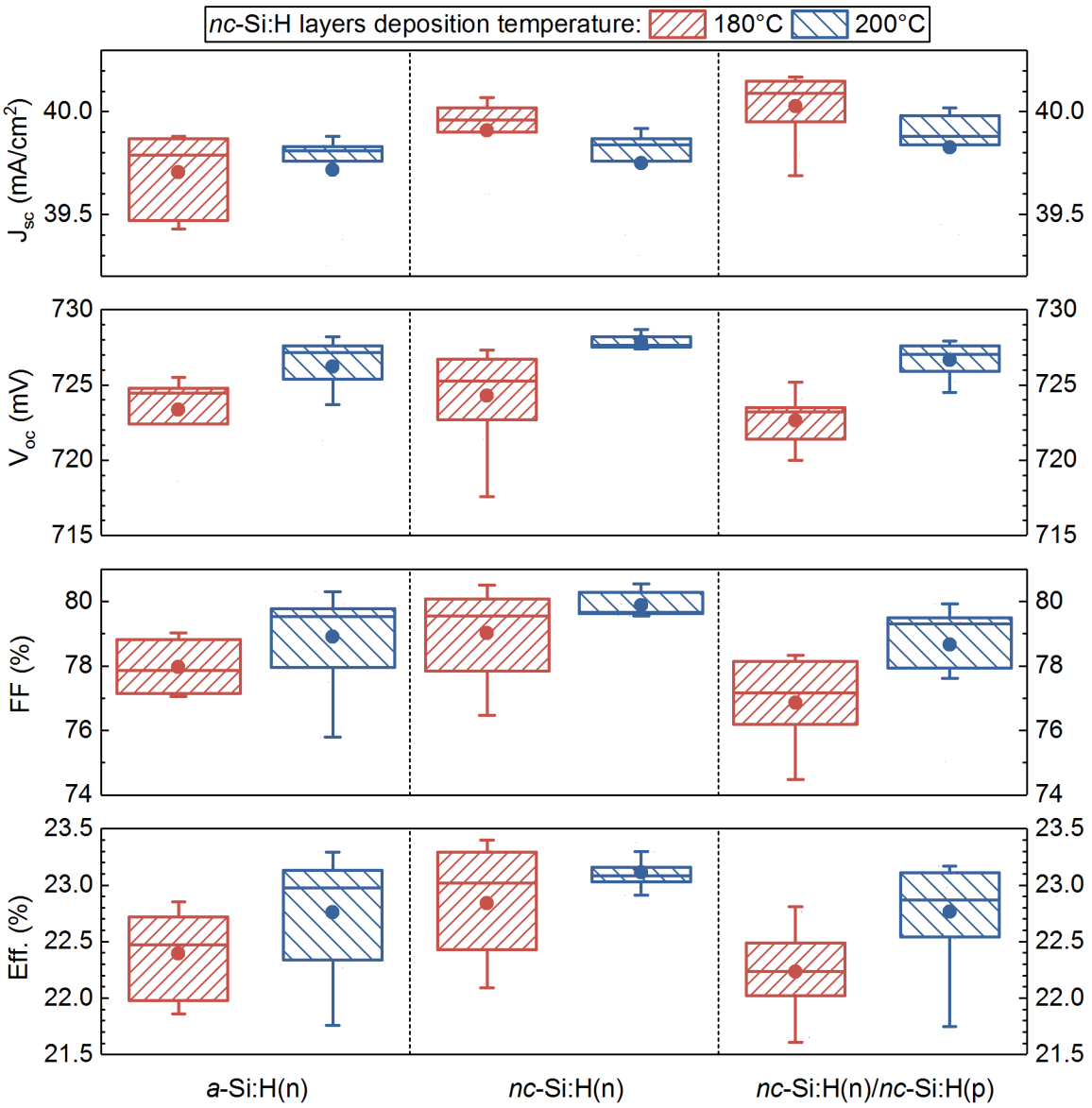

Figure 7. *I-V* parameters of 4-cm^2 two side-contacted SHJ devices featuring a TJ as rear electron collector for two different deposition temperatures of the *nc*-Si:H layers. 10 devices were processed and measured for each conditions. The boxes gives the 25 %, the 50 % and the 75 % percentiles; the whiskers are the 2σ deviations; the filled dots are the average values.

Figure 8 then plots the influence of χ_c of the *nc*-Si:H(n)/*nc*-Si:H(p) stack on the electron collection properties of the TJ based on this stack. As can be seen, a minimum χ_c of ca. 15 % (corresponding to a 50-nm-thick *nc*-Si:H(n)/*nc*-Si:H(p) stack) is required to build up a good electron selectivity with minimal transport losses, and a median V_{oc} and FF of 726 mV and 79 % are obtained. Increasing further χ_c of the TJ up to 40 % (corresponding to a 65-nm-thick *nc*-Si:H(n)/*nc*-Si:H(p) stack) only results in moderate V_{oc} and FF gain.

As an intermediate conclusion, the developments of TJ in FHC devices revealed that (i) a fully *nc*-Si:H-based TJ is required to obtain a good electron selectivity without impeding the carrier transport, and (ii) *nc*-Si:H-based TJ deposited at 200°C with at least 15 % χ_c yield the best V_{oc} and FF.

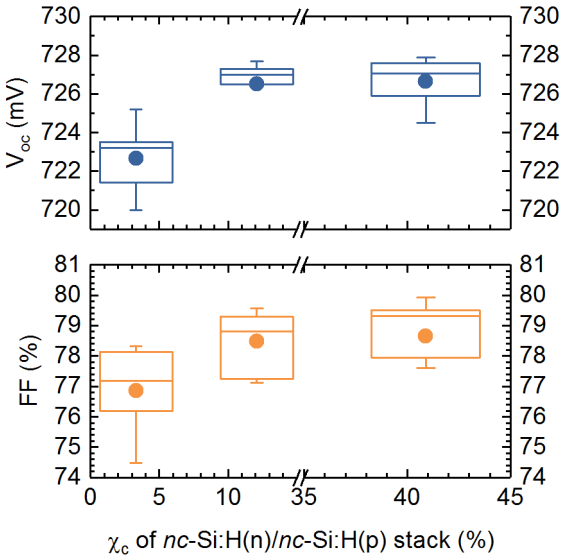

Figure 8. Influence of the crystallinity (χ_c) of the *nc*-Si:H(n)/*nc*-Si:H(p) TJ on the V_{oc} and the FF of two side-contacted SHJ devices featuring a TJ as rear electron collector.

4.3 Development of p-type *nc*-Si:H hole collector

In section 4.2 above, the use of n-type *nc*-Si:H layers and *nc*-Si:H(n)/*nc*-Si:H(p) TJs was validated as electron collector only. Yet, in the tunnel-IBC, the p-type *nc*-Si:H layer has to work as an efficient hole collector outside the TJ locations. However, in contrast to n-type *nc*-Si:H layers, obtaining efficient *nc*-Si:H hole collector might be more problematic. Several detrimental effects have been observed, such as poor crystallinity (Chou et al., 1992), poor hole selectivity and impaired carrier transport (Lee et al., 2014; Mazzarella et al., 2014), as

well as lifetime degradation after deposition of the p-type *nc*-Si:H layer (Ji et al., 2012; Pomaska et al., 2015). Fortunately, in the specific case of the tunnel-IBC architecture, the constraints on the p-type *nc*-Si:H layer are less stringent because a high χ_c is only required at the TJ location, and not necessarily at the hole collecting regions. Hence, in these regions, it is not an absolute necessity to strive for a high χ_c of the p-type *nc*-Si:H layer, but rather to focus on optimizing the hole selectivity and collection properties of this latter. Based on this, one option is to stay in a proto-crystalline regime, where the p-type *nc*-Si:H layer will essentially stay amorphous on the intrinsic *a*-Si:H substrate layer in the hole-collecting regions, while still presenting an important crystallinity at the TJ locations (see again Figure 4 in section 4.1).

Figure 9 plots the variation of the χ_c of p-type *nc*-Si:H layers grown on top of a 10-nm-thick intrinsic *a*-Si:H substrate as a function of the doping gas concentration in the p-type *nc*-Si:H layers, and the corresponding V_{oc} and FF of type II FHC devices. The layer thickness was kept constant at 35 nm regardless of the doping gas concentration. Consistently with the literature, χ_c decreases with increasing the doping gas concentration. This owes to the amorphization effect induced by the boron atoms (Ji et al., 2012; Saleh and Nickel, 2003). Starting from χ_c = 25 % for a doping gas concentration of 1 %, χ_c quickly drops to 5 % for a doping gas concentration of 1.5 %. For higher doping gas concentrations, χ_c is lower than 1 %, so p-type *nc*-Si:H layers grown in these conditions are actually essentially amorphous. Interestingly, V_{oc} and FF are actually found to be the highest for a doping gas concentration of 3 %, hence for a proto-crystalline p-type *nc*-Si:H layer. If the doping gas concentration is pushed further, then the devices suddenly feature an s-shaped *I-V* curve (see Figure 10), and their V_{oc} and FF are strongly affected. This behavior might owe to a very large defect density of the p-type *nc*-Si:H layer when using a too large doping gas flow.

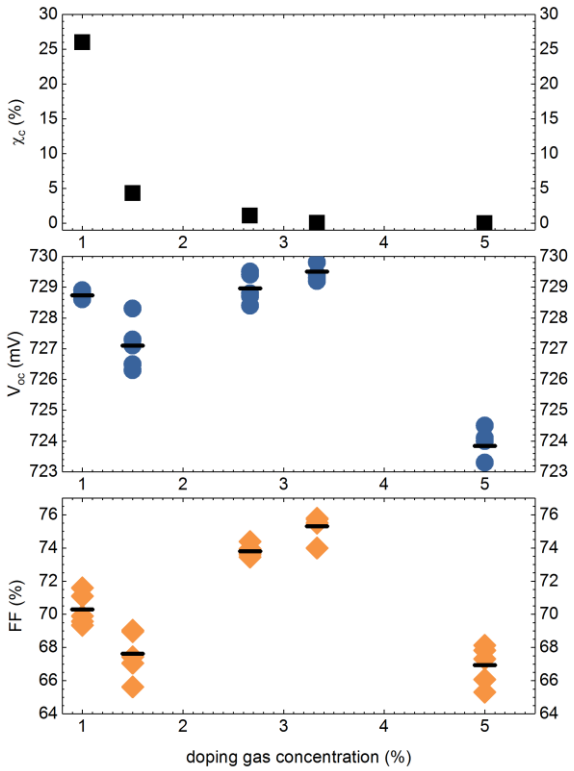

Figure 9. Crystallinity (χ_c), V_{oc} and FF of 4-cm^2 two side-contacted SHJ devices featuring a p-type *nc*-Si:H layer as front hole collector, as a function of the doping gas concentration in the p-type *nc*-Si:H layer, for a fixed thickness of 35 nm.

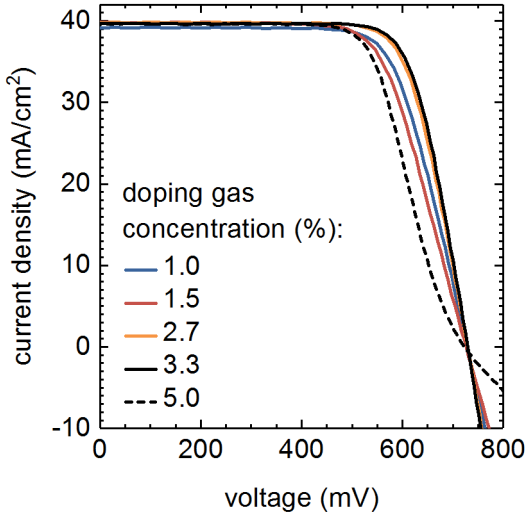

Figure 10. Selected *I-V* curves from some of the 4-cm^2 two side-contacted SHJ devices featuring a p-type *nc*-Si:H layer as front hole collector presented in Figure 9.

The results of a complementary experiment, plotted in Figure 11, show the variation of χ_c (again for p-type *nc*-Si:H layers grown on a 10-nm-thick intrinsic *a*-Si:H substrate), V_{oc} and FF of type II FHC devices as a function of the p-type *nc*-Si:H layer thickness, for a fixed doping gas concentration of 1.5 %. χ_c follows the expected trend and increases with the layer thickness. Regarding hole selectivity, a p-type *nc*-Si:H layer at least 35-nm-thick is required to build up a correct V_{oc}; increasing the thickness of the p-type *nc*-Si:H layer over this value does not result in major V_{oc} improvement. In contrast, mean FF values below 70 % are obtained as long as the p-type *nc*-Si:H layer is thinner than 65 nm; with the considered doping gas concentration, at least an 80-nm-thick p-type *nc*-Si:H layer is required to obtain FF values close to 78 %. The fact that such a thick layer is required to obtain decent FF values when using 1.5 % doping gas concentration suggests a too low active doping of the p-type *nc*-Si:H layer; full dopant activation is only reached when the crystalline growth sets in, *i.e.* with very thick layers. As such a thickness would seemingly be quite incompatible with the SHJ standards for mass production, it is therefore more suitable to use 35-nm-thick layers but with well-chosen doping efficiency, as demonstrated from Figure 9.

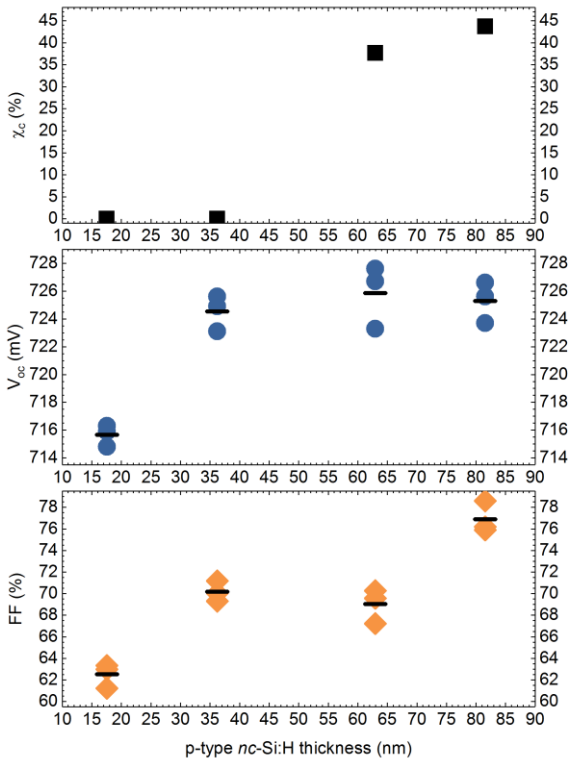

Figure 11. Crystallinity (χ_c), V_{oc} and FF of 4-cm^2 two side-contacted SHJ devices featuring a p-type *nc*-Si:H layer with increasing thickness as front hole collector, for a fixed doping gas concentration of 1.5 %.

These results show that crystallinity must not be the primary parameter to be considered when developing p-type *nc*-Si:H layers for tunnel-IBC devices, but rather to aim at a high V_{oc} and FF obtained with a reasonable layer thickness. The "best" p-layer for this function is thus obtained when staying in the proto-crystalline regime. Doing so, many potential detrimental effects of p-type *nc*-Si:H layers are avoided, such as lifetime degradation of the underlying intrinsic *a*-Si:H layer, or poor hole selectivity and transport. Eventually, the proto-crystalline regime will still ensure a high crystallinity of the p-type *nc*-Si:H layer when grown on the patterned n-type *nc*-Si:H fingers, and hence good TJ properties, as seen in Figure 4.

4.4 Tunnel-IBC devices: current status and outlook

Tunnel-IBC devices integrating the above-described *nc*-Si:H layers and TJs were processed. Starting from 9-cm^2 proof-of-concept devices with up to 22.6 % certified efficiency (Tomasi et al., 2017), we up-scaled our process to 25-cm^2-large devices. To date, our best 25-cm^2 tunnel-IBC device features 23.9 % efficiency, with J_{sc} = 41.6 mA/cm^2, V_{oc} = 734.5 mV and FF = 78.2 %

(see Figure 12). Importantly, the pseudo-FF of this device was measured to be 85.1 %, hence validating that this tunnel-IBC device does not suffer from lateral shunt, as anticipated from our *nc*-Si:H layers developments. Calculation of the R_{series} losses breakdown (see Figure 13) reveals that the tunnel-IBC device under investigation is mainly limited by the transport losses at the p-type *nc*-Si:H/TCO hetero-contact, this latter accounting for 61 % of the total R_{series} losses. This owes to its very high specific contact resistivity, which was measured to be as high as 400 mΩ·cm^2 (Nogay et al., 2016).

On these grounds, mitigating the transport losses at the p-hetero-contact can be made in two ways. A first straightforward option is to increase the hole collector area fraction (Desrues et al., 2011). Our modeling results suggest that a 1 to 2 $\%_{abs}$ FF gain could be expected by increasing the metalized hole collector fraction from 52 % (current design) to 66 %, keeping the same width for the electron-collecting fingers. Further increases of the hole collector area are not expected to yield any additional FF gain, as the reduction of the transport losses at the p-hetero-contact will come at the expense of an increase of the base resistance losses, unless the width of the electron-collecting fingers is notably reduced. Satisfying this latter possibility might however prove challenging with our current shadow mask patterning technique, as several detrimental effects such as a reduction of the deposition rate and a thickness tapering were found to be stronger for features patterned through narrow mask slits (Ledinský et al., 2016).

Alternatively, a second promising option is to reduce the specific contact resistance of the p-hetero-contact. The potential FF gain here is much more promising, as our modeling predicts that FF above 82 % are achievable with our current rear side geometry, providing a 10-fold decrease of the *nc*-Si:H(p)/TCO specific contact resistivity. How to actually reach such low contact resistivity is unfortunately not known yet. Recent results suggest that FF as high as 86 % can be obtained reaching an activation energy smaller than 200 meV for the doped layers (Procel et al., 2017). Here, *nc*-Si:H layers are again promising candidates as they are known to offer a lower activation energy than *a*-Si:H ones.

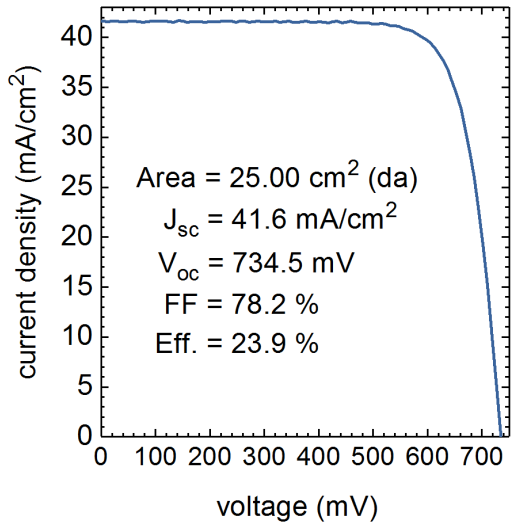

Figure 12. *I-V* characteristic of the tunnel-IBC with the highest efficiency processed so far in our facilities.

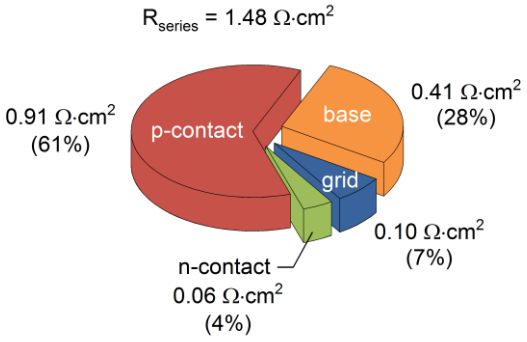

Figure 13. Breakdown of the series resistance losses of the tunnel-IBC device whose *I-V* characteristic is presented in Figure 12.

5. Conclusion

In this paper we reported on the development of an innovative IBC-SHJ architecture – named "tunnel-IBC" – featuring a silicon interband tunnel junction. This approach drastically reduces the complexity usually associated with IBC-SHJ devices processing. *nc*-Si:H layers with well-controlled growth properties were demonstrated to be the key enablers of the tunnel-IBC concept, as this materials allows to concomitantly obtain an highly-doped n/p interface at the tunnel junction and a low lateral conductance of the hole-collecting layer. Tunnel-IBC devices were processed and reached so far up to 23.9 % efficiency. Transport resistance losses at the p-type hetero-contact were found to be the main limiting factor to higher efficiencies. Mitigation of these transport losses are expected from a drastic reduction of the specific contact resistivity between the p-type *nc*-Si:H hole collector and the TCO, and from the adaptation of the rear side design in a lesser extent.

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