MIA, a reusable execution platform for space missions. A case study based on an Autonomous Flight Termination Unit.

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S.A.F.E.S.T.
Smart Avionics for Flight Termination System

Introduction

In this new space era, the price dictates the business. In order to increase the reusability, modularity and overall, ease the development of FSW, we have developed the sMart Integrated Avionics (MIA) platform. This platform significantly facilitates the development of space software and applications, such as the one presented as use case in this work, an Autonomous Flight Termination Unit (AFTU). This autonomous launcher subsystem allows unmanned operations, increasing the maximum launch cadence, thus reducing the cost for space missions, facilitating that access to space is more easily and rapidly achieved by all types of agents.

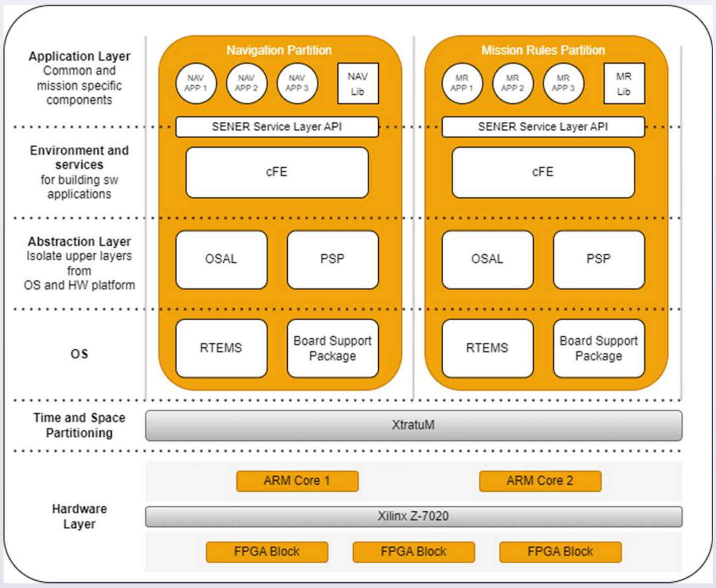

Figure 1. MIA specification for the AFTU

The MIA platform

The MIA platform is composed by a set of interchangeable software components, FPGA blocks, and hardware devices in which it can be executed. MIA presents a highly decoupled layered architecture developed to operate and communicate using a set of standardized common interfaces between layers. This allows us to customize MIA by changing the components for each particular space mission implementation without affecting the rest, granting the needed modularity and reusability to the platform. To cope with the requirements of the AFTU system we have developed a MIA specification that follows the architecture shown in Figure 1. It is developed to be deployed over the Xilinx MPSoC Z-7020. At software level, the structure designed for MIA to fulfill the needs of an AFTU is the following:

- FentISS XtratuM Hypervisor for Time and Space Partitioning. The hypervisor plays a pivotal role in enabling the deployment of the two primary applications of the AFTU: the Navigation Partition and the Mission Rules partition.
- Real-Time Executive for Multiprocessor Systems (RTEMS) as Real Time Operating System. Allows the deployment of different priority level applications on top of the platform, required by some algorithm functions embedded both in the Navigation and Mission rules partitions.
- core Flight Executive (cFE) the core of NASA's core Flight System (cFS) for the FSW framework. The cFE provides a set of core services including Software Bus (messaging), Time, Event (Alerts), Executive (startup and runtime), and Table services. Both, cFE and RTEMS are particularly tailored to fulfill the necessities and certification requirements that space missions present by means of developing a Qualification Data Package (QDP) categorized under ECSS software criticality C. This QDP is specifically designed for deployment on the Xilinx Z-7020 platform by the consortium company embedded brains.
- SENER Service Layer API (SSLA) is central to the design of MIA, it comes along with its own Software Development Kit (SDK), and it presents developers with a set of common services and functionalities, useful in the context of space missions, for deploying their own mission FSW.

AFTU SW Partitions

For the AFTU, two Mission Partitions are developed, the 'Navigation' and the 'Mission Rules', each of them executed in a separate hypervisor partition.

The Navigation is responsible for processing real-time sensor inputs and executing algorithms to ensure precise and accurate position location throughout the flight trajectory. In parallel, the Mission Rules partition operates as a flight correctness and trajectory verification system. It continuously monitors the flight parameters against predefined mission rules and criteria, verifying the adherence to desired flight paths and safety protocols. These parameters not only come from the inner Navigation partition, but also from others tracking inputs that the user can send to the system. The architecture and high-level data flow of the AFTU system is described in Figure 2.

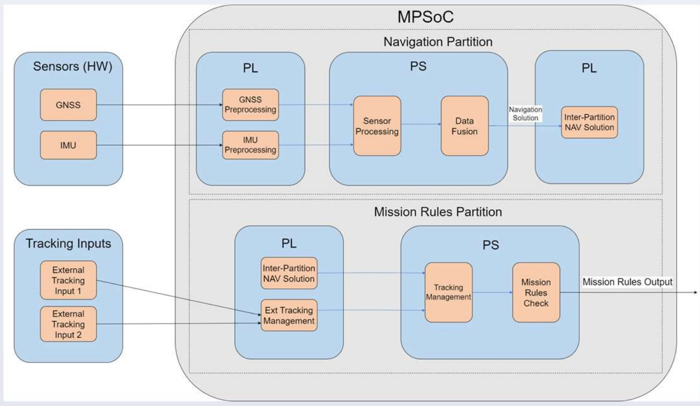

Figure 2. High-level Navigation Partition data flow

To deploy this architecture on the MIA platform, a set of SSLA applications and FPGA blocks have been developed. At SW level, three main SSLA application types are developed. FPGA communication, scheduler management and algorithm function applications. For instance, for the Mission Rules Partition the software architecture to be developed is solved with four applications. The two FPGA read and write applications, configured to receive and write the desired data. A Mode Manager application, which receives parameters and computes the system's operating mode. Lastly, the Mission Rules Checker application, which embed the autogenerated algorithm function that checks the correctness of the trajectory. This application configuration and the messages that are interchanged between the applications are shown in Figure 3.

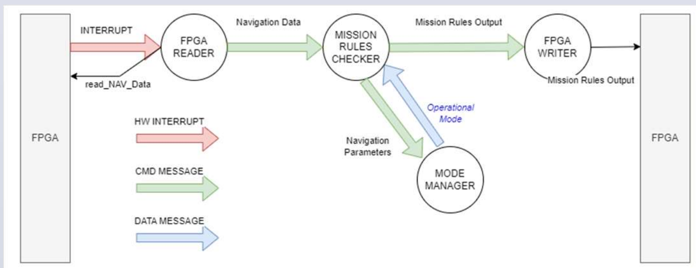

Figure 3. Mission Rules Partition SSLA application architecture

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