On the borderline between hardware and software: Free instruction set architectures as an alternative

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Abstract

Nowadays, free and open instruction set architectures do not present even a rounding error in the microprocessor marketshare measurements. Nevertheless, this is likely to change in the near future especially in the prospect of emerging industries like Internet of Things or Artificial Intelligence which will favor custom processors that offer flexibility to assemble only required parts thus substantially reducing die-size, power and price, and where the place for a dominant processor architecture is still vacant. Although not the only one, the main free candidate to take this leading position is the so-called RISC-V which backed-up by several semiconductor and software industry's big players recently gained quite some momentum. Despite being a relatively young standard, RISC-V already has an extensive userbase as well as the considerable ecosystem around it, both in terms of toolchain support and actual chip demonstrators. Built on the basis of modular rather than traditional incremental design, RISC-V embraces the basic integer set which is frozen and will never change, hence providing a stable target to system programmers. The modularity comes with optional hardware (multiplication/division or floating-point operation for example) extensions to the mandatory base instructions.

Furthermore, this architecture also leaves space for entirely new opcodes to invoke application-specific accelerators, thus being able to cover a complete spectrum from embedded and personal to super and warehouse-scale computers. Even though it is certainly not expected to overthrow the giants like ARM or x86, it has a nice head start to shake the processor world and do something similar to what GNU/Linux has done in the field of operating systems.

Keywords: microprocessors; system-on-chip; Instruction Set Architecture (ISA); RISC-V; open-source hardware.