DETERIORATION OF SHORT CHANNEL EFFECTS IN DUAL HALO BASED TRIPLE MATERIAL SURROUNDING GATE (DH-TMSG) MOSFET

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Abstract

In the proposed work, the analytical model for Surface potential and Electric field has been carried out in a novel structure named dual halo triple material Surrounding-gate metal-oxide-semiconductor field effect transistor (DHTMSG). The new device has been incorporated with symmetrical dual halo regions near source and drain ends, while the gate terminal consists of three different metals with different work functions. The results prove that the device significantly deteriorates the short channel effects which are studied by analytical model for surface potential and electric field using parabolic approximation method. The analytical results are endorsed by the simulation results.

Keywords

Dual halo, Triple material surrounding gate, Short channel effects, Parabolic approximation method.

1. INTRODUCTION

As the device dimensions have been diminishing, the parameters of MOSFET needs better scrutiny to achieve high packing density, high speed and better performance. For the past several decades, the semiconductor industry has gone through series of revolutions in various platforms and one among them is the evolution of Multi Gate MOSFETs. Generally the conventional MOSFETs used by the design engineers are formulated using charge based analysis. Short Channel Effects (SCE) is the major hindrance which deteriorates the performance of conventional MOSFETs. During the application of high voltage near drain, the channel tends to pinch off due to the expansion of depletion region between drain and body. This intrudes inside the inversion region which gives rise to one of the SCE, Drain Induced Barrier Lowering (DIBL) which in turn increases the non-linearity between the drain current and gate to source voltage. As the drain takes the control over gate, the measure of drain current at particular control voltage has become even more complex. Due to the formation of pinch off region, there exists a high electric field near the drain region which leads to Hot-Carrier Effect. This electric field powers the electrons inside the channel region that tends to isolate the gate and inversion region which gives rise to trapping of static charge inside the insulating structure.

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From the theory of PN junction diode, it is possible to reduce the expansion of depletion region between semiconductors by increasing the doping concentration on either side which gives rise to the theory of Pocket implants. At the expense of reverse saturation leakage current, the shallow heavier doping across the small region around drain can considerably reduce the expansion of depletion region with respect to the bias across its PN Junction. After evaluating various multi gate MOSFETs the surrounding gate MOSFET is preferred, as the silicon pile is surrounded by gate in all sides which offers better gate controllability and resilience to short channel effects [1-5].

Threshold voltage Roll-off is another primary threat in the form of sub-threshold current before the MOSFET turns ON. Hence, two unique materials can be embedded together as single gate in such a way the work function variation reduce the threat of short channel effect [6-8]. This work has been extended by replacing three gate materials [9] along with pocket implants [11, 12] which introduces a novel structure, dual halo triple material surrounding gate (DH-TMSG) MOSFET.

2. MODEL FORMULATION

The dual halo triple material surrounding gate (DHTMSG) SOI MOSFET is shown in figure 1. The model comprises five different regions in which the pocket implants are introduced near source end and drain end. The lengths of the three materials (M_1, M_2, and $M3$) in gate are L_1, L_2-L_1 and L_4-L_2, respectively. Therefore, the lengths L_0 and L_4-L_3 are halo doped with doping concentration N_h and the other regions in the channel are doped with doping concentration N_c which is lesser than N_h.

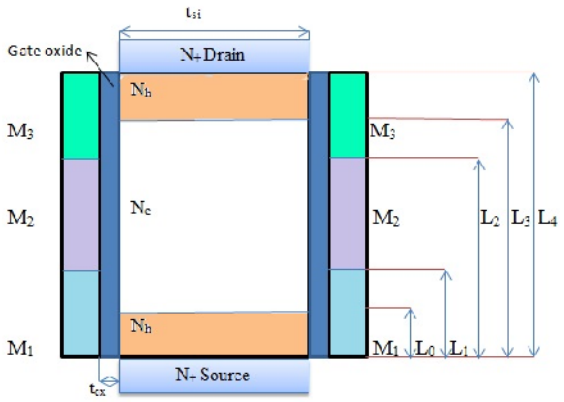

Fig1. Schematic view of DH-TMSG MOSFET

The device structure tends to be cylindrically symmetrical and so the cylindrical coordinate system is employed, which consists of a radial direction r, a vertical direction z, and an angular component θ. The symmetry of the structure indicates that the potential has no variation in the θ direction. Henceforth, a two dimensional analysis is satisfactory.

The surface potential can be derived by solving Poisson's equation in the silicon pile. Assuming that the influence of fixed oxide charges and charge carriers on the electrostatics of the channel can be neglected and the silicon film before the onset of strong inversion can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi_i(r,z)}{\partial r}\right)+\frac{\partial^2 \phi_i(r,z)}{\partial z^2}=\frac{qN_i}{\varepsilon_{si}} \quad (1)$$

$(L_{i-1} \le z \le L_i, 0 \le r \le \frac{t_{si}}{2}$, i=1, 2, 3, 4)

Where ε_{si} is the dielectric constant of silicon pillar, $N_0=N_4=N_h$, $N_1=N_2=N_3=N_c$ and $\phi_i(r,z)$ represents potential distribution.

The potential profile is approximated using parabolic function for surrounding gate MOSFET and its solution is given as

$$\phi(r, z) = c_1(z) + c_2(z)r + c_3(z)r^2 \quad (2)$$

Where the arbitrary constants $c_1(z), c_2(z), c_3(z)$ are obtained by solving and substituting the boundary conditions.

(a) The electric field in the center of the silicon pillar is zero by symmetry, so we have

$$\left.\frac{\partial \phi_i(r,z)}{\partial r}\right|_{r=0}=0$$

(3)

$L_{i-1} \le z \le L_i, 0 \le r \le \frac{t_{si}}{2}$, i=1, 2, 3, 4

(b) The electric flux at the oxide-silicon interface is continuous, and so it is given as

$$\left.\frac{\partial \phi_i(r,z)}{\partial r}\right|_{r=t_{si}/2}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\times\frac{V_{gs}-V_{FBi}-\phi_i(r,z)}{t'_{ox}} \quad L_{i-1} \le z \le L_i, 0 \le r \le \frac{t_{si}}{2}, \text{ i=1, 2, 3, 4} \quad (4)$$

Where $t'_{ox}=r\times\ln(1+\frac{2t_{ox}}{t_{si}})$, ε_{ox} is the dielectric constant of gate oxide, t_{ox} is the thickness of the gate oxide and V_{gs} is the gate-to-source bias voltage.

(c) The surface potential and electric flux at the interfaces between dissimilar metals are continuous, thus we get

$$\phi_i(r, L_i) = \phi_{i+1}(r, L_i) \quad (5)$$

$$\left.\frac{\partial \phi_i(r,z)}{\partial z}\right|_{z=L_i} = \left.\frac{\partial \phi_{i+1}(r,z)}{\partial z}\right|_{z=L_i} \quad (6)$$

i=1, 2, 3.

(d) The potential at the source end is

$$\phi_1(r,0) = V_b \quad (7)$$

Where built-in potential is given by

$$V_{b_i} = V_T \ln\left(\frac{N_i N_D}{n_i^2}\right), \quad (8)$$

$$V_T = k_B T / q \ , \quad (9)$$

k_B is the Boltzmann Constant and T is the temperature.

(e) The potential at the drain end is

$$\phi_4(r, L_4) = V_b + V_{ds}. \quad (10)$$

Using the boundary conditions (3) – (10) the surface potential is determined using parabolic approximation method as

$$\frac{d^2\phi_{si}(z)}{dz^2} - \alpha^2 \phi_{si}(z) = \beta_i \text{ i=1, 2, 3, 4} \quad (11)$$

Where $\alpha^2 = \dfrac{2\varepsilon_{ox}}{R^2 \varepsilon_{si}(\ln(1+\frac{t_{ox}}{R}))}$ (12)

$$\beta_i = \frac{qN_i}{\varepsilon_{si}} - \alpha^2 (V_{gs} - V_{FBi}) \quad (13)$$

In DHTMSG, the flat band voltages of the five parts will be different and it is given as

$$V_{FBn} = \phi_{Mn} - \phi_{si} \text{ n, i=1, 2, 3,4} \quad (14)$$

ϕ_{Mn} is the work function of the gate materials

ϕ_{si} is the silicon work function which is given by

$$\phi_{si} = \chi_{si} + \frac{E_g}{2q} + \phi_F \quad (15)$$

$$\phi_F = V_T \ln(\frac{N_A}{n_i}) \tag{16}$$

The solution of the equations using complementary function and particular integral is obtained as

$$\phi_{si}(z) = A_i e^{\alpha z} + b_i e^{-\alpha z} - \frac{\beta_i}{\alpha^2} \tag{17}$$

$0 \le z \le L_i$ i=1, 2, 3, 4

Substituting the boundary conditions, the expressions of the constants are acquired and given in equations

$$b_3 = \frac{V_{bh} + V_{ds} + \frac{m_4}{\alpha^2} - P\beta_4^{-1} + \frac{(m_3 - m_4)}{2\alpha^2} * (\beta_3^{-1}\beta_4)}{(\beta_4 - \beta_4^{-1})} \tag{18}$$

$$b_2 = \frac{2b_3\beta_2 - \frac{m_3}{\alpha^2} + \frac{m_2}{\alpha^2}}{2\beta_2} \tag{19}$$

$$b_1 = \frac{2b_2\beta_1 - \frac{m_2}{\alpha^2} + \frac{m_1}{\alpha^2}}{2\beta_1} \tag{20}$$

$$b_0 = \frac{2b_1\beta_0 - \frac{m_1}{\alpha^2} + \frac{m_0}{\alpha^2}}{2\beta_0} \tag{21}$$

$$b_4 = \frac{2b_3\beta_3 - \frac{m_3}{\alpha^2} + \frac{m_4}{\alpha^2}}{2\beta_3} \tag{22}$$

$$A_4 = -b_3 + P \tag{23}$$

$$A_3 = A_4 + \frac{m_3\beta_3}{2\alpha^2} - \frac{m_4\beta_3}{2\alpha^2} \tag{24}$$

$$A_1 = A_3 + \frac{m_2\beta_2}{2\alpha^2} - \frac{m_2\beta_1}{2\alpha^2} + \frac{m_1\beta_1}{2\alpha^2} - \frac{m_3\beta_2}{2\alpha^2} \tag{25}$$

$$A_0 = V_{bh} - b_0 + \frac{m_1}{\alpha^2} \tag{26}$$

$$A_2 = \frac{A_4\beta_2^{-1}\beta_3^{-1} + b_2\beta_2\beta_3^{-1} - b_4\beta_3\beta_2^{-1} - b_3\left(\beta_2\beta_3^{-1} - \beta_3\beta_2^{-1}\right)}{\beta_2^{-1}\beta_3^{-1}} \tag{27}$$

Where,

$$P = \frac{m_3\left(\beta_2^{-1} + \beta_2 - \beta_3\right) + m_2\left(-\beta_2^{-1} + \beta_1^{-1} - \beta_2 + \beta_1\right) + m_1\left(-\beta_1^{-1} + \beta_0 + \beta_0^{-1} - \beta_1\right) + m_0\left(-\beta_0 - \beta_0^{-1}\right) + m_4\beta_3}{2\alpha^2} + V_{bh} + \frac{m_1}{\alpha^2}$$

$$\beta_i = e^{\alpha L_i} \qquad \beta_i^{-1} = e^{-\alpha L_i}$$

3. RESULTS AND DISCUSSIONS

The performance of the dual halo triple material surrounding gate (DH-TMSG) MOSFET is studied by analyzing the surface potential. Simulation parameters: $V_{gs} = 0.1V$, $V_{ds} = 0.5V$, $t_{ox} = 4nm$, $t_{si} = 60nm$, $N_h = 3X10^{18}cm^{-3}$, $N_c = 10^{16}cm^{-3}$, $N_D = 10^{20}cm^{-3}$, $L_0 = 15nm$, $L_1 = 30nm$, $L_2 = 45nm$, $L_3 = 55nm$, $L_4 = 60nm$. The work functions of the three metals M_1, M_2 and M_3 are 4.8, 4.7 and 4.2 respectively.

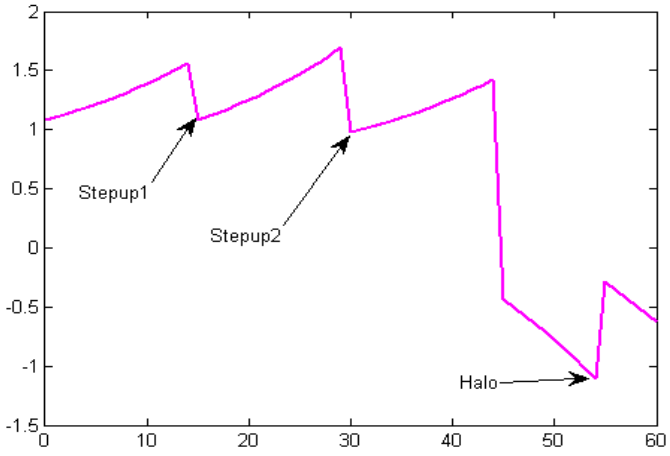

Fig2. Surface potential of DH-TMSG MOSFET

The surface potential distribution of DHTMSG structure acts as Y-axis and the X-axis denotes the distance from source which is plotted in figure2. It can be seen that the minimum surface potential occurs in the halo parts for DH-TMSG and it is still lower compared to TMSG and HDSM structure. In the proposed DH-TMSG structure, there is an extra potential step on the right and left of the minimum surface potential. There exists a first potential step near the boundary of the first two different metals and the second step up near the interface of the next two metals which improves the short channel effects.

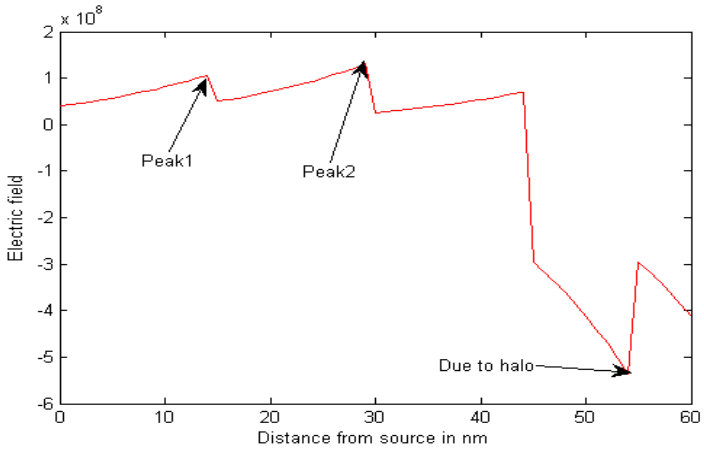

Fig3. Electric field of DH-TMSG MOSFET

The electric field of DH-TMSG is shown in figure3. It can be seen that the electric field has peaks due to material interfaces and minimum points over halo regions which improves the performance of the device. The increase in halo concentration improves the starting value and final peak while the increase in work function improves the second and third peak thus increasing the speed up of carriers. This produces better performance and current drive capability.

4. CONCLUSION

The 2D analytical model is developed for surface potential and electric field of dual halo triple material surrounding gate MOSFET (DHTMSG). It is shown that DHTMSG shows better performance in suppressing the short channel effects and hot carrier Effects. The peaks and step up obtained in the halo boundaries of the device makes the carriers travel through the channel more quickly. DHTMSG provides more proficient process for augmenting the performance.

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