Roadmap on Low-power Electronics

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I. Broad Overview:

A Roadmap for Low Power Computing: Materials for a Sustainable Microelectronics Future

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I. Summary: This article is written on behalf of many colleagues, collaborators, and researchers in the field of advanced materials who continue to enable and undertake cutting-edge research in the large field of low power computing. What I present is something that is extremely exciting from both a fundamental science and applications perspective and has the potential to revolutionize our world, particularly from a sustainability perspective. To realize this potential will require numerous new innovations, both in the fundamental science arena as well as translating these scientific discoveries into real applications. I hope this article (and this roadmap) will help spur more fundamental as well as translational research within the broad materials community.

II.Introduction: Before, I get into the specific topic of this paper, namely energy efficiency in computing, it would seem to make sense to give a broader energy perspective. In 2010, I was asked by Energy Secretary Steve Chu to join him in the US Department of Energy to lead and articulate the DOE Sunshot Initiative. The name "Sunshot" was coined to bring back memories of the original "Moonshot" Initiative, which led to the Apollo program and galvanized the U.S. into action in the space race. Sunshot was meant to galvanize a different generation, to focus on clean energy and in doing so solve the biggest problem of our lifetime, namely Climate Change. In 2010, solar electricity was about 5X more expensive than electricity from fossil fuel (for example, the levelized cost of electricity in the U.S was ~5c/kWh in the wholesale market; compared to that solar was ~27c/kWh, leading to the factor of 5X difference). The Sunshot challenge, therefore, was this: how does one bring the cost of solar electricity down by a factor of 5X? I note that a 5X reduction of the cost of any technology in a commodity market with small margins, is extremely difficult; indeed, this is one of the main reasons that the incumbent technologies are so difficult to displace, since they have already built up the economies of scale and captured market share. Furthermore, the challenge from Secretary Chu was that we should use the power of Science and Technology to solve this rather than revert to policy pathways. Thus, we needed a holistic approach, bringing together innovations in the hardware side as well as in market transformations and manufacturing. The cost of solar electricity has come down dramatically over the last decade, reaching the Sunshot target well ahead of the originally set 2020 target (REF: US Department of Energy). Of course, this dramatic drop in the cost of solar electricity was aided by the corresponding drop in the prices of solar panels due to large scale manufacturing in China. Sunshot was thought to be a success of the Steve Chu administration, perhaps mainly for the fact that an aggressive target was set by the federal government and a clear game plan was articulated and executed. A broader impact of the Sunshot Initiative manifested itself during the recent transition to the Biden-Harris administration in 2020-2021. I had the opportunity to participate in the transition team, focused on the Department of Energy. In doing so, I had the privilege of working with some amazing scientists, engineers, policymakers in the Energy Transition Team, on identifying the top priorities, given the administration's focus on Climate Change, eradicating the COVID-19 pandemic, creating a more environmentally just investment as well as build back jobs and manufacturing. Based on our learning from the Sunshot Initiative, we proposed a set of "Earthshots", focused on large, tough problems in Energy and Climate Change. All the five proposed Earthshots had measurable, quantitative success metrics. One of them focused on a 1000X increase in Energy Efficiency in

Microelectronics. The rest of this article (and this roadmap) tries to capture the science & technology challenges required to bring the energy consumption down in Microelectronics.

II.1 The Macro-systems Perspective: We begin the discussion from a broad, macro-systems perspective. Microelectronics components and systems form an ever-increasing backbone of our society. Computing devices have pervaded many parts of our daily life, for example through a host of consumer electronics systems, providing sensing, actuation, communication, and processing and storage of information. All of these are built upon an approximately $570B/year global market that is growing at a steady pace of ~15% annually[1,2]. Many of these innovations started as materials research ideas, often first discussed within the hallways of the many physics and materials conferences worldwide. The emergence of a few new global phenomena will change this landscape dramatically. The first among them is the notion of the "Internet of Things" (IoT) [3], "which is the network of physical devices, vehicles, home appliances, and other items embedded with electronics, software, sensors, actuators, and connectivity which direct integration of the physical world into computer-based systems, resulting in efficiency improvements, economic benefits, and reduced human exertion" [4]. Thus, it is not inconceivable that every modern building will be outfitted with millions of sensors and actuators that can dynamically optimize the energy consumption dynamics of that building. Similarly, a modern automobile has many sensing, communicating components embedded. While still in its infancy, it is possible that driver-less automobiles, for example, will be a routine aspect of our life twenty years from now.

The second major phenomenon is the field of machine learning (ML) / artificial intelligence (AI), that is taking the technology world by storm. It uses a large amount of statistical data analytics which, in turn, provides the computing system the ability to "learn" and do things better as they learn, not unlike normal human beings. While there are several scientific disciplines that come into play, of relevance to us is the fact that microelectronic components are critical underpinnings for this field.

II.2 Do we need a new paradigm for computing? We can now ask the question: how do these global phenomena relate to microelectronics and, more importantly, to new materials? Or stated in a different way, what can *materials physics* do to enable this coming paradigm shift? To put this into perspective, we now need to look at the fundamental techno-economic framework that has been driving the microelectronic field for more than five decades. This is the well-known "Moore's Law", which underpins the field of microelectronics through the scaling of CMOS-based transistors (**Fig. 1**). Broadly, it states that the critical dimensions of the transistor shrink by 50% every 18-24 months. At its inception, CMOS transistors were "macroscopic" with the critical dimension well over 1 μm. In 1974, a path to shrinking such transistors, at constant power density was proposed[5–7] and was followed for the next 30+ years. Today, however, this so-called Dennard scaling is no longer sustainable while the critical dimensions of modern transistors are rapidly approaching sub-10 nm scales; the point at which both the fundamental science (*i.e.*, classical electron dynamics) no longer more suffices to adequately understand operation and ever more complex manufacturing issues must be addressed. In the past 5-8 years, there has been an ever-increasing sense that something has to be done about the energy efficiency of computing[8–12].

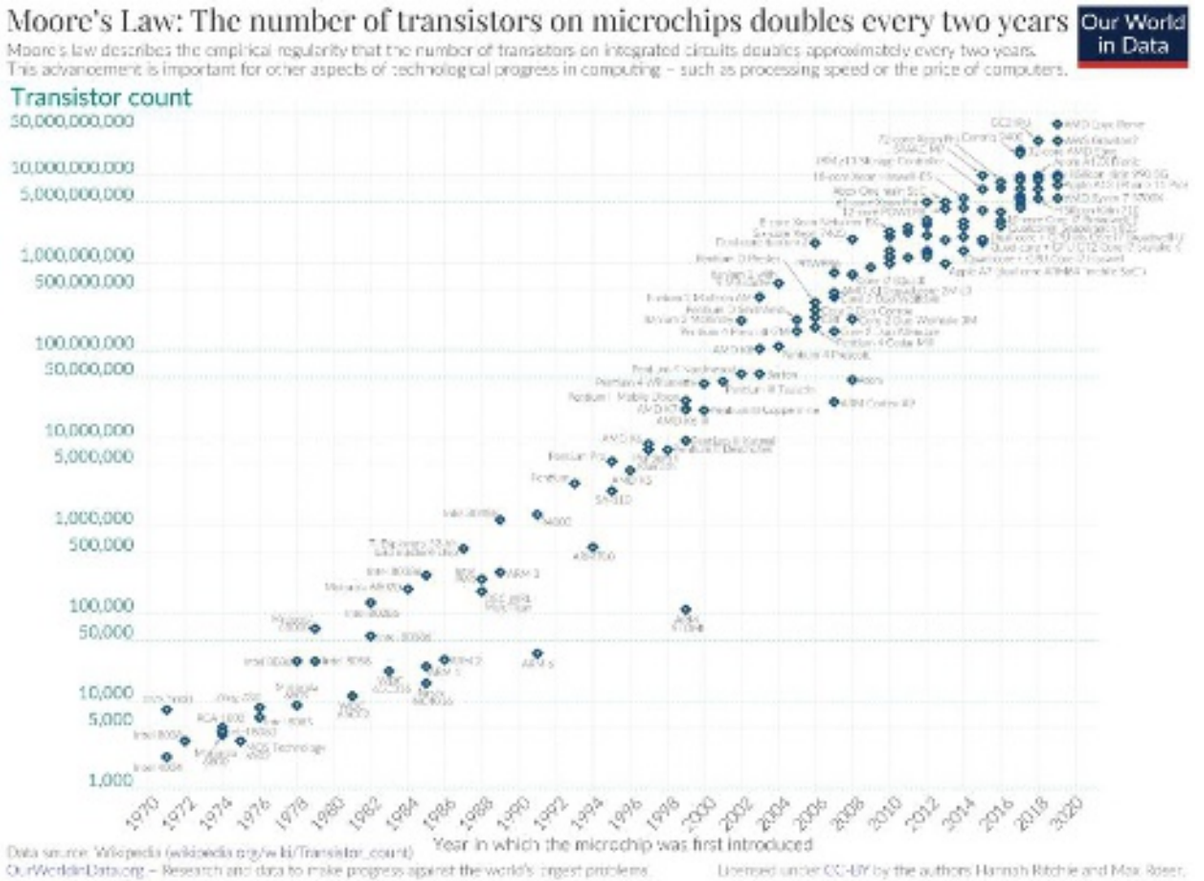

Fig.1: A manifestation of Moore's Law, leading to the doubling of the number of transistors on chips every ~2 years

II.3 Energy Efficiency in Computing: As if this combination of challenges was not enough, we have yet to introduce perhaps the single most important aspect into consideration: energy consumption (**Fig. 2**)[13]. Of the many issues modern technologists must address, the one we highlight here has the potential to be the most impactful from a sustainability perspective, namely **energy**. The energy consumed per

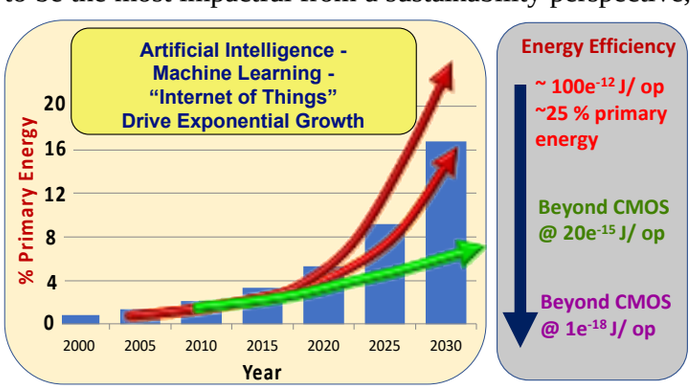

Fig.2: A plot of fraction of primary energy consumed in Microelectronics for three different scenarios. The plot in RED is for the status quo and the lower plot in RED is for Beyond CMOS @ 1 fJ/logic operation. The plot in GREEN is for Beyond CMOS at 1aJ/logic operation.

logic operation, which in today's CMOS transistor is of the order of 50-100 pJ/logic operation (note that this actual number may be debated, but it remains that the energy consumed is of the order of pJ/operation). For the sake of discussion, lets assume that there is no change to this number soon, but,

at the same time, the demand for and consumption of microelectronic components in IoT and AI/ML will grow exponentially. Consequently, it is quite conceivable that the total energy consumption in all of microelectronics could grow to ~25% of primary energy by 2030[14]. Today, it is of the order of 5-7% and thus is not of great concern, especially in contrast to sectors such as buildings, which consume ~38% of the total energy consumption, or transportation which consumes ~24% (fractions noted here are for the United States). At the scale of ~25% of primary energy, microelectronics would become a serious component of the worldwide energy consumption mix and thus deserves to be addressed from the energy efficiency perspective as well. Thus, these three global phenomena, namely the emergence of IoT and AI/ML as well as the end of Moore's Law (including aspects of dimensional constraints and total energy consumption in microelectronics) forms the backdrop for our discussion as we ask: **what can we do with new materials physics**?

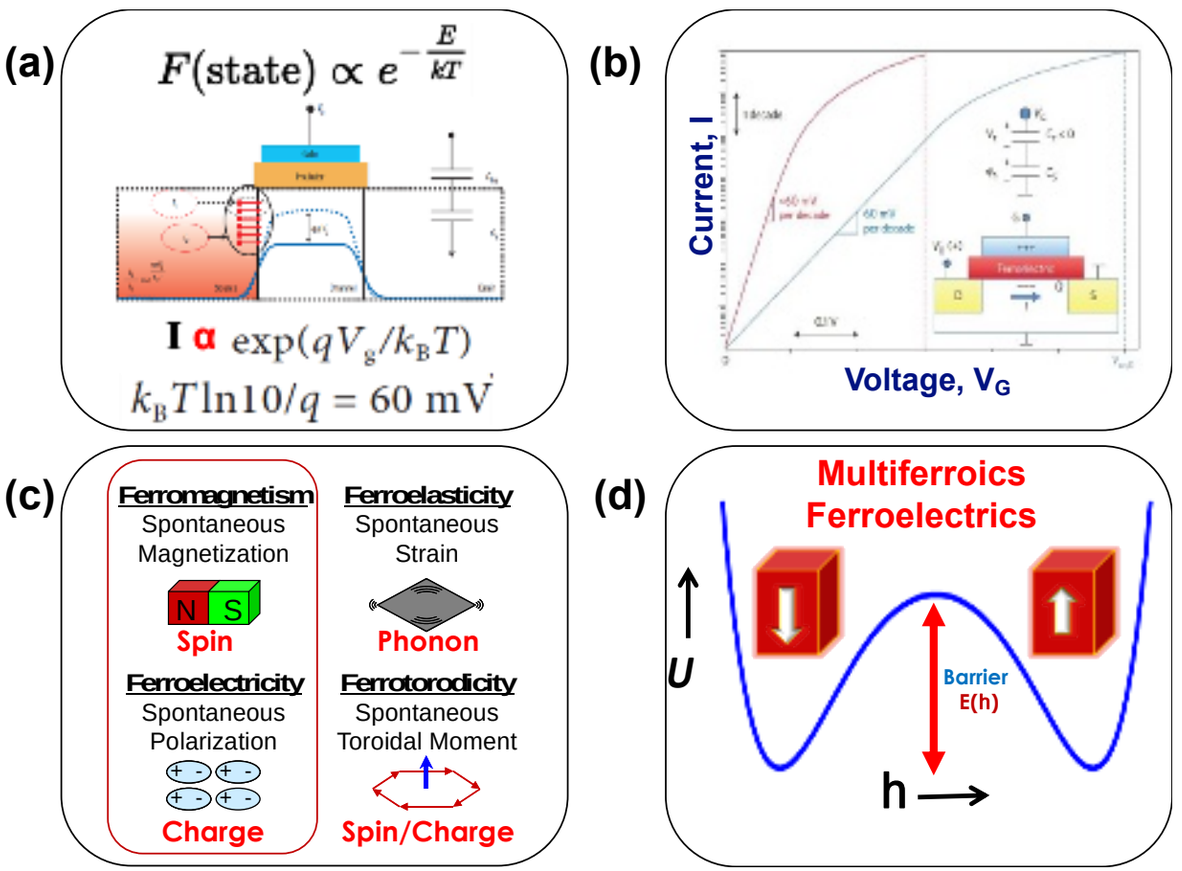

Fig.3: (a) a schematic of a Si-CMOS channel with the "Boltzmann Tyranny" equation at the bottom; (b) A schematic I_d-V_g plot for a standard CMOS channel (IN GREEN) versus that with a ferroelectric gate (in RED); (c) Possible pathways to incorporate the spin degree of freedom (ferromagnetism) breaking time reversal symmetry, dipolar order breaking spatial inversion symmetry (ferroelectricity), spontaneous strain (ferroelasticity) and spontaneously broken time and inversion symmetry (Ferrotoroidicity).

II.4 The opportunity for new materials science leading to technology: The microscopic behavior of the electronic charge in a CMOS transistor is governed by the Boltzmann distribution (**Fig. 3(a,b)**)[15]. A quick analysis shows that the current changes exponentially with voltage, with a slope of 60 mV/decade of current[12], termed as the "Boltzmann Tyranny"[1,11] since the Boltzmann physics is

imposed on the functioning of the actual device. In real transistors, this voltage slope is typically larger. This fundamental behavior is central to the performance of the transistor, both in terms of the voltage required and the energy consumed in the process of operating the transistor. In recent years, there has been the realization that the Boltzmann Tyranny needs to be addressed – thus the need for new materials and materials phenomena. One proposed pathway is to use materials exhibiting a metal-to-insulator transition, such as in correlated-electron systems. Under ideal conditions, such a metal-to-insulator transition can be very abrupt. Another key realization, which is described in a seminal review[1], identifies the broad class of quantum materials as possible candidates to overcome this tyranny, mainly through the insertion of an additional, internal interaction energies into the Boltzmann distribution, Fig.3(c,d). For example, this could be the exchange interaction in a ferromagnet or the dipolar interaction in ferroelectrics. In its simplest form, such an interaction can be represented by an additional term in the Hamiltonian that represents the exchange interaction energy for a magnet given by: $E_{ex} = -J \cdot S_1 \cdot S_2$, where J is the exchange integral and S_1 and S_2 are the two neighboring spins (or the corresponding dipolar energy in the case of a ferroelectric). This term then becomes the key component within the Boltzmann distribution function, and it modifies the energy landscape. In simpler terms, the exchange energy (or the dipolar energy in a ferroelectric) makes the spins (or the dipoles) align collectively *without the need* for an external source of energy. Thus, if one could use spin or a spontaneous dipole as the primary order parameter rather than merely the electronic charge in a CMOS device, one could take advantage of such internal collective order to reduce the energy consumption. Indeed, this is the premise behind two recent proposals [1,10], where the rudiments of a possible magneto-electric spin orbit (MESO) coupled memory-logic device are discussed. While many parts of this device require further detailed study and innovations, one aspect that we will focus on, pertains to advanced materials and electric-field control of magnetism.

This forms the backbone for the articles in this Roadmap, which is formatted into three sections. The first section provides some broad perspectives of a field that is moving rapidly. Some examples provide the illustrations for how one could approach energy efficiency in computing. The second section focuses on specific technology pathways, again focusing on energy efficiency. The third section details the challenges and opportunities in processing and metrology, as the various technologies progress towards high energy efficiency.

Energy Efficient Electronics – Research Needs and Outlook

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Introduction:

The need for information processing has been accelerating over the last few decades. Computing now impacts every aspect of human life and is a critical enabler in the battle against the most pressing challenges of our time such as in health care, sustainability, poverty and world hunger. As big data analytics become increasingly mainstream for automation and efficiency, the need for computing is only going to accelerate. But computing is not free. When crypto currency mining became popular, the energy bill that the mining machines were generating increased exponentially. In fact, after the early years, the prohibitively expensive energy bills made crypto mining economically unsustainable for many. While the crypto currency miners brought the issue of energy consumption in powerful computers to the attention of the rank and file, to the community of researchers in the computing field, this has already been known and a matter of intense research since the early 90's. Indeed, power consumption is why clock frequency scaling ended in the early 2000's and computers pivoted toward multi-core architecture. A recent study[16] by the Semiconductor Research Corporation (SRC) shows that the rate of increase in the energy used for computing is significantly larger than that of the world energy production and the computing energy is slated to account for a significant percentage of world's energy consumption by early 2030's. This underscores the need for substantial lowering of energy in computing hardware.

Fundamentals of Energy Dissipation in Electronics:

There remain significant opportunities for optimization in computing architecture that lowers overall energy. Indeed, in recent years, a rethinking and re-optimization of software, algorithms, and hardware architecture at or near the top of the computing stack have yielded substantial gain in energy and performance[17]. In this article, we focus on the technology aspects – the basic building blocks of the computing hardware at the bottom of the computing stack – where an improvement in energy efficiency acts as a multiplier to any gain achieved through architectural design optimization. Interestingly, recognizing the fact that the computer is essentially an R-C circuit (R: resistance, C: capacitance), the opportunities for optimization can all be identified as enabling physics, materials and transistors that improve energy, CV^2 (V: operating voltage) and delay, CV/I (I: current). In short, one desires lower C, lower V and larger I. It should be noted that the capacitance of the wires dominates the capacitance of the transistors – as a result the transistor capacitance itself does not contribute significantly to the overall energy consumption. On the other hand, the operating voltage is determined by the voltage needed to operate the transistors. Therefore, the V and I are dictated by the transistors whereas the C is dictated by the wires. It should be noted, however, that the delay, CV/I, is affected by the transistor capacitance because the device capacitance will often determine the logic depth that can be supported for a given speed.

Potential pathways to energy efficiency:

Intrinsically, V is determined by two requirements. Above the threshold, a certain voltage is necessary to reach the desired ON current or I, which is a product of the capacitance (gate oxide capacitance) and velocity. Substantial research culminated in the adoption of high-κ, metal gate around 2008, enabling the devices to reach very large gate capacitance[18]. However, improvement in gate capacitance has stalled since then. Essentially, further reduction of the thickness of the high-κ HfO_2 layer and/or reduction of the interfacial SiO_2 layer (IL) leads to unacceptable increase in leakage and/or degradation of reliability. Recently, ferroelectric-dielectric superlattices has been shown to significantly increase gate capacitance through the Negative Capacitance (NC) effect beyond classical HfO_2 based gate

oxides without degrading leakage or reliability[19]. This shows a pathway towards reducing V. Further improvement through the NC effect and improvement of the Si/SiO_2 interface chemistry to enable a thinner IL should substantially reduce the voltage requirement. Increased gate capacitance has the added benefit of reducing short channel effect that lowers the OFF current, a topic that we address next.

A second requirement on V comes from the OFF current (I_{OFF}) considerations – voltage swing needed below the threshold to reach a desired I_{OFF}. In this context, tunnel FETs, that can filter off the high energy tail in the Boltzmann distribution of carriers injected from the source into the channel and thus provide a lower I_{OFF} at the same voltage swing, have been explored for many years[20]. Indeed, recent results show the efficacy of this approach, at least for compound semiconductor devices[21], albeit with lower on-state current (I_{ON}). The NC effect, when it is strong enough to overcome the capacitance of the inter-layer (IL) dielectric, is also expected to lead to a steeper subthreshold voltage swing. In fact, the NC effect and tunneling can be combined in the same device for a multiplicative effect. One added advantage in this approach is that the ON current of the tunnel FET can be boosted by the NC effect[22].

Of course, one way to substantially lower the voltage below threshold is to lower the operating temperature. Low temperature operation has been investigated sporadically over the last several decades with limited success. Currently, however, the simultaneous occurrence of extreme increase in computing needs and associated power dissipation and newly available technology in terms of high gate capacitance and precise control over the threshold voltage may finally make it possible to achieve a net gain in energy and performance from low temperature operation. Estimates show that highly optimized CMOS transistors with re-targeted threshold voltages enabled via gate work function engineering, extremely thin equivalent oxide thickness, e.g., achieved via the NC effect, and low external resistance via contact engineering, when operated at T=77K, may indeed lead to a net gain in energy and performance after factoring in the cost of cooling[23,24].

Many materials boast much larger mobility of electrons and holes than silicon. These materials could increase the on-state current and simultaneously reduce the voltage needed to reach the saturation velocity[25]. However, one needs to keep in mind that the ON-current is the product of charge and velocity and both are important. Often compound semiconductors with low effective masses are plagued by low density of states making it difficult to obtain large currents (notably, this does not limit their transit time as that only depends on velocity). Another aspect of new materials is to take advantage of their low dimensionality such as in one dimensional carbon nanotubes or two-dimensional transition metal di-chalcogenides – low dimension allows better gate control for the same gate capacitance[26], which in turn can lower the voltage swing needed to reach a desired I_{OFF}. For any channel material other than silicon, one would also need to solve the gate oxide reliability that for silicon has proved to be a critical issue and had to be resolved every time any change was made to the gate oxide. The present trend is to explore a wide range of materials in search of the best available property. Eventually a specific material will have to be chosen and interface chemistry and gate oxide integration as well as threshold voltage tunability will have to be established for technological adoption. In addition, the ability to make good contacts with new materials is also a critical research problem. More about good contacts next.

Extrinsic Effects

So far, we have mostly discussed aspects that affect the intrinsic behavior. However, for the most advanced devices, extrinsic effects are equally important, if not more. The first is contact or series resistance. This is a fundamental challenge – as the footprint of the contact reduces with scaling, its

resistance increases, increasing the voltage drop across this 'unwanted resistance'. The series resistance therefore is a critical barrier to lowering the operating voltage. Notably, due to the band-alignment of metal and semiconductors, almost all contacts are Schottky type, meaning they operate by quantum mechanical tunneling through the barriers. Traditionally, doping of the semiconductor has been used to reduce the width of the barrier and lower resistance. However, the time is ripe to go beyond the conventional approach. Indeed, recent efforts have explored unpinning of the Fermi level at the interface and thereby reducing the barrier height[26]. For low dimensional materials, an added difficulty is the mode mismatch – whenever charge carriers leave the low dimensional material and enter a higher dimensional material or vice versa, they encounter a substantial mismatch in the number of modes – that leads to resistance[27]. Is it possible to exploit other mechanisms (e.g., improving the matching of density of states on either side of the interface) that can substantially improve tunneling? This seems to be well poised as a fundamental challenge for the device community.

Scaling of the gate length decreases the footprint of the gate contact, increasing the gate resistance. This is especially critical for the modern gate replacement process where the gate metal is smaller than the lithographically defined channel length. Similarly, reduction in the footprint of the contact holes increases resistance of the interconnects. Filling up very small diameter holes with high aspect ratio, while still maintaining large grain size and therefore reasonable resistance is another daunting challenge of today's computing hardware. In the most recent nodes, we have seen adoption of cobalt and ruthenium as a source drain contact metal[28]. Improving contact resistances both for the gate metal and interconnects is of critical importance and is ripe for materials and physics innovation[29].

Continuing on with the extrinsic effects, about half of the capacitance observed at the gate of a FINFET transistor comes from parasitic capacitance. For Gate-All-Around transistors this ratio can in fact go up even more. Notably, the parasitic gate capacitance has no connection to the intrinsic device and does not lead to increased current, I – rather now the device will have to carry this extra 'load', leading to an increased delay, CV/I. This means that to maintain a given delay the current, I, has to be increased, which eventually requires V to increase. So, finding ways to reduce parasitic capacitance is of paramount importance. Is it possible to implement air-gap spacers[30] in the transistors following what has been done at the lower metal levels[31]?

Back end technologies to aid Energy Efficiency:

In the context of reducing the impact of wire capacitance on energy consumption and information throughput, another trend has recently gained significant traction –to limit data movement through the long wires that extend off-chip, by monolithically integrating memory with logic transistors. The potential benefit is significant – if substantial memory can be integrated on chip, it saves the long wires with enormously large capacitance that is needed to go off-chip. Effectively it reduces significant capacitance of the interconnect. In addition, it may also alleviate the need to use higher voltage I/O transistors as there is no need to supply a substantial capacitive load. This can lead to very significant savings in power consumption. While this approach does not directly rely on improving the wires themselves, practical implementation requires substantial advances in integration as all components have to be compatible with Back-End-Of-the-Line (BEOL) processing. Substantial effort is currently in place, both in academia and industry, to explore memory devices that are on-chip embeddable. Resistive random access memories and magnetic random access memories have received much attention in this regard along with phase change memory which is already commercial as a stand-alone memory technology[32]. The ultimate benchmark for any on chip memory is the SRAM – substantial advance in either density or latency will be needed to make an impact in this context. With the potential

for large amount of on-chip memory, computing in memory (CIM)[33] has recently garnered a lot of interest, especially for AI workloads where CIM could substantially reduce energy and latency associated with matrix vector multiplications. This is an example where device, algorithm and architecture are co-optimized to offer substantial system level benefit. However, for CIMs to be successful, energy associated with analog-digital conversion has to be kept small – currently considered a significant challenge.

Along the same direction, recent years have also seen substantial research in semiconducting oxide transistors as a potential cell transistor, or a drive transistor[34] to enable 3D integration of memory on top of the logic components. In addition to being amenable for BEOL processing, semiconducting oxides have large bandgap that allows very low leakage current that is advantageous for certain applications such as a DRAM transistor. However, challenges remain in terms of achieving the desired ON current, while holding on to a low leakage within a small voltage swing. Another challenge is the generation of oxygen vacancies with continuous voltage cycling that may lead to substantial threshold voltage shift and accelerated aging of such transistors. In addition, a p-type oxide channel has remained elusive to date[35] despite substantial research in the last few years. Nonetheless, the potential benefit for a 3D integrated oxide channel transistor is substantial, and innovations in new materials and advances in understanding of defect formation in such materials and novel defect mitigation strategies are of critical importance.

Conclusion:

The last decade has seen a new trend in electronic devices. Going beyond just geometric scaling, functional improvement of various components by introducing new materials and novel physics is becoming increasingly common[12]. There is also a growing acceptance of the need for domain specific device technology, making the flavors of devices used on a chip increasingly larger every generation (this is being accelerated even more via heterogenous integration). These trends make the next decade particularly exciting for materials, physics, process integration and device innovation that will deliver increasingly improved energy efficiency.

Low-Power High-Performance Electronics

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Overview

The quest for sustainable growth in computing performance and expanded functional capabilities of information technology and communication (ICT) products requires energy-efficiency improvements of underlying technologies in devices, systems, architectures, algorithms and software, and information representation and processing. Bridging the gap between existing silicon nanotechnology and future VLSI needs innovations in devices and interconnect fabrics, each and all-cohesively enabling higher integration-density, performance improvements, and capabilities at lower power consumption cross-generations. Continued growth in computing capacity requires significant improvements in energy efficiency for it to be sustainable as illustrated in Fig. 4 adapted from the SRC-SIA Decadal Plan of Semiconductors[16]. Artificial intelligence (AI) is a key element in the fourth industrial revolution. Increased cognitive capabilities are key to next generation AI, attaining them while decreasing the power consumption, as illustrated in Fig. 5, will be critical regardless of application domain. The quest for the necessary energy efficiency requires innovations at all levels from the basic technology structures and building blocks to the system architectures and algorithms including novel forms of information representation and processing, c.f.[36]. Research and development monumental efforts on silicon-based CMOS technology scaling continuously raise the bar on energy-efficiency, performance, density, reliability, and cost that exploratory devices, interconnects, and novel integration concepts ought to meet to be of impactful technological value. This section discusses emerging transistors, memories, and interconnect fabrics. It highlights open research areas, the necessary completeness of the metrics in research, and associated modeling challenges to identify viable alternatives to beyond the projected evolutionary paths of state-of-the art technologies.

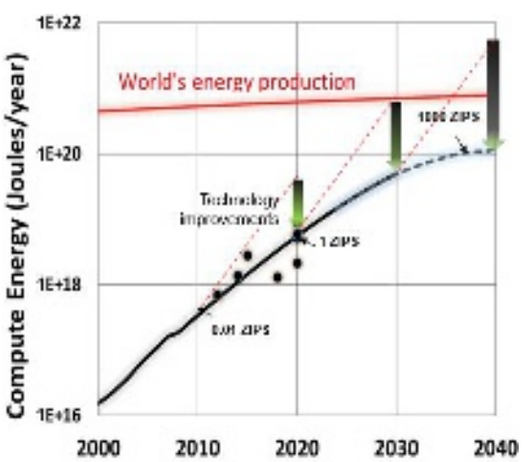


Fig. 4. Sustainable computational capacity growth requires continuous technological innovations enabling necessary energy-efficiency demands[16].

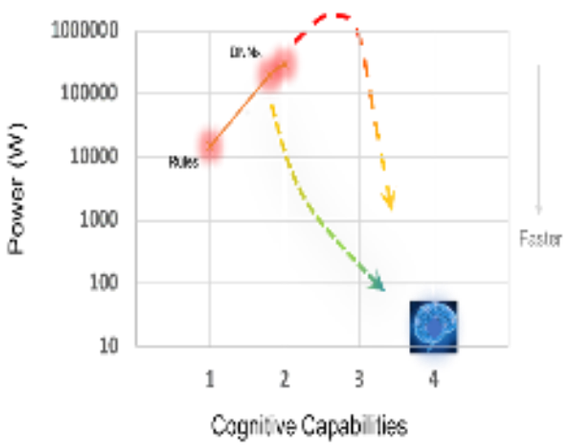


Fig. 5. Increasing AI capabilities towards human-level cognition hinge on energy-efficient innovations in information representation and processing and the semiconductor technologies.

Transistors

Power supply scaling is a critical knob in boosting energy efficiency from generation to generation, capacitance being the other. The optimal nominal operating voltage (minimum) for a given speed goal is bounded to the left by leakage power and to the right by active power as illustrated in Fig 6. To retain or improve switching speeds while also reducing power supply, materials with significantly better transport properties than silicon are needed as shown in Fig. 7. One such candidate is germanium where research efforts on addressing critical challenges such as reliable and scalable CMOS-capable gate-dielectrics and n-type doping challenges made significant inroads, c.f.[37]. Transistor structures such as stacked gate-all around channels will enable improved electrostatic control / steeper subthreshold slope than present Fin-FETs resulting in significant reduction of minimum operating voltages as shown in Fig. 8[38].

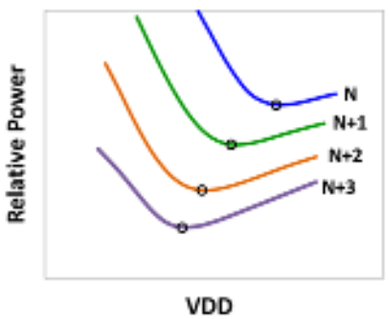


Fig. 6. Power supply scaling critical a fundamental knob for cross-generation enhancements in power scaling, energy-efficiency enhancements.

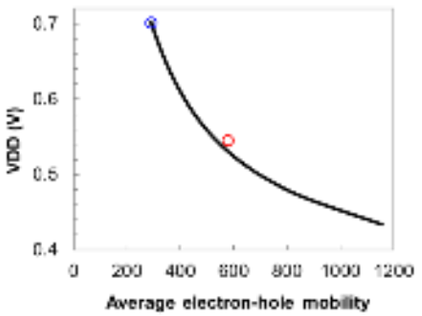


Fig. 7. Channel materials with significantly better transport properties key to boost drive strength and circuit speed while scaling power supply.

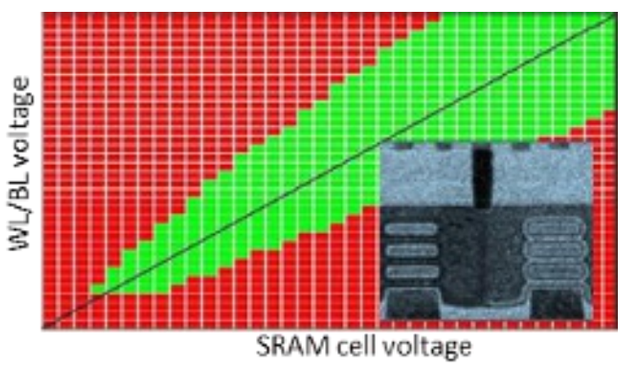


Fig. 8. Stacked gate-all-around channel structures to enable V_{DD} scaling beyond Fin-FETs, c.f.[38].

Exploratory work on low-dimensional materials such as transition metal di-chalcogenides (TMDs) [39], arm-chair graphene nanoribbons (aGNRs) [40,41], or semiconducting carbon nanotubes (CNTs) [42] seek to demonstrate their potential for higher performance at lower operating voltages than silicon-based state-of-the art logic transistors and their projected evolutionary paths; key metrics include CMOS capability, drive current per unit footprint, off-state leakage, reduced parasitic capacitances, and reliability, among others.

Synthesis of device-quality channel materials continues to make significant fundamental inroads. The growth of carbon nanotubes by iron-catalyzed CVD along with an electric field modulation of the semiconducting-CNT nucleation energy (electro-re-nucleation) introduced by Wang et al. established

a viable path for the synthesis of high-purity semiconducting CNT arrays as illustrated in Fig. 9 adapted from[43]. Further work is needed to demonstrate high purity arrays (arrays with << 1ppm metallic CNTs) while also supporting high density (sub 5nm pitch) semiconducting CNTs within the array. Meanwhile, the GNR bottom-up synthesis of graphene nanoribbons from monomer precursor(s) continues to advance, c.f. [40,44,45], demonstrating uniform-width ribbons along the growth direction but also in proving concepts that can produce nanoribbon hetero-structures as illustrated in Fig. 10. The bottom-up synthesis of a-GNRs provides a pathway to monodisperse ribbons having atomically smooth edges, a necessary characteristic to support the projected high-performance potential of a-GNR based logic transistors. Albeit current methods may suffice to validate transport properties at single transistor-level, further fundamental research work is needed to consistently produce long-enough ribbons (> 100nm), pre-empt ribbon edge defectivity, and to conceptualize and proof-concept the regular placement and orientation of ribbons in an array on a substrate.

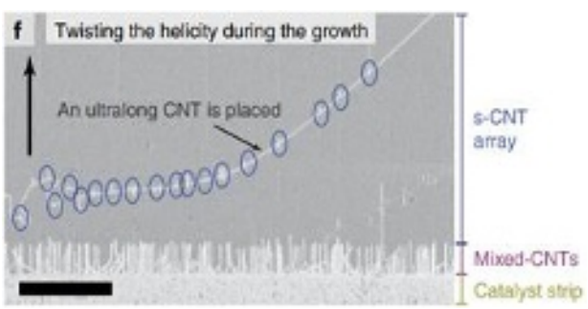
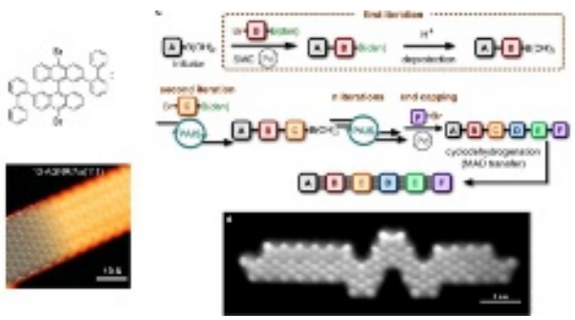


Fig. 9. Iron-catalyzed CVD growth of CNTs made significant inroads for the synthesis of high purity oriented semiconducting CNT arrays by the introduction of electro-re-nucleation concept [43].



(a) Ref. [40]. (b) Ref. [45].

Fig. 10. Bottom-up synthesis of graphene nanoribbons from monomer precursor(s) opened paths for their exploration towards logic high-performance low-voltage transistor applications.

Low resistance contacts are critical to asserting the performance potential of new transistors based on those novel channel materials. Figures 11 and 12 illustrate some of the best results to date for contacts to 2D TMDs and CNT channels respectively, c.f.[46–50]. Low-resistance contacts, particularly n-type, and the thermal stability under standard CMOS processing thermal budgets and standard operating condition requirements remain outstanding fundamental research challenges that needs to be addressed for contacts to these and other novel channel materials.

The unreactive nature of the surfaces in device-quality CNTs, a-GNRs, or 2D TMD channel materials constraints the formation of the corresponding gate dielectrics or interlayers to physisorption, c.f. [51,52]. This process requirement appears key to preserve the carrier transport properties that make these materials potential alternatives beyond silicon-based channels. Top-gated CNTs with ALD interlayer dielectrics produced in this way have been shown to support good subthreshold slopes of about 65mV/dec down to 15nm gate lengths [42]. Further fundamental research is still necessary to address the scalability and reliability of corresponding high-k gate-dielectrics, their CMOS thermal budget and process compatibility, and the demonstration of associated metal gate-stacks supporting multiple work-functions.

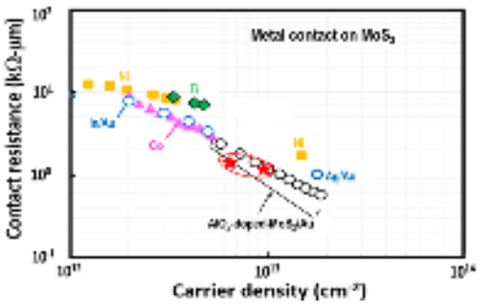


Fig. 11. Chart adapted from [46]. Notwithstanding reported improvements in contact resistance to 2D TMD channels, stable and CMOS compatible low-R contacts are still to be fully demonstrated.

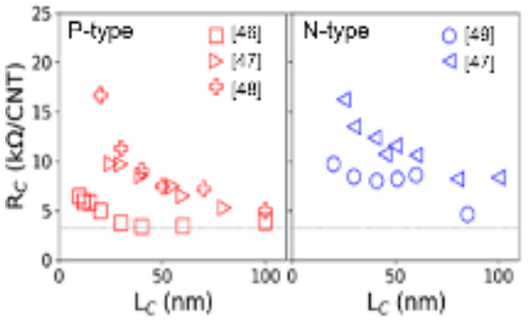


Fig. 12. Advances in low resistance contacts to CNT channels. Lower resistivity contacts that are also thermally stable require continued research.

Despite the advancements on transistor exploratory work, theoretical and experimental fundamental work that is holistic in terms of the critical transistor metrics is still required to identify true platform-viable alternatives to silicon-based CMOS transistors. Comprehensive and predictive, fundamental transport models that can realistically project on and off-state capabilities including thermally, and mechanically stable low-resistance contacts remain imperative. Also, key are the reduction in turn-around time (TAT) for fundamental screening of new materials synthesis and processing concepts through multi-scale modeling.

Memory Elements

A representative compute memory hierarchy of a computing system is shown in Fig. 13. Emerging memory devices in each level of the memory hierarchy must outperform incumbent technologies on critical indexes to be considered promising alternatives. Those critical indexes include density, energy efficiency, speed, endurance, retention, environmental robustness, controllability, and complexity as proxy to cost/bit. Spin-orbit-torque MRAM (SOT-MRAM) fast-enough write-speeds and inherent endurance capabilities make this memory class a potential alternative to standard 6T-SRAM memory cells. In-plane (magnetization) type-Y SOT-MRAM cells, illustrated in Fig. 14, leverage the shape anisotropy of the magnetic tunnel junction stack to enable field-free write operation at relatively low write currents, c.f. [53,54]. However, type-Y SOT-MRAM cell size scalability is a fundamental challenge largely related to the requirements on shape anisotropy. As such, active research continues to be directed towards enabling field-free and low write current operation of perpendicular SOT-MRAM cells, specifically identifying and demonstrating materials with high spin generation and spin injection efficiency into the associated MTJ cell stack are paramount to meet attain write-currents that can be significantly lower than those of state-of-the art high-density SRAM cells while supporting also tight write-error rates and magnetic immunity requirements, c.f. [55,56]. Ferroelectric memories are also subject of active research for their high density and energy-efficiency potential[57], progress in understanding and resolution of endurance has recently been reported[58] as shown in Fig. 15.

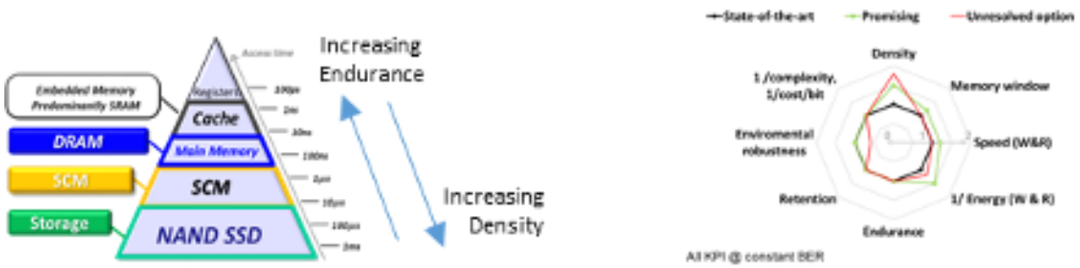


Fig. 13. Memory hierarchy and key research metrics.

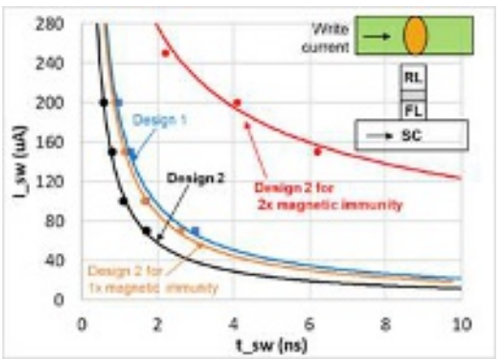


Fig. 14. SOT-MRAM type-Y and type-Z cells can support fast field-free operation. Low write current density, magnetic immunity, write speed, and bit-error rates remain challenging, c.f. [54–56].

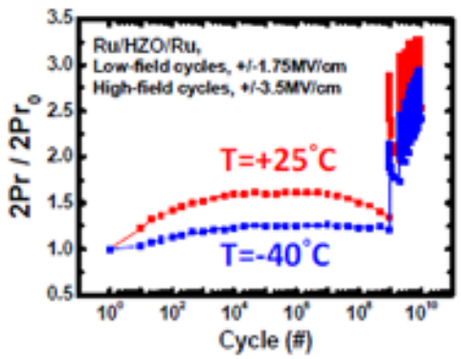


Fig. 15. Progress in fundamental understanding and approaches to high endurance ferroelectric memory cells has been reported, c.f. [58].

Emerging memory research and development demands ever increasing modeling capabilities to enable accurate, predictive, and fast TAT mapping of the design space including process variability, bit-error-rate, retention, and endurance metrics that along with power-performance-area (PPA) indicators are key to assert alternative memory cells across the memory hierarchy.

Interconnect fabrics

The resistance of vias, via-line interfaces, and lines represent a continuous challenge to the attainable chip-level performance and energy efficiency in advanced nodes. The search for materials with the goal of 2x or larger resistance reduction over elemental state-of-the-art solutions is a critical technology challenge; yet when successful significant power-performance benefits are expected at the corresponding inception node as illustrated in Fig. 16 left panel. The right panel in this figure exemplifies some promising results on very low resistivity novel interconnect material exploration[59]. Inter-chip data movement (e.g., between external memory and processing units) is also an area of significant opportunities for elevating the system-level performance and energy efficiency[59,60]. Scalable 3D-interconnect fabrics enabling increasingly higher intra and cross-die connection density as shown in Fig. 17 will be instrumental to denser VLSI systems supporting very high memory bandwidths[59,61].

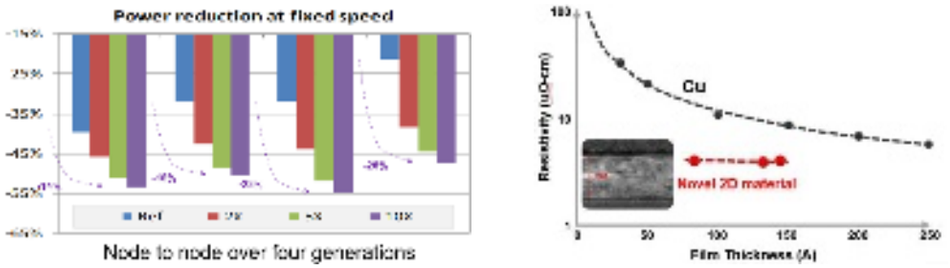


Fig. 16. Novel materials beyond elemental interconnect solutions continue to be searched with the goal of seeking 2x or larger via and line resistance reduction for significant chip-level power-performance benefits at inception node.

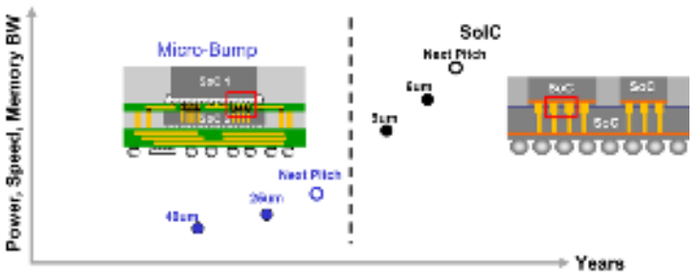


Fig. 17. 3D chip-stacking integrated into 2D/2.5D advanced packaging enables combined system-level performance, power, form factor, and functionality benefits, c.f.[59,61].

Concluding Remarks

Systems with increased levels of performance, functionality, and density will require increasingly more significant energy-efficiency innovations from software to process technology. Significant progress continues to be made in exploratory devices and interconnects. Yet challenges remain to attain proofs of concept which meet complete sets of critical metrics asserting their potential over evolutionary state-of-the art silicon-based pathways. To this end, experimental efforts compounded with a robust computational modelling framework remain imperative to efficient and effective research and pathfinding by mapping comprehensive sets of critical metrics over the relevant design space.

Acknowledgement

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Magnetoelectric Devices Towards Low-Energy Logic

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Abstract

The growth of computations performed in the world leads to an un-sustainable growth in required energy. To avoid this crisis, dramatic improvements in the energy efficiency of computing devices must be discovered, researched, and developed. One of the most promising types of energy efficient logic devices in research, is based on the use of magnetoelectric (ME) materials. The operational features of each one of these ME devices are described in this paper. Future directions of research, such as lowering the switching voltage and raising the output voltage of these energy efficient logic devices, are discussed.

1. Introduction

The tremendously successful development of information technology (IT) was enabled by the scaling of the semiconductor process according to Moore's law[5]. For the first 20 years it relied on bipolar transistors and for the following 40 years – on the MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) and CMOS (Complementary MOSFET) transistors. The insatiable customer demand for computing, mostly internet services and AI workloads, resulted in the growth of computing operations performed in the world per year by 100x per decade[16]. Even with continued computational energy efficiency improvement from Moore's scaling, the corresponding consumed energy is growing at >10x per decade. If this trend continues, the energy demand will reach a few ten's of percent of the global energy supply by 2030. Therefore, the discovery of super-energy-efficient devices and circuits (SEEDC, >100X better than CMOS))[16] will be required to avoid a stagnation of IT computing performance. This requirement flies in the face of the conventional wisdom in the computer industry – where the speed of circuits (commonly referred to as 'computing performance') for single-thread computing is valued by customers. Now, instead, the energy efficiency of the computing devices is valued. Nowadays, in most of the specifications of computer chips, one quotes 'performance per power' such as TOPS/W (tera-operations per second per Watt) which is just the inverse of the energy of switching the logic circuit for a given operation; it does not contain its speed. In addition, the potential speed of these integrated logic circuits, in turn, cannot be utilized across all computing application segments (from the datacenter to wearables) due to the limitations on the power delivery and the removal of dissipated heat.

Research on logic devices beyond CMOS has been underway for more than 15 years, and a significant share of this research was supported through the industry consortium, the Semiconductor Research Corporation. Such computing devices utilize multiple physical quantities other than electric ones (charge voltage, current) to hold the computing state[1]. Among them are electric dipole, spin and orbital momentum of electrons and, equivalently the magnetic moment associated with them, strain, orbital state of electrons, intensity of light, etc. Some of them use collective states (aka 'order parameter') of multiple particles, such as ferroelectricity, ferromagnetism, ferrodistortion, superconductivity, Bose condensate, coherent states of light, etc. Some of the materials, called multiferroics, possess more than one collective state. Simulation benchmarking of a wide variety of such devices[62,63] enabled researchers to identify the best pathway to computing energy efficiency – the lowering of the power supply operating voltage.

Spintronic devices, having magnetic moments as a computing variable, can be switched by a variety of phenomena. Among them are: the magnetic field of a current in a wire, spin-transfer torque (the effect of spin polarized current contributing magnetic moments), spin-orbit torque (the effect of coupling of the orbital motion and spin in some materials), exchange bias, i.e. a quantum interaction due to exchange transfer of spin polarized carriers across an interface, magnetoelectric coupling in some materials, etc. Spin orbit interaction can originate in a bulk of the material ('spin Hall effect') or at an interface ('Rashba-Edelstein effect'). Spintronic devices were shown to operate at lower voltages. Among them, the ones relying on the magnetoelectric (ME) switching were standing out in terms of lowest energy consumption and this was due to the fact they operate by charging of a capacitor. This contrasts with various spin transfer torque devices which require driving a current for longer time periods to ensure switching despite the thermal fluctuations on the magnetization. For a review of spintronic devices and more details on the above phenomena see[64]. Here we present a review of the history of ME devices research and attempt to map the pathways for the future. We focus on devices for logic. Various non-logic devices such as ME memory[65], ME antenna, sensors, filters, etc.[66] are outside the scope of this paper.

2. Review of magnetoelectric device research

In this section we briefly summarize the principle of operation of each device and point out their advantages and disadvantages. Advantages common to all devices are:

- non-volatility (unless there is no stable binary state, such as in spin wave devices)
- low energy ME switching.

A. Magneto-electric spin-orbit (MESO)[11,67] device.

MESO comprises the magneto-electric (ME) module which writes the computing state, i.e., converts the input voltage into the direction of magnetization, and the spin-orbit (SO) module which reads the computing state.

The ME module uses a ME multiferroic such as $BiFeO_3$. When the input voltage charges the capacitor with $BiFeO_3$, its ferroelectric polarization switches. The antiferromagnetic order as well as canted magnetization in $BiFeO_3$ are locked to the polarization and thus switch too. BiFeO3 exerts exchange bias on an adjacent ferromagnet (FM, e.g., CoFe) and reverses its magnetization.

The SO module comprises a transistor which drives current through the FM. The FM spin polarizes the current in the direction of its magnetization. Then a material with spin orbit coupling (SOC) can convert the spin direction into the charge current direction via the inverse spin-orbit effect (called inverse spin Hall effect if it occurs in the bulk, and inverse Rashba-Edelstein effect if it occurs at an interface). Thus, the direction of the output current reads the magnetization in the device.

In recent years, a complete MESO device has been demonstrated[68]. It included the demonstration of the magnetization switching by the magnetoelectric effect at ~200mV, the voltage generation due to spin-orbit effect, and the process integration to fabricate the ME and SO modules monolithically in the same chip.

Advantages:

- favorable scaling of the energy with size, specifically the width of the FM
- electrical (rather than spintronic) interconnects
- the output from the SO module is an electro-motive force (rather than magnetoresistance) which can charge a capacitor directly (i.e., the load capacitance of the interconnect and the device)

Disadvantages:

- requires a transistor to drive current through the SO module

- the output voltage of the SO module is low in demonstrations up to now
- the FM switching speed is limited by the time of the magnetization precession (~1ns)

Circuit simulations of MESO[69] discovered potential problems with sneak path currents and suggested solutions. Further circuit works [70,71] resolved such problems by using the differential inputs and outputs of the device, which enabled electrical isolation of stages, and gave deeper insights into the effects of spin transport in three dimensions and the influence of the backflow current.

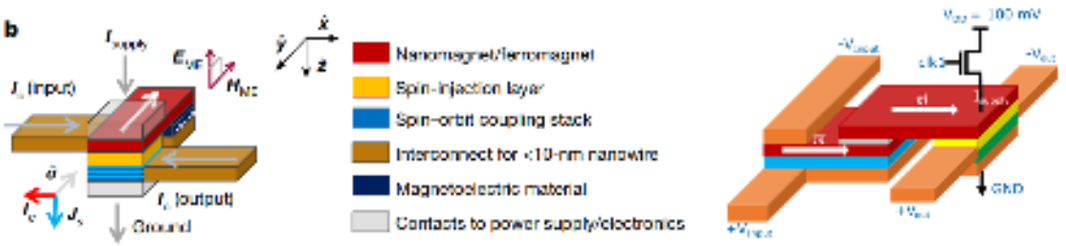

Fig. 18. Schemes of the MESO logic, (left) single-ended[67] and (right) differential[70].

B. Composite-input magnetoelectric-based logic technology (CoMET)[72].

The C0MET device consists of the write and read modules as well. In the write module, the ME effect in a ME ferroelectric converts the input voltage to the magnetization direction in the FM. The direction of magnetization is transmitted from the write to the read module as a motion of the domain wall. The domain walls are driven by the spin Hall effect (SHE) of the current flowing in the SHE layer under the FM. In the read module, the direction of magnetization is converted to voltage by the inverse ME effect in another ME ferroelectric. Then a sensing CMOS circuit converts the output voltage into another voltage suitable to drive the next stage of CoMET logic.

Advantages:

- made cascade-able by the sensing CMOS circuit

Disadvantages:

- longer logic switching delay due to a relatively low domain wall speed compared to electric interconnects. (Even though the speed of domain walls as high as ~4km/s was demonstrated[73], the speed of electric interconnects is ~500km/s.)
- propagation of domain wall is less energy efficient than electric interconnects.
- Output voltage in inverse ME effect may be low.

Circuits such as a non-volatile flip-flop has been envisioned with COMET[74]. These devices can implement a complete set of logic gates (MAJ, (N)AND, (N)OR, etc.) as is the case for the rest of spintronic logic reviewed here.

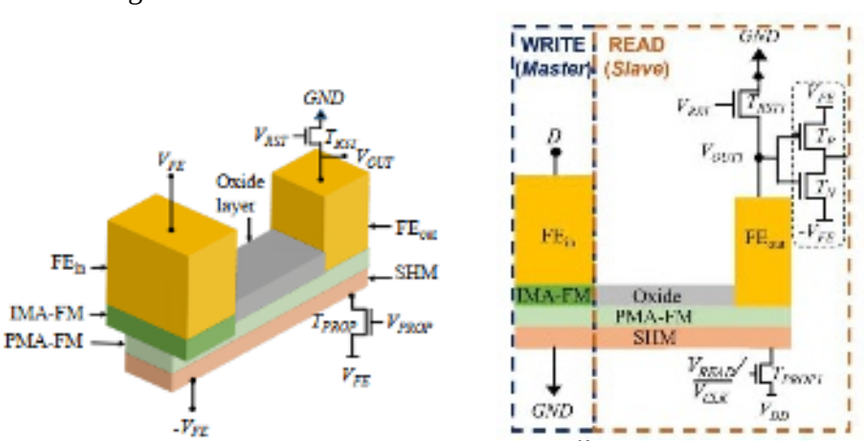

Fig. 19. Scheme of the COMET logic device[72] and a non-volatile flip-flop[74] .

C. Anti-ferromagnetic spin-orbit read (AFSOR)[75] device.

The AFSOR device is similar to a usual MOSFET. It uses the gate voltage to switch the electric polarization in a multiferroic ME material (such as BiFeO3). This is accompanied by switching of the net magnetization in the ME material. Unlike usual MOSFETs, the channel in AFSOR comprises a material with spin-orbit coupling (e. g. a topological insulator being an extreme case). Then carriers with spins with one orientation (labeled 'up') predominantly flow in one direction along the channel, while the spin with the opposite orientation (labeled 'down') predominantly flow in the opposite direction. When the magnetization in the ME material favors one direction of spin of carriers by lowering their energy, this results in a unidirectional conduction, i.e., lower conductance in one direction that the other. If the FE polarization of the multiferroic ME material switches, the direction of conduction is reversed.

Advantages:

- uses the efficient field effect for controlling current.
- Electrical isolation of the write and read paths.

Disadvantages:

- need to demonstrate higher net magnetization in a ME material.
- the degree of unidirectional conduction is low in SO demonstrations up to now.

Reliance on the unidirectional conductance requires circuits which are different from traditional CMOS ones. An example of such circuits and their benchmark is presented in Ref. [76].

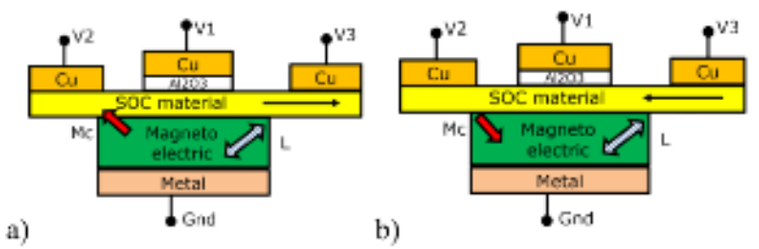

Fig. 20. Scheme of the AFSOR logic device[75] .

D. Spin-orbit torque field-effect transistor (SOTFET)[77]

The SOTFET uses the SO torque to switch the direction of magnetization of a FM in the write module. The change of magnetization switches the magnetic order in the ME multiferroic, then the ferroelectric polarization should follow. In the read module, the direction of polarization opens or closes conduction in a semiconductor channel like in a typical FET. In usual ME materials, like BiFeO3, the energy of the ferroelectric order is much higher than that of the magnetic order. Thus, the magnetic order is driven by the polarization. The opposite situation is required for a SOTFET. This necessitates the search for ME materials with a stronger magnetization and weaker polarization[78]. No material or material combination of materials has been found that fully satisfies this requirement with the remaining condition that the phase transition temperature is significantly higher than the room temperature.

Advantages:

- uses the efficient field effect for controlling current.
- Electrical isolation of the write and read paths.

Disadvantages:

- requirement of stronger FM and weaker FE in the multiferroic dictates the choice of a material which has not been identified yet.
- the speed is limited by the time of the magnetization precession (~1ns).

Circuit simulations[79] demonstrates that typical logic gates, Random Access Memory (RAM), and ternary content-addressable memory (TCAM) can be implemented with the SOTFET.

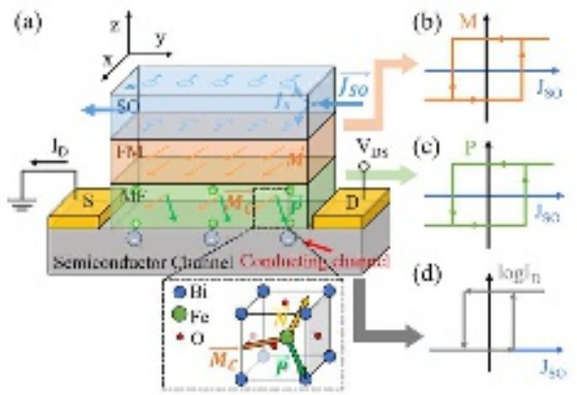

Fig. 21. Scheme of the SOTFET logic device[77] .

E. ME-driven spin wave devices[80].

For spin wave devices, the electrical-to-spin transduction is expected to be more energy-efficient if the ME effect is used. In the implementation below, a heterostructure of a piezoelectric and a magnetostrictive material is used. In the write module, an AC voltage is used to excite a spin wave in a FM waveguide. The spin wave propagates to the read module, where the alternating magnetization is converted into an AC voltage in a similar ME heterostructure as in the write module. A spin-wave majority gate has been experimentally demonstrated[81].

Advantages:

- ME effect in a heterostructure is expected to be more efficient than in a single material.
- possibility to use both amplitude and phase for logic functions.

Disadvantages:

- the output is a propagating spin wave signal rather than an element which can hold the logic state. There have been theoretical proposals of such[82], but they have not been experimentally implemented.
- difficulty of using AC voltage inputs and outputs to realize logic.

Circuit simulations[83] show that spin wave circuits can efficiently implement complex logic functions (due to the use of majority gates) and compare favorably with CMOS.

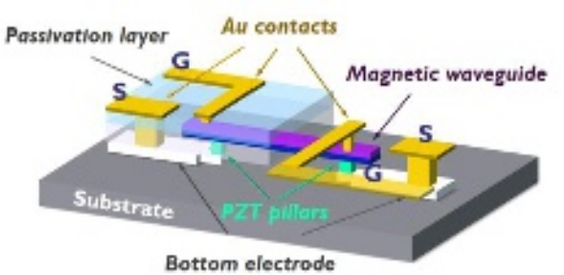

Fig. 22. Scheme of a ME-driven spin wave device[80] .

3. Benchmarking

Simulation benchmarking of exploratory energy efficient logic devices is often useful to map the future direction of their development. Here we present the benchmarking results for CMOS, tunneling FET (TFET), ferroelectric FET (FEFET), and MESO with their dependence on the supply voltage. The method follows closely Ref.[63]. Updated benchmarking studies covering many spintronic devices and circuits can be found in[84].

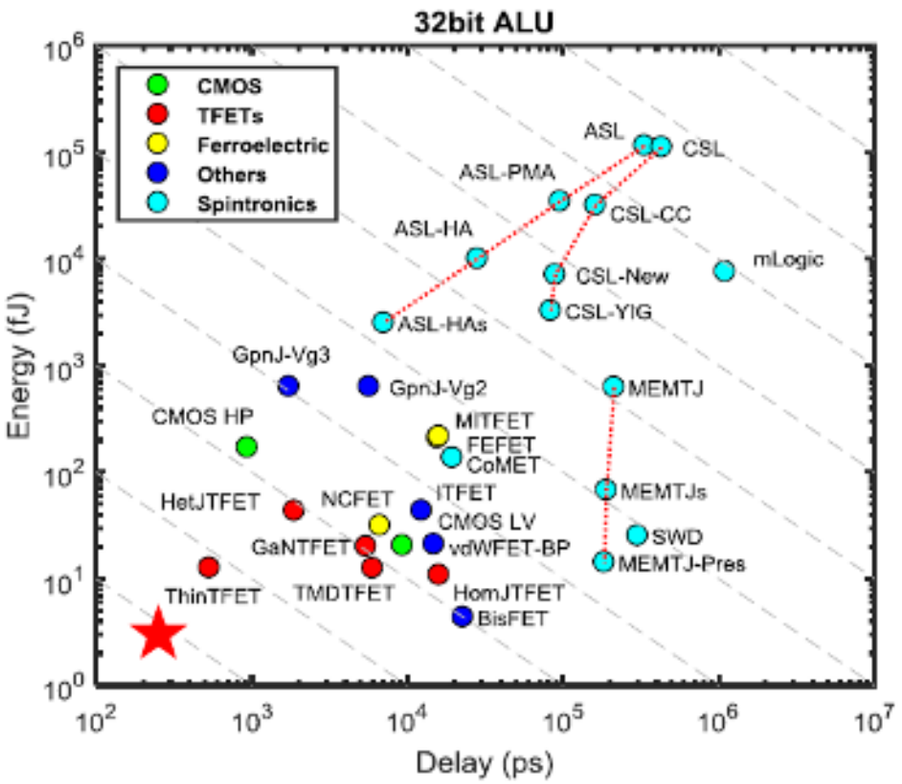

Fig. 23. Reproduced from [84]. Energy versus delay of a 32-bit ALU for a variety of charge- and spin-based devices. Please see the original paper for the labels of devices. The red star indicates the preferred corner.

We observe that, as expected, the energy of operation decreases, and the delay increases as the supply voltage is decreased (~ constant Energy x Delay product). The increase of delay becomes very dramatic for CMOS at Vdd < 0.4V. This is caused by the necessity that the MOSFET has an appreciable (~0.3V) threshold voltage to efficiently turn off its current at a gate-to-source voltage = 0V. The on-current strongly decreases as the supply voltage approaches the threshold voltage. The advantage of a TFET over the MOSFET is that the subthreshold slope is steeper and thus the threshold voltage can be decreased[85]. Besides, the charge in the channel of TFET can be lower. Thus, TFET can be faster at the same energy. However, the difference in delay and energy between CMOS and TFET is less dramatic than with other beyond CMOS devices. FEFET can have a steeper subthreshold slope due the negative capacitance effect[86]. The switching delay of an FEFET is limited by the intrinsic switching time of a ferroelectric material. The operating supply voltage can be further decreased in ME spin orbit logic provided the coercive voltage of ME materials can be sufficiently decreased, since it is not limited by

the threshold voltage. The delay of MESO is limited by the intrinsic switching time of a nanomagnet (~1ns).

In summary, decreasing the supply voltage is the main pathway to decreasing energy in logic devices. Beyond CMOS devices have a different slope of energy versus delay dependence and can be more efficient than CMOS at lower voltages.

One should not interpret the trade-off of slower speed for lower energy as unfavorable. Such a trade-off has been made in 1990s via a transition of mainstream electronics (personal computers and mainframes) from bipolar transistors to CMOS transistors. Then and once again nowadays, the energy efficiency is valued more than speed. One of the reasons for that is that the dissipated heat power per unit area is limited by our ability to remove this heat. With this limitation in mind, one cannot use the full speed of high-performance CMOS transistors, and one must decrease the activity factor of circuits. This way, more energy efficient circuits can allow a higher computing throughput that CMOS. From that point of view, increasing the device speed would be counterproductive.

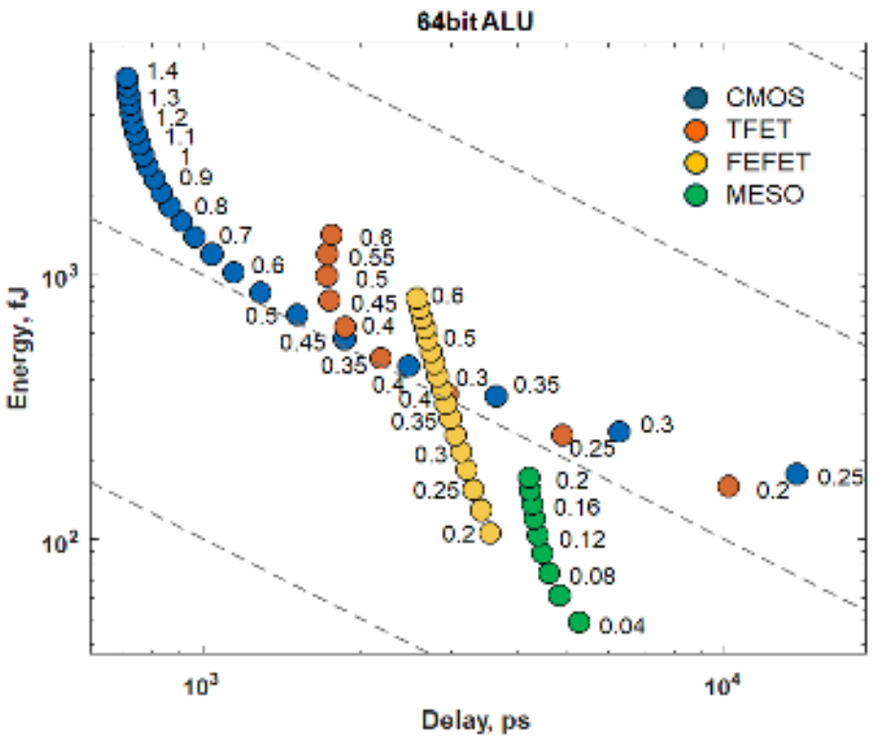

Fig. 24. Benchmarking of energy vs. delay of a single operation of an ALU based on CMOS (blue), TFET (red), FEFET (orange), and MESO (green) devices for a range of voltages (labeled next to corresponding dots).

4. Requirements for future development

Let us give our view on the trends in exploratory research for low voltage devices.

1) Logic devices need to fulfil certain tenets [62] to be used as building blocks of digital logic for computing. One of the tenets is the devices need to be cascade-able, e.g., the output voltage can drive the input of the next logic stage. Otherwise, additional circuits, with their corresponding delay and energy expense, are required to amplify device's output logic signal.

2) The need to decrease the ME switching voltage. Some experimental progress has been made in reaching ultra-low switching voltage[87]. In general, the use of quantum materials, exhibiting novel

phenomena, such as having unusual order parameters that are collectively switched, can have energy barriers which are easier to switch[1].

3) The need to increase the output voltage via stronger spin-to-charge conversion. Note that the figure of-merit for spin-to-charge conversion is different than that for spin-orbit torque. Pathways for the improvement of the SO output voltage[88], in which both higher spin Hall coefficient and higher resistance of the SO material are required. Materials such as SrIrO3[89] are of interest.

4) Avoiding the delay limitation of the FM switching. This requires creative thinking to discover "magnet-less" device schemes. In this regard, an experimental demonstration[90] proved that it is possible to reverse the sign of the spin-orbit effect by an adjacent ferroelectric. One needs to come up with ways to read-off of the polarization state or the antiferromagnetic state of a ME material. One of the possibilities is to read the antiferromagnetic order by the anomalous Hall effect[91] directly, without an intermediate FM.

5. Conclusions

In summary, we presented some leading examples of ME logic devices, which were proposed mostly in the last 5 years, and summarized the status of research on them. They have attractive features as well as challenges to overcome. To make them viable building blocks for logic circuits, their material parameters need to be dramatically improved. This requires creative ideas and research into unconventional materials and devices.

Neuromorphic Engineering — Bio-inspired and Bio-mimicking Computing Platforms

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The biological neuronal network—the brain—boasts unique computing abilities, such as easy learning from few and noisy data, adaptation to the environment, autonomy, and cognition, and all of these at low power consumption. Neuromorphic engineering originally attempted to closely mimic the details of the biological neuronal network on a silicon integrated circuit[92] in hopes of reproducing the unique computing capabilities of the brain, but such close brain mimicry proved difficult due to the lack of knowledge on how a large number of neurons in the brain wire to create its functions. The goal of neuromorphic engineering thus was relaxed from the detailed mimicry of the biological neuronal network to a design that is inspired by certain overall characteristics of the biological neuronal network. A notable example of such brain-inspired design is the non-volatile memory (NVM) crossbar array[93–100]that performs analog vector-matrix multiplications—or analog multiply-accumulate (MAC) operations—in low power. The NVM crossbar array, which co-locates memory and computing, is inspired by the brain where biological memories (synapses) are spread across the neuronal network. At the same time, this bio-inspired NVM crossbar array does not mimic the details of the biological neuronal network and the in-memory arithmetic computing it performs is a far cry from reproducing the unique computing abilities of the brain.

The bio-inspired in-memory computing with the NVM crossbar array may one day prove useful for artificial neural net (ANN) computing for artificial intelligence (AI). The commercial success of AI is enabled by digital processors, such as graphics, neural, and tensor processing units (GPU, NPU, and TPU), tailored for the ANN computing. They handle well the intensive vector-matrix multiplications, the most frequent computation in ANNs. However, shuttling ANN weights from off-chip memory to these digital processors consumes a significant power. In contrast, in-memory computing based on NVM crossbar arrays [93–100]that co-locate memory for weight data storage and computing (analog vector-matrix multiplication) can achieve a lower power consumption. In the standard NVM crossbar array architecture shown in Fig. 25, each memory cell in the array, which stores an ANN weight as its conductance value, multiplies an input voltage by the weight based on Ohm's law to produce a current. Each column of the array, which connects the memory cells in parallel, then adds the memory cell currents based on Kirchhoff's law. Thus, each column current is the dot product of the input vector consisting of the voltages fed to the rows and the vector consisting of the column's weight values. Then the vector comprising all column currents is the multiplication of the input voltage vector and the weight matrix of the array. In this way, the crossbar array co-locates memory and analog computing, removing the power dissipation associated with shuttling ANN weights.

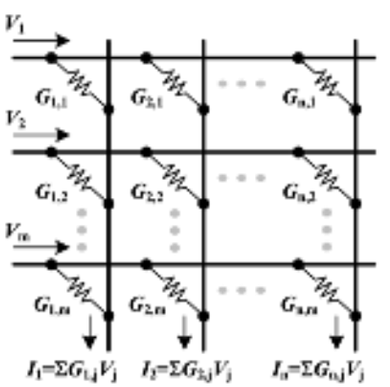

Fig. 25. Conventional memory crossbar array. Each column connects memory cells in parallel. Reused with permission from Ref.[101] , Springer Nature Ltd.

1. The frontier of in-memory computing – an example with magnetic synapses

The study of the NVM crossbar array has been especially active with resistive and phase-change random access memory (RRAM and PRAM)[93–100]. In contrast, crossbar arrays with magnetoresistive random access memory (MRAM) for in-memory computing have only recently been demonstrated[101], which we will describe here to illustrate an example effort in the frontier of in-memory computing. The MRAM is based on a magnetic tunnel junction (MTJ) comprising two magnetic layers sandwiching a thin insulator. The two magnetic layers can have parallel or anti-parallel magnetizations,

which respectively lead to low (R_L) or high (R_H) resistance. The prior challenge for building an MRAM crossbar array stemmed from noticeably small R_L and R_H values, with which the conventional crossbar array (Fig. 25) with the column connecting memory cells in parallel (with the column output being the sum of the memory cell currents) would dissipate a considerable power. The recent development of the MRAM crossbar array[101] came over the issue with a new crossbar array architecture, where each column connects memory cells in series with the column output being the sum of the memory cell resistances.

This architecture uses a memory cell of Fig. 26a, featuring two parallel paths, with each path formed by a field-effect transistor (FET) switch and an MTJ in series. The FETs of the left and right paths are gated by a binary input voltage *IN* (V_L or V_H) and its complementary voltage, respectively. The MTJs on the left and right path store a binary weight *W* (R_L or R_H) and its complementary weight, respectively. As *IN* selects one path of the two, the cell's output becomes the MTJ resistance of the selected path. The cell outputs for all 4 possible *IN* and *W* combinations (Fig. 26b) show that the cell output is the binary multiplication of *IN* and *W*, if we assign 1 to R_H and V_H, and -1 to R_L and V_L. This switching-based analog binary multiplication to output the memory cell resistance replaces the Ohm's law based multiplication that outputs the memory cell current in the standard crossbar array.

In the new architecture, each column stacks these memory cells in series (Fig. 26c). The memory cell's output resistances are then summed to yield the column resistance *R*, which is the column output. This column resistance sum replaces the Kirchhoff's law based column current sum in the standard crossbar array. The column *R* is the dot product of the input vector consisting of *IN* values fed to the rows and the weight vector consisting of the column cells' *W* values. Then the vector consisting of all column resistances is the multiplication of the input voltage vector and the weight matrix of the array. This architecture lowers power consumption for small R_L and R_H, enabling the MRAM crossbar array. The MRAM crossbar array[101], with an energy efficiency of 262 ~ 405 TOPS/W, performed all vector-matrix applications for a 2-layer ANN to classify 10,000 MNIST digits with a 93.23% accuracy, and a part of vector-matrix applications of a 10-layer ANN to detect faces with a 93.4% accuracy.

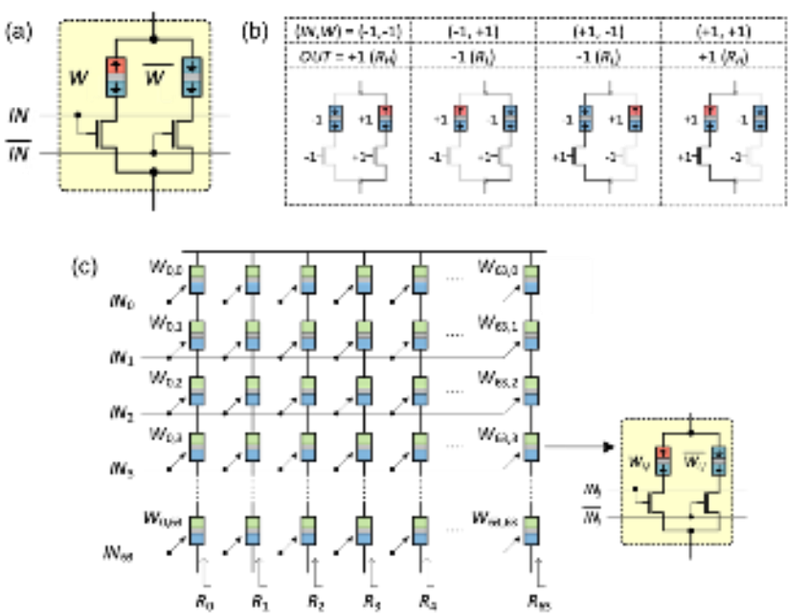

Fig. 26. (a) MRAM memory cell with a binary input voltage *IN* and a binary weight *W*. (b) Memory cell resistance for all 4 combinations of *IN* and *W* values. (c) MRAM crossbar array. Each column stacks memory cells in series. Adapted with permission from Ref.[101] , Springer Nature Ltd.

This development complements other NVM types for in-memory computing, as different NVMs bring differing merits (for MRAM: energy, speed, stability, endurance) and drawbacks (for MRAM: 1b per cell). As MRAM is a commercially mature NVM embedded in CMOS technology, this development can also be a seed for future fully integrated in-memory computing processors, where many crossbar

arrays would be integrated with CMOS electronics to map out the entire ANN for not only vector-matrix multiplications but also digital processing (such as pooling and activation). In fact, the commercial viability of in-memory computing based on memory crossbar arrays needs to be studied with such a fully integrated processor chip, carefully examining how the power consumption reduction in crossbar arrays would translate to the power consumption reduction in the overall chip, and whether the reduced power consumption is worthy of having to live with drawbacks of in-memory computing such as analog computing error and increased chip area due to the storage of weight data on the processing chip itself.

2. Bio-mimicking computing platform from neurobiology

The NVM crossbar array is inspired by the memory-compute co-location feature of the brain, but it does not mimic the details of the biological neuronal network to reproduce the unique computing abilities of the brain. While close [92]brain mimicry has been difficult due to the lack of knowledge on neuronal connections in the brain, recent advances in neurobiology tools bring us closer to mapping the biological neuronal connectivity map, and this in turn may help the close brain mimicry, the original goal of neuromorphic engineering.[92]

A notable example of such new tools is the CMOS nanoelectrode array[102,103], a neuro-electronic interface capable of massively parallel intracellular recording of mammalian neuronal networks (Fig. 27). Parallelization of intracellular recording has been a significant pursuit, for it would allow for the functional synaptic connectivity mapping in a biological neuronal network, but proved difficult. For example, the patch clamp electrode transformed neurobiology with its highly sensitive intracellular recording: it can measure not only action potentials but also synaptic signals and thus can find and study a synapse. But as the patch clamp cannot be scaled into a dense array, only up to ~10 parallel patch recordings were possible, with which mapping a network-wide synaptic connectivity is difficult. For another example, the microelectrode array[104,105] can record many neurons so it can monitor a network, but it is a low-sensitivity extracellular method and cannot record synaptic signals. The CMOS nanoelectrode array (Fig. 27) finally parallelized intracellular recording[102,103], with both surface nanoelectrodes and the underlying CMOS circuits being critical for this feat. In Ref.[102] , the CMOS nanoelectrode array with 4,096 recording sites measured intracellular signals from 1,728 sites, a great advance from ~10 patch intracellular recordings. As the network-wide intracellular recording data includes synaptic signals from many neurons, one can find synaptic connections from the data. In Ref.[102] , 304 excitatory and inhibitory synaptic connections were mapped from the 1,728 intracellular signals obtained from 19 min recording, a throughput unprecedented in functional synaptic connectivity mapping.

Fig. 27. CMOS nanoelectrode array for network intracellular recording. Adapted with permission from Refs. [88, 96], Springer Nature Ltd.

Such functional synaptic connectivity map extracted from the network-wide intracellular recording data may then be imitated by a solid-state memory network, a computing platform that would more closely mimic the biological neuronal network. So far, the parallel intracellular recording has been done on rat cortical neurons *in vitro* cultured on the surface of the CMOS nanoelectrode array. Challenges, and also opportunities, thus lie in developing a CMOS nanoelectrode array can onward be developed for *in vivo* network-wide intracellular recording (currently available *in vivo* recording tools are all extracellular techniques[105]). Ref.[95] details this approach to leverage state-of-the-art neurobiology tools for retargeting the original neuromorphic goal.

Computing-in-Memory Design and Benchmark

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Introduction: As we march deeper into the age of Artificial Intelligence (AI) and big data, the edge-computing hardware supporting large matrix multiplication workloads is becoming ubiquitous. The computing needs to provide high precision while squeezing dense on-chip model storage with energy efficiency. Conventional general-purpose architecture utilizes memory and computing circuits separated with intermediate cache hierarchy to handle spatio-temporally localized access patterns within a small working set[106]. However, the need to support such random accesses is not mandatory for AI workloads that have deterministic but massive working sets. This results in perpetual shuffling of data between the memory and computing with large energy and latency costs on conventional hardware. This has resulted in efforts on bringing computing close to the memory using newer computing architectures called computing-in-memory (CIM). The CIM includes strategies to bring computing elements close to the memory (near-memory computing or NMC) or merging computing with the memory (in-memory computing or IMC)[107]. These methods suppress unnecessary data movement which improves latency, power consumption and efficiency.

CIM Background: Fig. 28 compares the conventional computing with CIM alternatives. NMC operates on similar principal as that of conventional processing with memory readout and processing occurring sequentially. However, the computing circuits are close to the memory array which reduces the data transfer costs and the predictable access and computing patterns allow completion of an operation within a single clock cycle. On the other hand, IMC uses memory to store the model weights and the input are applied to the memory array to fuse the computing with memory with mixed-signal readout with minimal data movement overheads. CIM requires a dense storage memory to keep the weights of the model on-chip to avoid energy cost of reading external memory while the inputs are typically provided externally. SRAM has been utilized previously for both NMC and IMC because of mature process integration and continuous scaling capacity with process nodes[108–114]. However, the volatility of SRAM causes efficiency degradation with continuous leakage when the edge processor is deployed in mostly-off scenario and latency degradation during initialization for every wake-up call. DRAM suffers from similar volatility constraint with additional challenges in process integration with CMOS at scaled nodes. The leakage and refresh cost of the previous volatile memory choices can be mitigated by various non-volatile memory devices (NVM) like process integrated RRAM[96,115–124], PCM[98,125–130] and STTMRAM[101,131–136]. These devices offer greater density compared to SRAM at similar process nodes.

Fig. 29 shows the example of CIM operations with 1T1R RRAM memory array storing the model weights. NMC uses adjacent computing units for carrying of the operations like addition/multiplication etc. The memory operation involves activating a word-line (WL) to read the bit-lines (BL) current accumulated on the source-lines (SL) using sensing circuitry and utilize the output data in the computing circuits to produce results in a single clock cycle. On the other hand, IMC uses the memory array to carry out the multiply and accumulate (MAC) operation within it. This is carried out by applying the inputs at the WL which causes the current in the devices depending upon their resistance value. This accumulates over the BL and is read using a readout circuit to produce a localized multi-

input multi-weight operation in a single clock cycle with high throughput and high efficiency. The article will focus on nonvolatile in-memory computing (nvIMC) operations because of the extreme energy efficiency achieved by Silicon-verified macros over the past decade.

IMC Design: High accuracy requirement of computing puts stringent constraints on computation precision and encoding of inputs and weights, readout circuitry for outputs and handling device non-idealities. This multi-dimensional design space offers ample choices to tune the design.

Input: Most neural-nets (NN) use rectified linear unit (ReLu) activation requiring efficient input encoding for positive activations and Fig. 30 shows the different approaches. Serial binary (SB) approach applies the bits of the input sequentially at the WL and the outputs from the sensing circuit are read over every BL. The outputs are externally added with place-value-aware accumulation with the computing time being proportional to the bit-width (n)[137]. Pulse width modulation (PWM) approach alters the duration of the input pulse depending upon the binary value stored within the number and the accumulated charge in the BL provides the output of MAC operation[123]. The worst-case latency scales exponentially (2^n) with increasing bit-widths. The third scheme uses analog input voltage (AIV) by converting the digital input values to analog values using digital-to-analog converters (DAC) and produce outputs within a single clock cycle[124] irrespective of the bit-width. However, the encoded voltage needs to be lower than the programming voltage to avoid read-disturb and additional DAC hardware is required to speed up the computation. Both PWM and AIV approaches are susceptible to error injection due to process-voltage-temperature (PVT) variations causing inaccurate voltage or duration encodings.

Weight: NN weights typically contain both positive and negative values and the approaches dealing with incorporating the sign of the operation are shown in Fig. 31. The first approach uses separate banks for storing the positive and negative weights[138]. The sensed outputs are subtracted externally. However, the simplicity of computation results in 2x storage requirement and compute energy. The 2's complement weight approach uses the MSB to store the sign of the weight. The computation over each column is combined with the place-value using a separate MSB detection circuit. This saves storage hardware at the cost of slightly higher computational overhead[123]. Both input and weight encoding schemes require MAC computation outside the IMC macro which have been demonstrated using charge sharing[139], capacitive coupling[140] or digital additions[117].

Implication of memory devices: NVM devices typically have variation in the resistance in both high and low resistance states (HRS, LRS) caused by process variations. Additionally, the ratio of the resistance in HRS and LRS (R-ratio) varies for different NVM choices. These variations result in the bitline current (I_{BL}) having a wide distribution and limited separation (sensing margin) between adjacent output values as shown in Fig. 32. For example, the case of sensing '3' over a 9-WL read configuration can be because of 3 driven-WL accessing 3 LRS-cells (3L0H). Similarly, this case may also be for 3 driven-WL accessing 3 LRS-cells and 6 driven-WL accessing 6-HRS cells (3L6H). Such pattern-dependency widens the distribution for each output value and compresses the sensing margin. Smaller R-ratio makes it further challenging to distinguish I_{BL} for, say, 3L6H and 4L0H. Fig. 33 shows how increasing output bit precision (9 WL in this case) reduces the sensing margin because of multiple crowded distributions for every output[107]. The sensing margin improves if the device offers larger R-ratio and the pattern dependent contribution of HRS current reduces. R-ratio improvement is possible by over-setting and over-resetting a device to widen the resistance window and circuit techniques have been proposed to cancel I_{HRS}[141].

Output readout methods: The current over the BL needs accurate readout circuit which is demonstrated using both voltage-mode analog-to-digital converters (ADC) and current-mode sense amplifiers (CSA)[107]. Both schemes require the sensing voltage to remain under the programming voltage to avoid read disturbance. CSA uses current mirrors to combine place-value-aware currents from adjacent BLs

followed by readout to digital domain as shown in Fig. 34. Voltage-mode approaches use current to voltage converter (IV converter) to convert I_{BL} to voltage, followed by combining the voltages into partial analog voltages (partial MACs) which are sensed by the ADC. Current-mode readout provides V_{DD} independent readout but causes DC power with DC currents. On the other hand, voltage-mode readout suppresses power consumption at the cost of reduced signal margin (increased errors) with changing V_{DD}. Voltage-mode scheme from[123] show 1.88x power reduction compared to current-mode scheme from[142] by eliminating the DC currents (Fig. 35). Additionally, the area consumption of the two modes is compared in Fig. 36 where generating multiple references and noise-tolerant large transistor results in larger area utilization for current-mode sensing. The trade-off is effectively utilized in previous approaches[123,128,141].

Benchmark*:* Fig. 37(a) illustrates the benchmark of recent Silicon-verified CIM publications. Digital SRAM-IMC has achieved the highest overall performance in terms of compute density (TOPS/mm^2) and energy efficiency (TOPS/W). However, nvCIM and analog SRAM-IMC also show their strengths in energy efficiency and compute throughput density, respectively. SRAM-IMC designs achieve excellence compute density with smaller memory capacities of tens of kilobits (kb) that provide smaller parasitics and higher area fraction utilized by the memory array. In contrast, high cell density of nvCIM devices results in memory capacity of several megabits (Mb) or more. This, along with a large area overhead of readout ADCs hamper the performance metrics involving area density. Fig. 37(b) provides another perspective by incorporating memory capacity into compute throughput density on the x-axis. This reveals that the compute density separation among different CIM architectures diminishes if memory capacity is considered. Additionally, the key differentiator of nvCIM, its nonvolatility, is application dependent and challenging to incorporate in these analyses. Therefore, it is crucial to consider these application dependent factors, such as memory capacity and nonvolatility, in addition to energy efficiency and compute throughput density when evaluating CIM architectures.

Conclusions: Computing-in-memory is an architectural strategy that aims to bring computing elements closer to the memory, either through near-memory computing (NMC) or merging computing with the memory (in-memory computing or IMC). This article offers an overview of the design approaches used in CIM, as well as the implications for memory device technology. Additionally, it provides a benchmark of recent Silicon-verified CIM publications.

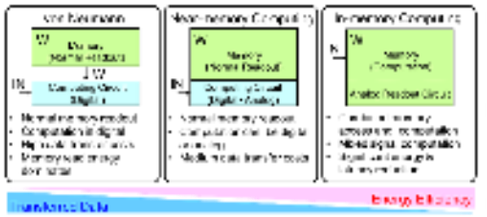

Fig. 28 Conceptual illustrations of (a) von Neumann, (b) near-memory computing (NMC) , and (c) in-memory computing (IMC) architectures.

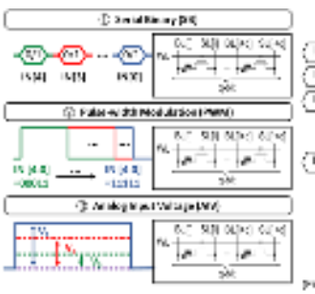

Fig. 30 Three multi-bit input schemes: (a) serial binary input pulse, (b) pulse-width modulation, and (c) analog input BL voltage.

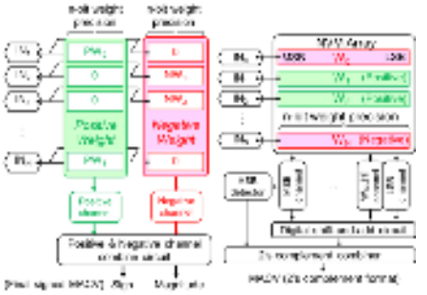

Fig. 31 Two types of weight data commonly used in nvCIM: (a) separate positive and negative weight data and (b) two's complement weight data.

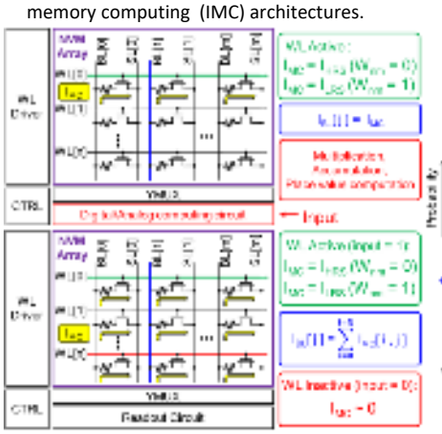

Fig. 29 Basic concept and structure of (a) NMC and (b) IMC using nonvolatile computing-in-memory (nvCIM).

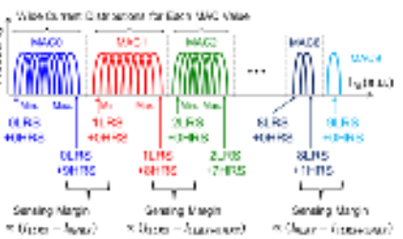

Fig. 32 Pattern-dependent variation in bitline current (I_{BL}) widens the distribution of MAC values (MACV) and decreases sensing margin.

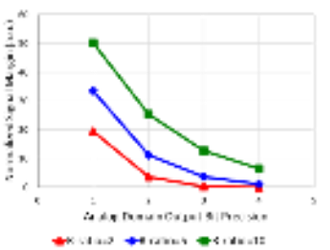

Fig. 33 Simulated signal margin versus output precision in the analog domain under different R-ratio values.

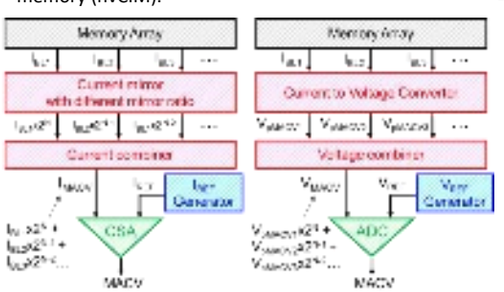

Fig. 34 Comparison between two readout schemes: (a) current mode readout and voltage mode readout.

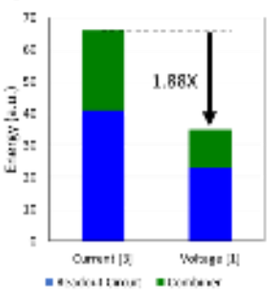

Fig. 35 Energy comparison between current-mode and voltage-mode readout.

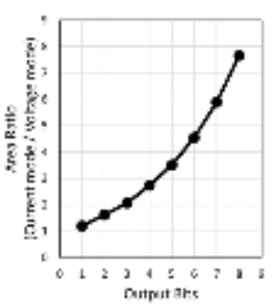

Fig. 36 Comparison of area between voltage and current mode using sequential readout.

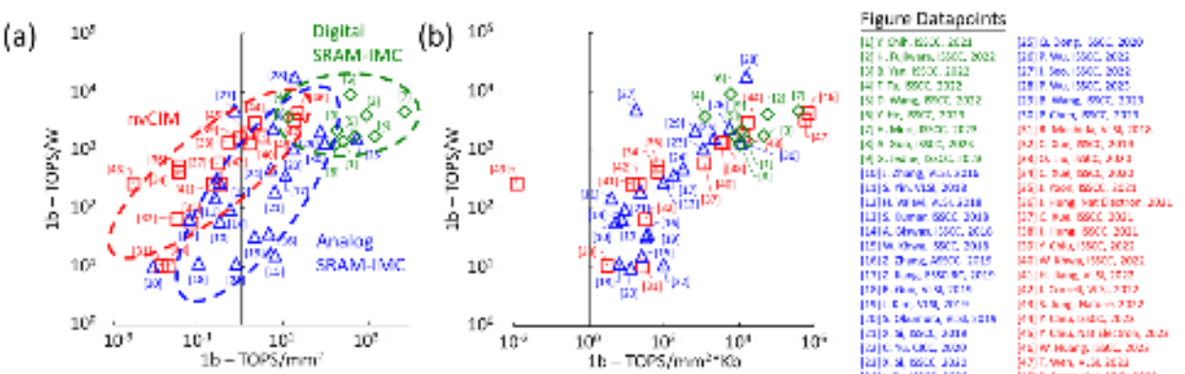

Fig. 37 Benchmark of recent Silicon-verified CIM publications – (a) compute throughput density (TOPS/mm^2) versus energy efficiency (TOPS/W) and (b) incorporating memory capacity into compute throughput density (TOPS/mm^2*Kb).

(For the reference above, the [1]→ [113], [2]→ [109], [3]→ [110], [4]→[111], [5]→[112], [6]→[143], [7]→[108], [8]→[144], [9]→[145], [10]→[146], [11]→ [147], [12]→ [148], [13]→[149], [14]→[150], [15]→ [114], [16]→[151], [17]→ [140], [18]→[152], [19]→[153], [20]→[154], [21]→[155], [22]→[156], [23]→[157], [24]→[158], [25]→[159], [26]→[160], [27]→[161], [28]→[162], [29]→[163], [30]→[164], [31]→[165], [32]→[138], [33]→[166], [34]→[142], [35]→[167], [36]→[119], [37]→[123], [38]→[122], [39]→[133], [40]→[127], [41]→[168], [42]→[169], [43]→[101], [44]→[131], [45]→[136], [46]→[118], [47]→[115], [48]→[116])

II. Technology Approaches

Pathways to voltage-controlled antiferromagnetic spintronics

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A. Status

Moore's law is an empirical finding which quantifies the phenomenon of accelerated return commonly observed in evolving information technologies (IT). Arguably the most severe challenge to maintain an exponential increase in the performance-to-price ratio of information processing devices is the breakdown of Dennard's law. It describes the invariance of the electric power density on scaling of charge-based integrated electronic circuits which are based on field effect transistors (FET)[6]. Much of the advances in modern IT, which led to new paradigms such as brain inspired computing and the internet of things, became possible because of scaling. Today, scaling of complementary metal-oxide semiconductor (CMOS) technology takes place at the 5nm CMOS technology node enabled by extreme UV lithography. Continuation of scaling is, however, confronted with the breakdown of Dennard's law accompanied by detrimental energy dissipation and Joule heating.

Spintronics has emerged as a promising alternative to charge-based IT. Spintronics can mitigate issues such as memory volatility associated with leakage of charge which intensifies with ever decreasing device dimensions. However, not all spintronics approaches are equally favorable. Traditionally, manipulation of collective spin states hinges on controlled magnetization reversal in ferromagnetic thin films. Here magnetization serves as state variable which can be switched by electric currents exerting torques on the magnetization to change the angular momentum through spin transfer torques and spin-orbit torques generated by a plethora of mechanisms including angular momentum conservation, spin Hall and the Rashba-Edelstein effect to name a few[170]. Such spintronic devices have some advantages in niche applications where properties such as non-volatility and radiation robustness matter. They are, however, challenged when benchmarked against the energy-delay product of CMOS technology. This is largely because magnetization reversal in ferromagnets is notoriously slow (ns) and energy inefficient. To improve spintronic devices it is necessary to reduce their switching energy and delay time. Both problems can be addressed with the help of antiferromagnetic (AFM) spintronics. AFM spintronics allows switching of the state variable on the ps time scale, orders of magnitude faster than magnetization reversal in ferromagnets. The speedup originates from the presence of a strong exchange field acting on the sublattice magnetization. Exchange fields can be orders of magnitude larger than practical applied magnetic fields. The increase in field strength gives rise to increased precession frequencies compared to the Larmor precession frequency of a ferromagnetic moment in an applied field.

In addition, voltage-controlled manipulation of the AFM order parameter in the absence of electric currents can be virtually dissipation-less. As a result, voltage-controlled AFM spintronics can be vastly superior over current induced switching making scalable, ultra-low power, non-volatile memory, and logic with attojoule switching energies feasible[171]. In lowest order, *i.e.* at temperatures significantly below the Néel temperature and at magnetic fields significantly below the onset of field-induced phase transitions such as spin-flip or spin-flop transitions, antiferromagnets do not couple to homogenous applied magnetic fields. The weak coupling originates from the absence of an overall magnetic moment in an antiferromagnet with virtually perfect compensation of the magnetization of its sublattices. As a

result, the Zeeman energy of an antiferromagnet in a homogeneous magnetic field is virtually zero reflecting the fact that a staggered rather than a homogeneous magnetic field is conjugate to the AFM order parameter. This property makes AFM spintronics insensitive to external magnetic field perturbations and minimizes crosstalk between neighboring devices. However, this beneficial property comes at the price of making it more challenging to manipulate the antiferromagnetic spin state, compared with ferromagnets. Next some advances in manipulating the antiferromagnetic state are discussed with special emphasis on pure voltage-control. Some common readout mechanisms are briefly introduced as well.

B. Advances and Challenges

Although AFM spintronics is only a subset of spintronics it is in and of itself a broad and fast growing field with multiple evolving branches. Fig. 38 depicts a Venn diagram which uses switching mechanisms and basic materials properties as an organizing principle. With focus on potential applications for scalable, integrable, and CMOS compatible solid state devices, Fig. 38 leaves out the otherwise exciting field of ultra-fast laser induced switching of antiferromagnets such as $TmFeO_3$, a G-type antiferromagnet from the group of rare-earth orthoferrites known to have strong temperature dependent anisotropy[172,173].

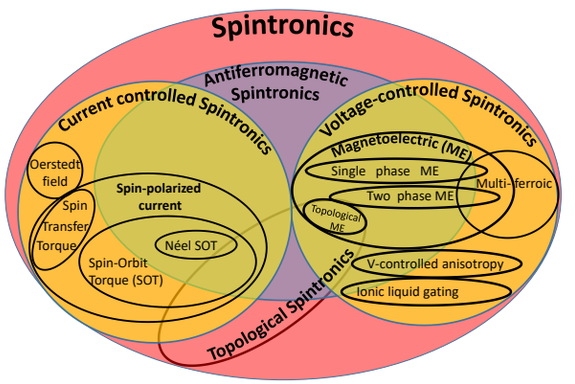

Fig. 38: Venn diagram using common voltage and current induced switching mechanisms to organize various sub-fields of spintronics including voltage-controlled AFM spintronics.

A communality of AFM spintronics rests in some form of control over the AFM order parameter either via reorientation of the Néel vector or switching between AFM order and disorder. Fig. 38 displays the diversity of mechanisms, which give rise to manipulation of the AFM order parameter. Switching mechanisms include non-relativistic spin transfer torques[174], and relativistic spin-orbit torques[170]. Spin-orbit torques can be generated by electric currents in metallic AFM materials such as CuMnAs where sublattices form inversion partners with locally broken inversion symmetry[175]. Order parameter switching is also achieved by electrochemical transformations and electrostatic gating effects, *e.g.*, through liquid ion gating triggering ion motion or electrostatic doping effects[176–178].

AFM spintronics with pure voltage-controlled state variables plays an exceptional role in the overall landscape of spintronics. There are voltage-controlled switching mechanisms where charge flow, apart from the unavoidable and potentially reversible charging associated with the finite capacitance of a device, is absent. Pure voltage-control is achieved via magnetoelectric coupling or voltage-controlled anisotropy. Spin-orbit coupling, which is the fundamental origin of the magneto-crystalline anisotropy, can be voltage-controlled by various mechanisms. One such path exploits a voltage-induced electronic band structure change. It is typically strongest at interfaces[179], preferentially those between ferromagnetic metals and ferroelectrics, where ferroelectric polarization supports strong interface electric fields within the Thomas-Fermi screening length of the metal[180].

Another path utilizes piezoelectrically driven strain effects where magnetoelastic coupling changes the orbital charge distribution and, via spin-orbit coupling, the magnetic anisotropy[181]. The interplay between piezoelectric strain and magnetoelastic coupling is systematically exploited in composite

multiferroics. Multiferroic composite structures can show record breaking magnetoelectric response through interaction between piezoelectric materials (often ferroelectrics as a subset of piezoelectric materials) and ferromagnetic materials in close proximity[182]. The proximity allows for effective stress-strain coupling between the piezoelectric and magnetoelastic materials[183,184].

Pure voltage-controlled switching phenomena can have major advantages over current induced switching schemas with regard to dissipation and Joule heating. At the same time, there are fundamental obstacles associated with voltage-controlled switching of a magnetic order whether it is ferromagnetic or antiferromagnetic. Both magnetic orders are odd under time inversion while the electric field is even. Magnetization is trivially reversed with the help of a magnetic *H*-field, which is odd under time inversion, but it is not straight forward to do so with an electric field. The linear magnetoelectric effect makes a contribution to the Gibbs free energy which is proportional to the product of electric and magnetic field. In the absence of a magnetic field the magnetoelectric energy is zero independent of the strength of an applied electric field[185]. A Legendre transformation relates the Gibbs free energy expressed in terms of fields[186] with the Helmholtz free energy, expressed in terms of order parameters. The leading coupling term in a Landau expansion of the Helmholtz free energy of a proper multiferroic is quadratic in both order parameters[187,188]. This implies that, in equilibrium processes, reversal of the polarization by an electric field leaves the free energy invariant and, hence, the magnetization unaffected. As a result, 180 degree switching of a magnetic order parameter by an electric field is not straight forward to achieve. Among the methods to attain reversal of a magnetic order parameter are dynamic approaches and consecutive 90 degree switches[189]. Dynamic approaches, known as precessional switching, are non-equilibrium in nature and utilize voltage pulses which temporarily reduce the anisotropy barrier between degenerate 180 degree domain states. Proper timing of the pulse width allows to turn on the anisotropy barrier at the right moment to trap the precessing order parameter in its reversed states. The timing, which requires precision on the order of the inverse precession frequency, is technically challenging to realize and renders the approach impractical.

Heron et al. showed that in strain-engineered thin films of the magnetoelectric multiferroic $BiFeO_3$, switching kinetics can lead to reversal of a weak ferromagnetic moment which originates from canting of the AFM aligned spins where magnetoelectric coupling between the AFM order parameter and ferroelectric polarization is exploited for voltage-control[190]. Building on this achievement, Manipatruni et al. used 10 µs voltage pulses to control exchange bias in nanostructured $Co_{0.9}Fe_{0.1}/BiFeO_3$ and $La_{0.7}Sr_{0.3}MnO_3/BiFeO_3$ heterostructures where the multiferroic $BiFeO_3$ serves as the voltage-controlled pinning layer. The effects showed an interesting geometry dependence reflected in improved performance when scaling to sub-micron device dimension[171].

A straightforward way to fulfill the symmetry requirements for voltage-controlled reversal of a magnetic order parameter is achieved when applying a stationary external magnetic field. It can be provided for instance from the magnetic stray-field of a ferromagnetic component of the device such as a tunnel magnetoresistance structure used to readout the free layer orientation which encodes the bit. The magnetic field breaks time inversion symmetry and reversal of the AFM order parameter by an applied electric field becomes possible. Pioneering works using magnetoelectric antiferromagnets and multiferroics have been performed on $Cr_2O_3/CoPt$[191] and $Cr_2O_3/CoPd$[192] as well as $BiFeO_3/La_{0.7}Sr_{0.3}MnO_3$ exchange bias heterostructures[193]. Voltage-controlled exchange bias systems benefit from the simplicity of reading out the state variable encoded in the orientation of the magnetization of the ferromagnetic constituent. However, they suffer from the detrimental delay associated with magnetization reversal and scaling is limited due to the fact that the antiferromagnetic pinning layers have a critical thickness to warrant pinning[194]. In addition, the magnetoelectric energy needed to reverse the ferromagnet decreases with decreasing AFM volume. Hence, structures with reduced complexity, which avoid a ferromagnetic auxiliary component altogether, are favorable for applications as ultra-fast switches.

The diversity of writing/switching mechanics is matched by the vast array of readout mechanisms. Readout can employ exchange coupled ferromagnetic films via the exchange bias mechanism[171,192], or eliminate ferromagnetic components, *e.g.*, with the help of electric transport phenomena. Often, a particular physical mechanism such as the spin Hall effect, can serve a dual role. For example, the giant spin Hall effect is used to write via spin injection followed by spin transfer torque but also employed to read interface magnetization of insulating antiferromagnets[91,192,195] via the corresponding spin Hall magnetoresistance effect. It is worth to mention that significant work is left to do to pinpoint all contributions to the Hall signal in heavy metals on antiferromagnets[196]. The often-dominating spin Hall magnetoresistance contribution originates from a combination of the spin Hall and the inverse spin Hall effect. Generally, there is a far-reaching correspondence between spin torques and magnetoresistance effects. Anisotropic magnetoresistance and tunneling anisotropic magnetoresistance can read magnetic state variables and, just as the spin Hall effect, can be utilized to switch magnetization. Even more exotic are topological read out schemas considered in the field of topological AFM spintronics[197] where the reorientation of the Néel vector can modify the electronic band structure of the AFM material and change transport properties by opening and closing gaps at Dirac points or Dirac nodal lines[198]. In recent years, multiple magnetoelectric memory and logic device architectures have been proposed which all take advantage of the pure voltage-controlled switching through magnetoelectric coupling in either multiferroics or magnetoelectric antiferromagnets[11,199–201].

C. Future Directions

Much attention has been given to the manipulation of AFM ordered states by electric currents which, inevitably, gives preference to the study of metallic antiferromagnets such as AMn with (A=Ir,Fe,Ni, Pt, Pd), Mn_2Au and FeRh, as well as semimetallic and semiconducting antiferromagnets such as CuMnAs, $MnSiN_2$, Sr_2IrO_4, and MnTe[202]. However, enormous potential for ultra-low power spintronics lies in insulating antiferromagnets particularly those which show some form of magnetoelectric response. Recently, a single phase material has been added to the list of antiferromagnets which fulfill virtually all requirements of the ideal material desired for voltage-controlled antiferromagnetic spintronics. The boron doped variation of the archetypical magnetoelectric Cr_2O_3 shows qualitative differences compared with its undoped counterpart making it an outstanding candidate for future AFM voltage-controlled spintronic applications. First and foremost, substitutional anion B-doping increases the Néel temperature and with it the device operation temperature from <307 K of pure Cr_2O_3 to above 400 K for B: Cr_2O_3 such that CMOS compatibility becomes feasible[203]. Most importantly, B-doping of Cr_2O_3 enables reversible, voltage-controlled and non-volatile $\pi/2$ rotation of the Néel vector in the absence of an applied magnetic field[195]. These properties combined can be considered the holy grail of spintronics. Just as pure Cr_2O_3, B: Cr_2O_3 possesses roughness insensitive boundary magnetization[192,204–207]. It accompanies and orients in accordance with the bulk AFM order parameter and can serve as proxy of its orientation. The boundary magnetization can be read by spin Hall magnetoresistance but alternative readout methods can be envisioned. Fig. 39a shows a schematic of a device which serves as a prototype of a non-volatile voltage-controlled antiferromagnetic memory.

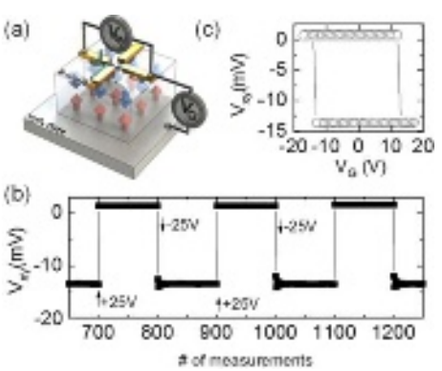

Fig. 39: (a) Pt/B:Cr_2O_3(200nm)/V_2O_3 device structure. V_G is gate voltage, V_{xy} is Hall voltage. (b) Zero H-field switching of V_{xy} in response to V_G switching of ±25 V. (c) A room temperature hysteresis, V_{xy} vs V_G, associated with Néel vector switching in B:Cr_2O_3. (adopted from Ref.[195])

The figure depicts the AFM spin structure of B:Cr_2O_3. A Pt Hall bar is utilized to read the transverse spin Hall signal, V_{xy}, which is generated in response to the electric current flowing in *x*-direction. The control voltage V_G, which allows to rotate the Néel vector, is applied between the top (Pt) and the bottom electrode (V_2O_3 layer). Fig. 39c shows the hysteretic switching between a state of $V_{xy} \approx 0$ (Néel vector and boundary magnetization in the plane) and $V_{xy} \neq 0$ (Néel vector and boundary magnetization out of plane). The coercive voltage of about $V_C = \pm 15$ V can be reduced with decreasing thickness of the AFM film which is 200nm in the example shown in Fig. 39. Extrapolating from transport data obtained in pure Cr_2O_3 thin films[208] and the fact that dielectric properties of the films improve with B-doping one can expect that reduction of the AFM film thickness by one order of magnitude is feasible which potentially brings $|V_c|$ down to desired values of a few V. Fig. 39b shows successive switching events between non-volatile $V_{xy} \approx 0$ and $V_{xy} \neq 0$ states where $|V_G| = 25V > |V_c|$ has been utilized to toggle the Néel vector. It is worth to mention that the pure voltage-controlled Néel vector rotation is not caused by the linear magnetoelectric susceptibility responsible for 180 degree Néel vector switching in similar device structures employing pure Cr_2O_3. As mentioned above, pure Cr_2O_3 requires an applied magnetic field to switch the Néel vector via a non-zero electric field dependent contribution to the Gibbs free energy[206]. Néel vector rotation in the absence of an applied magnetic field cannot be associated with the linear magnetoelectric effect. As outlined in Ref.[195], and corroborated by ongoing investigations utilizing Raman and NV center microscopy, it is likely that the voltage-controlled Néel vector rotation in B:Cr_2O_3 originates from electric field induced orientation of polar nanoregions. Their orientation gives rise to mesoscopic polarization with an associated piezoelectric response. The latter aligns the easy magnetic axis between out of plane and in-plane via magnetoelastic coupling and triggers rotation of the Néel vector.

The example of B:Cr_2O_3 shows that small changes in a material including chemical and electrostatic doping as well as strain-engineering can give rise to qualitative new properties some of which are beneficial for advances in AFM spintronics. A prominent example for strain-engineering is the transformation $BiFeO_3$ from a bulk multiferroic with almost negligible magnetoelectric coupling into a versatile magnetoelectric thin film platform enabling pure voltage-controlled spintronics at room temperature. The voltage controlled switchable boundary magnetization in B:Cr_2O_3 or the switchable weak magnetic moment in $BiFeO_3$ can be further exploited in heterostructures involving two-dimensional materials such as graphene or transition metal dichalcogenides. Here the voltage-controlled antiferromagnets can be utilized to voltage-control Hanle spin precession and other proximity effects which allow to control spin dependent transport in the two-dimensional constituents for logic AFM spintronics applications[209].

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The challenges and opportunities of magneto-electric materials and devices in MESO technology

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Introduction

The Magneto-Electric Spin-Orbit (MESO) device is an innovative logic/memory device proposed by Intel to build next-generation integrated circuits that offer tremendously higher energy efficiency over traditional Complementary Metal-Oxide-Semiconductor (CMOS) technology[11,68]. MESO devices utilize two major physical phenomena – magnetoelectric coupling and spin-orbit coupling to facilitate the switching of order parameters such as ferroelectric ordering and (anti)ferromagnetic ordering. MESO devices have potential advantages over traditional transistors which are based on charge states. Although CMOS scaling has enabled the exponential improvement in computation in terms of lower power consumption, faster switching, and higher transistor density for decades, it is approaching its fundamental limits beyond the nanometer node. The physical limitations are coming from the ability to control charge state and current at a such small length scale. By solving the three-dimensional Poisson equation, the characteristic length of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is given by $\lambda = \sqrt{\varepsilon_{Si}/\varepsilon_{oxide}\, t_{oxide} t_{Si}}$, where ε_{Si} and ε_{oxide} are the electrical permittivity of silicon and gate oxide, respectively, t_{Si} is the silicon film thickness, and t_{oxide} is the gate oxide thickness[9,210]. When the gate length is close to the characteristic length, the depletion regions of the source and drain start to overlap, known as the short channel effect. This greatly reduces the ability of the gate terminal to control the leakage current between source and drain. There is also the fundamental limitation of 60 mV/decade subthreshold swing which limits the threshold voltage and supply voltage scaling. On the other hand, MESO devices are not subject to the same scaling limits due to different operation principles. The memory and logic bit switching rely on altering the state of order parameters, such as ferroelectric polarization and ferromagnetic moments, which are thermally stabilized by the energy barrier, $\Delta E(\Theta)$, also known as retention energy, as a function of a given order parameter. The typical requirement of $\Delta E(\Theta)$ is ~80 k_bT (0.33 aJ) for 10 years of retention in 1Mb array at room temperature with an error rate of less than 1 ppm, or ~40 k_bT (0.16 aJ) for logic operation[1,211]. By utilizing two quantum phenomena, magnetoelectric coupling, and spin-orbit coupling, researchers from Intel and Berkeley have demonstrated and forecasted a pathway to achieve 10 aJ switching of order parameters at room temperature[11]. The Magneto-Electric Spin-Orbit (MESO) technology provides an exciting new approach to building integrated circuits, which offers potential advantages over traditional CMOS devices in terms of energy efficiency, scalability, and compatibility with

existing manufacturing techniques. As a result, MESO devices are viewed as a promising means of advancing beyond-CMOS devices for computing and sustaining the long-term progression of Moore's law.

In this perspective, we provide an overview of the genesis and recent advancements in MESO devices, followed by an examination of the challenges and opportunities in materials and devices, particularly in the magneto-electric (ME) module.

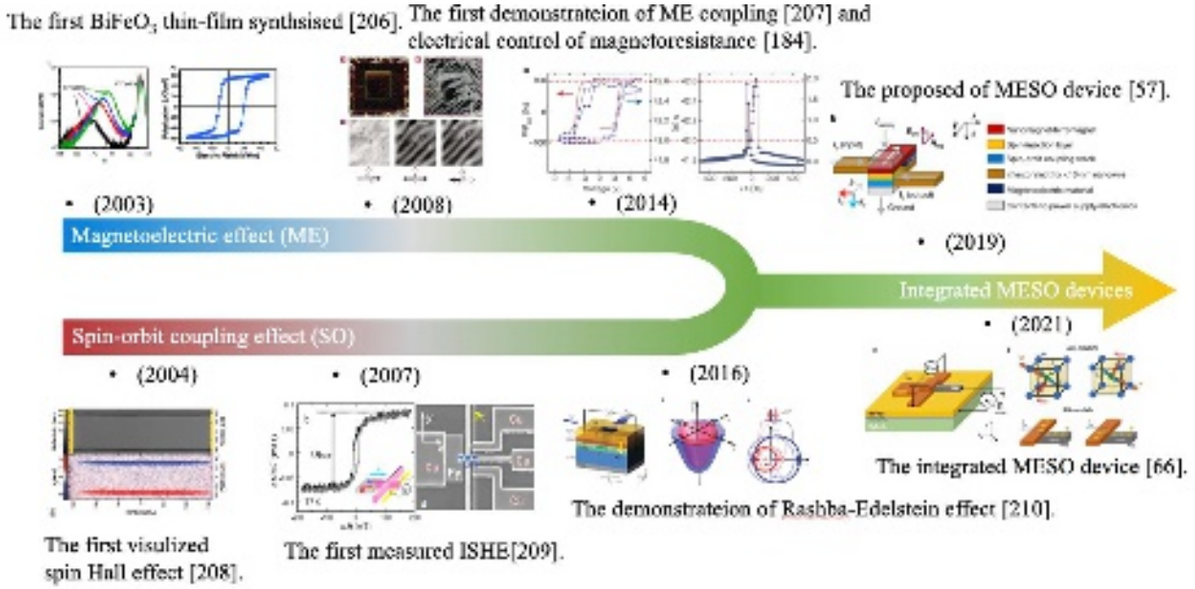

Figure 40. The development of multiferroic $BiFeO_3$ thin films, (inverse) spin Hall effect, and the concept of MESO device. (In the figure, [206]→[212], [207]→[213], [184]→[190], [57]→[11], [208]→[214], [209]→[215], [210]→[216], [66]→[68].)

The development of MESO devices

Starting from the multiferroic bismuth ferrite ($BiFeO_3$, BFO), BFO is by far the most studied single-phase multiferroic for the coexistence of two order parameters above room temperature - ferroelectric polarization and antiferromagnetism. Furthermore, it was observed that a canting of the magnetic moments in BFO is possible, resulting in a weak ferromagnetic moment (M_C) ~8 emu/cm^3 described by the Dzyaloshinskii-Moriya (DM) interaction. A groundbreaking paper published in 2003 by Wang et al., which focused on the growth and characteristics of thin films of BFO, sparked a flurry of research on this topic that has persisted until the present day. The paper demonstrated improvements in polarization ~90 μC/cm^2 and most importantly it reported a magnetoelectric coupling coefficient ~ 3 Vcm/Oe at zero field[212]. In 2008, Chu et al. published a comprehensive study in which they reported the first visual proof of electrical control of antiferromagnetic domain structures in a single-phase multiferroic at room temperature. They used piezoresponse force microscopy (PFM) to image ferroelectric domains and x-ray circular dichroism photoemission electron microscopy (XMCD-PEEM) to image ferromagnetic domains with the heterostructures of $Co_{0.9}Fe_{0.1}$/BFO. By combining the two imaging techniques, they were able to directly observe changes in the ferromagnetic domain structure in $Co_{0.9}Fe_{0.1}$when an electric field was applied. Due to the nature of the biaxial symmetry of Néel vector, it is argued that the switching of canted moment is non-deterministic unless an external

field is applied to break the symmetry. In 2014, Heron et al., demonstrated the deterministic 180º-switching of magnetization in the spin-valve/BFO heterostructures. One key to achieving this deterministic switching in BFO is realized by the two-step switching of ferroelectric polarization, a combination of 71º and 109º switching. This mechanism helps to lower the energy barrier required for switching and also provides a symmetry-breaking switching trajectory that has been observed through time-resolved PFM and modeled using DFT[190]. While this section focuses electric field controllable magnetism, it's noteworthy that an alternative method exists for manipulating magnetism through optical means. Kundys et al.[217] showcased a notable alteration induced by visible light in the dimensions of $BiFeO_3$ crystals at room temperature, hinting at the possibility of integrating mechanical, magnetic, electric, and optical functionalities in forthcoming remotely switchable devices. Additionally, Liou et al[218] documented the manipulation of various ferroic orders in an epitaxial mixed-phase $BiFeO_3$ thin film under ambient temperature conditions through laser illumination.

The second module, spin-orbit (SO), of MESO device relies on the spin-orbit coupling namely the (inverse) spin Hall effect ((I)SHE) to transduce the order parameter of magnetization to a sufficient voltage. The spin Hall effect is a fascinating phenomenon in condensed matter physics that has received a great deal of attention in recent years[219,220], for its potential in low power Spin-Orbit Torque Magnetoresistive Random Access Memory (SOT-MRAM) technology. It refers to the generation of a transverse spin current, perpendicular to the direction of an applied electric field, typically in heavy materials with strong spin-orbit coupling, such as Pt, W, and Ta[221]. The effect was first predicted theoretically in the 1970s[222], but experimental observations of SHE had to wait until the early 2000s due to the lack of materials with sufficiently strong spin-orbit coupling. Kato et al. used magneto-optical Kerr imaging to demonstrate the first observation of the Spin Hall effect at room temperature, which occurred at the edges of a GaAs semiconductor channel[214]. At room temperature, researchers demonstrated the measurement of spin Hall voltage at the opposite end of an Al wire after observing the spin Hall effect at the edges of a GaAs semiconductor channel via magneto-optical Kerr imaging. The experiment utilized a perpendicularly magnetized FePt and an Au Hall bar, and both spin Hall and inverse spin Hall effects were recorded at a separation of 70 nm between the injector and detector, with magnitudes reaching 2.9 mΩ. spin pumping[215]. Recently, researchers observed an inverse Edelstein voltage at the Rashba-split two-dimensional electron gas at the interface of $SrTiO_3/LaAlO_3$[216] and the spin-momentum locking in topological insulators[223,224]. These systems demonstrate high efficiency in transferring charge to spin and are suggested to be utilized as the spin-orbit (SO) module in MESO devices.

With this background, in 2019, the research teams from Intel and Berkeley proposed the concept of MESO devices and experimentally proved there is a clear pathway to achieve attojoule level switching of order parameters[11]. The MESO device proposed offers several advantages over current logic and memory technology, including (1) the non-volatility in order parameters can enable new building blocks for new computation architecture such as compute-in-memory and brain-inspiring computing[225], (2) the excellent voltage scalability to scale energy per operation to attojoule-level with switching energy about 30 times lower than advanced CMOS devices, (3) significant improvement in logic density, up to 5 times compared to advanced CMOS devices, facilitated by majority-gate circuits implemented with a collective switching device[69,226]. In the latest IEDM conference, Intel reported their latest progress on the ME module of MESO devices[227]. With the 6-nm La-doped BFO thin film, they demonstrated asymmetric 150 mV driven ME switching with a characteristic switching time of 1.95 ns.

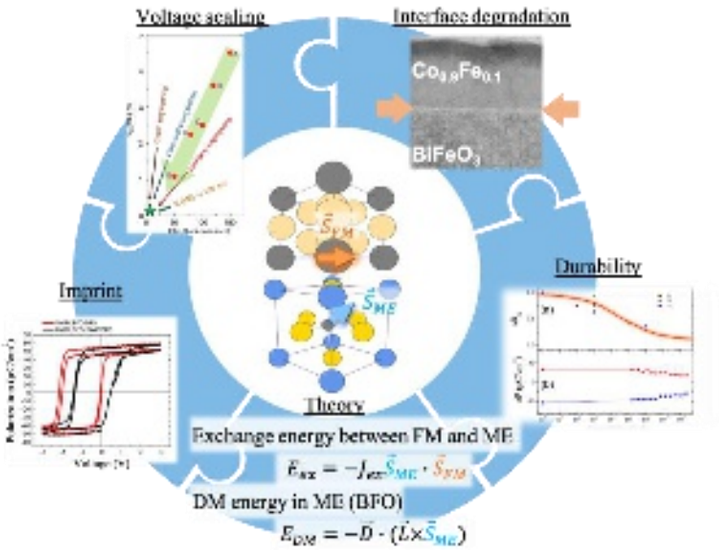

Figure 41. Challenges of the ME module.

The challenges and opportunities of MESO devices

Voltage scaling

In our 2019 publication, we outlined several possible approaches to scale the ME switching voltage, such as chemical doping, interface engineering, strain engineering, and thickness scaling[11]. Of these methods, we demonstrated that the replacement of bismuth by lanthanum via chemical doping in BFO (LBFO) thin films is an effective means of reducing the ME voltage[87,228]. While the substitution of lanthanum in BFO thin films softens the ferroelectric ordering, leading to a reduction in remanent polarization and coercive voltage, we note that this alteration also affects the exchange coupling between the ferromagnetic and magnetoelectric layers[228]. This is because the antiferromagnetic easy axis in the LBFO layer is no longer parallel to the parent phase of BFO driven by the crystal symmetry transformation from rhombohedral to monoclinic.

Besides the abovementioned strategies to scale down the switching voltage, researchers from Berkeley demonstrated that removing the substrates from epitaxial ferroelectric films can greatly improve the switching voltage and speed[229,230]. For example, in BFO freestanding membranes ~a 40% reduction of the switching voltage and a consequent ~60% improvement in the switching speed can be achieved. The open questions include (1) what is the ultimate limit for voltage switching? and (2) Can the magnetoelectric coupling follow the ferroelectric switching?

Imprint issues

The ferroelectric imprint effect is observed when a ferroelectric material exhibits a preference for one polarization state over the opposite one, resulting in a higher voltage requirement to overcome the preferred polarization state. The opposite polarization state has a strong tendency to switch back to the preferred state. This asymmetric preference issue is particularly crucial for ultralow voltage switchable ferroelectric thin films as the small thermal energy barrier makes it possible to have only one stable polarization state at zero bias. There are two major issues that can arise for MESO devices due to this effect. Firstly, there is a risk of write failure caused by the asymmetrical shift in the coercive voltage. Secondly, a potential memory loss can happen because the non-preferred polarization state does not have a stable remanent polarization. To resolve this issue, a typical approach is to balance the work functions between the interfaces of the top electrode/ferroelectric layer/bottom electrode using

conductive oxide electrodes[231,232]. However, in the application of the ME module, it is still essential to use the metallic ferromagnetic layer to transduce order parameters. Thus, we can only tune the bottom electrode materials to manipulate the polarization preference of the ME layer. Building upon our earlier research, in which we demonstrated the ability to manipulate the as-grown polarization state of ferroelectric thin films by engineering the bottom electrode materials, including termination control and conductivity tuning, we have incorporated a $La_{0.7}Sr_{0.3}MnO_3$/$SrRuO_3$ (LSMO/SRO) heterostructure as the bottom electrode for our ME module[233,234]. The SRO layer is designed for conductivity improvement as shown in Figure 41.

Interface degradation and durability

The realization of room temperature ME switching to date relies on ferromagnets/multiferroics heterostructure, for example, $Co_{0.9}Fe_{0.1}$/BFO. With a strongly coupled magnetic ordering, researchers have demonstrated the electric control of magnetization[190,213], exchange bias[171], exchange coupling strength[87,228], etc. This interlayer exchange coupling can be described by two energy terms:

1. the exchange energy between the $Co_{0.9}Fe_{0.1}$ layer and the BFO layer $E_{ex} = -J_{ex}\vec{S}_{M_C} \cdot \vec{S}_{Co_{0.9}Fe_{0.1}}$, where J_{ex} is the exchange coupling coefficient, $\vec{S}_{M_C}$ is the spin momentum of the canted moment in the BFO layer, and $\vec{S}_{Co_{0.9}Fe_{0.1}}$ the spin momentum of the moment in the $Co_{0.9}Fe_{0.1}$layer,
2. the DM energy in the BFO layer [235] $E_{DM} = -\vec{D} \cdot (\vec{L} \times \vec{S}_{M_C})$, where $\vec{D}$ is the DM vector, $\vec{L}$ is the Néel vector in the BFO layer. In the system of BFO, the $\vec{D}$ is parallel to the ferroelectric polarization $\vec{P}$.

Based on these two energy terms, it is evident that a substantial magnetization of the ferromagnetic layer is necessary to achieve robust interlayer coupling. Therefore, transition ferromagnetic metals are selected for transducing the order parameters (P and M). However, the high activity of transition metals, Co and Fe in our ME case, can lead to oxidation at the interfaces. This can result in the formation of non-magnetic or antiferromagnetic oxide layers at the interface, thereby diminishing the coupling between the ferromagnetic and ferroelectric layers shown in Figure 41. Additionally, the oxidation of the ferromagnetic layer can also reduce its magnetization (increasing the thickness of the dead layer), further weakening the coupling strength between the layers of ferromagnets and multiferroics. As a result, even the ferroelectric polarization can be cycled up to 10^9, the exchange coupling strength dimmishes way ahead of ferroelectric polarization at around 10^6 cycles, as shown in Figure 41. Tremendous efforts have been made to utilize oxide ferromagnets such as $La_{0.7}Sr_{0.3}MnO_3$ to prevent this oxidation issue and achieve better interface quality with cube-on-cube epitaxial growth[236,237], but the interlayer coupling is only limited at low temperatures.

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Magnetoelectric Memory Devices

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For many decades, magnetic-based technologies such as magnetic recording and magnetic tape have been the mainstay of data storage systems. Their prevalence can be attributed to their superior capacity, non-destructive readouts, and the ability to be produced en masse in a cost-effective manner. Beyond storage, magnetic-based memories, specifically magnetic random-access memory (MRAM), are emerging as prime candidates for the next generation of nonvolatile memory solutions[16]. These can potentially address the persistent issue of memory wall, which plagues the von Neumann architecture[17]. The foundational structure of MRAM is rooted in the principles of spin valve devices, where the resistance state of the device is governed by the relative magnetic configuration of two metallic magnetic layers, separated by a nonmagnetic spacer layer. Historically, the manipulation of one of these magnetic layers - the free layer (FL) - was achieved using a magnetic field, thereby facilitating the toggle of resistance states in these devices. However, the complex cell architecture and high-power consumption intrinsic to this approach have posed significant hurdles to its marketability. Considering these difficulties, current-induced switching mechanisms like spin-transfer torque (STT) and spin-orbit torque (SOT) have been introduced, significantly impacting the technological progression of MRAM devices. While these mechanisms show advantages over magnetic-field-assisted switching in terms of scalability and energy efficiency, their operational energy (10-100 fJ/bit) still surpasses that of CMOS devices (< 1fJ/bit). Additionally, the notorious Joule heating effect associated with current-driven devices presents a considerable challenge, particularly for STT, given the requirement for large switching currents. As a promising alternative, the exploitation of voltage or an electric field to control magnetism has emerged as a more energy-efficient approach. This technique holds the potential to reduce energy consumption to well below 1 fJ/bit, and potentially even to the aJ/bit range[183].

There are multiple methods to control magnetism using electric fields, such as modifying the magnetic moment by transitioning the phase from antiferromagnetic/paramagnetic to ferromagnetic, varying the anisotropy of the film, adjusting the exchange coupling between two ferromagnetic layers, and even altering the magnetization direction, among others[238]. Recently, ionic gating has been employed to alter the magnetic phase of the metallic/semiconducting layer; however, integrating these systems with spintronic devices is challenging due to their poor scalability, slow switching speed (within the millisecond range), and the complexity inherent in device fabrication[32].

The conventional technique for voltage control of magnetism used to manipulate the magnetic state of the free layer (FL) in cutting-edge Magnetic Tunnel Junction (MTJ) stacks involves the voltage-controlled magnetic anisotropy (VCMA) effect[1]. The primary obstacle with this technique is achieving a higher VCMA effect (> 200 fJ/V-m) to realize entirely voltage-driven switching in the MTJ stack. Multiple insertion layers, such as Hafnium (Hf), Iridium (Ir), Palladium (Pd), etc., have been introduced at the FL/MgO interface to augment the VCMA effect, yet a robust system with the required

VCMA effect remains elusive. An additional concern regarding the VCMA effect is the non-deterministic nature of the switching, which necessitates an in-plane magnetic field to ascertain the switching direction. Furthermore, the perpendicular magnetic anisotropy (PMA) of the FL decreases with one polarity of applied voltage but increases for the opposite polarity, making the combination of VCMA with the spin-transfer torque (STT) effect energetically favorable only in one direction of applied current/voltage. Thus, despite sharing a similar architecture with traditional STT-MRAM devices, VCMA-based MRAM devices do not present a promising technological prospect until the aforementioned issues are rectified. A recent addition to voltage-induced switching techniques, the voltage-controlled exchange coupling (VCEC)[239], has been documented, which can be readily integrated into the conventional MgO-based MTJ stack for MRAM applications. The principal advantage of VCEC over the VCMA effect is its deterministic nature and its compatibility with the STT effect for bidirectional energy-efficient switching of MRAM devices. However, this research area is still in its early stages, and a comprehensive demonstration of such a device with a significant breakthrough remains to be achieved.

Another compelling method to govern magnetism involves leveraging the magnetoelectric coupling property inherent to single-phase multiferroics. In these systems, the exchange interaction between the ferromagnetic film and the multiferroic materials' antiferromagnetic order is harnessed to manage the ferromagnetic film's magnetic state via the applied voltage/electric field. Initial efforts in this direction entailed manipulating a single ferromagnetic layer's magnetic state. Utilizing a blend of magnetometry and anisotropic magnetoresistance (AMR) measurements, Laukin *et al*[240]. pioneered the electric field control of exchange bias in Py/$YMnO_3$ heterostructures at 2 K.

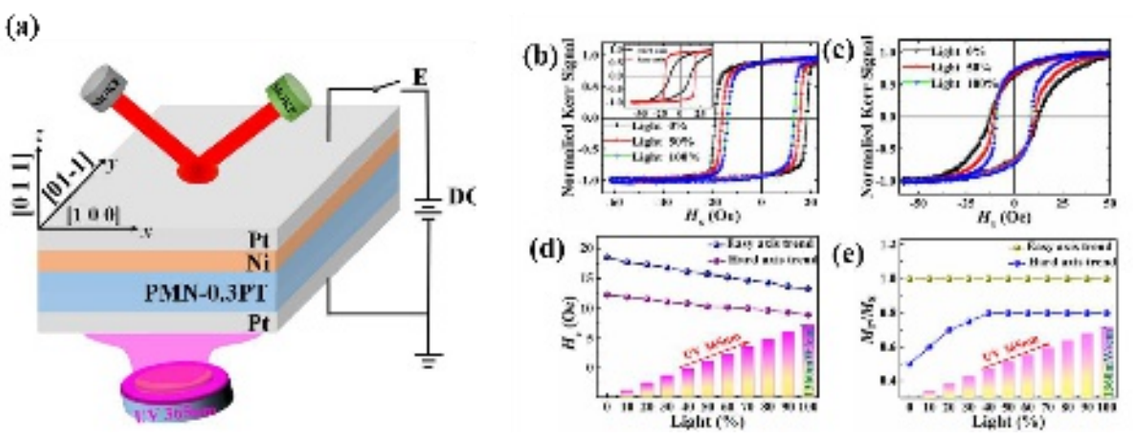

Figure 42: (a) Schematic of the (011) Ni/PMN-PT heterostructure with the experimental setup. Normalized magnetic hysteresis loops at varying light intensities (50% and 100%) for the easy (b) and hard (c) magnetic orientations (with an inset in (b) depicting the normalized Kerr effect hysteresis loops across both magnetic directions). Graphs showing changes in coercive field (d) and the remanence ratio (e) for both the easy and hard magnetic orientations under different light exposures[241].

Building on the concept of electric field control, the domain of optical control in artificial ferromagnetic (FM)/ferroelectric (FE) heterostructures presents an equally compelling avenue for the modulation of magnetic properties. This method transcends the limitations of electric field manipulation, offering non-invasive operation and opportunities for device miniaturization—key advantages in the quest for energy-efficient spintronics devices. Iurchuk et al.[242] demonstrated a

remarkable light-induced coercivity modulation in a nickel (Ni) thin film deposited on a ($BiFeO_3$) FE layer, unveiling the potential of optical means for magnetic control. Kundys et al.[243] further explored this realm by showing how the wavelength of incident light could dictate magnetic anisotropy within a CoFe/BFO ME heterostructure, indicating new possibilities for wavelength-specific magnetic modulation. Zhang et al. [241] addressed the challenge of the low photostriction response time of BFO by achieving coercivity modulation in a Ni thin film within a Ni/$Pb(Mg_{1/3}Nb_{2/3})O_3$-PT (PMN-PT) ME structure (see **Figure** 42), paving the way for more responsive and efficient optical control mechanisms. Additionally, Pathak et al.[244] introduced the concept of light-induced dynamic magnetization, presenting a method with practical relevance for remote-tunable oscillators in neuromorphic and other spin-based applications, thereby broadening the scope of optical control in magnetoelectric memory devices. These advancements collectively signal a shift towards more versatile and efficient methods for magnetic control in ME memory devices. While this article is primarily focused on the direct electric field manipulation of magnetic states, the exploration of optical control in FM/FE heterostructures opens up new frontiers in the design and implementation of energy-efficient, high-performance spintronics devices. By harnessing both electric and optical means to modulate magnetic properties, a new generation of magnetoelectric memory devices combines the best of both worlds—energy efficiency, miniaturization, and enhanced control over magnetic states.

The discovery of magnetoelectricity in multiferroic BFO has instigated a paradigm shift in voltage-controlled magnetism, primarily owing to strong exchange coupling of BFO with neighboring ferromagnets[245]. Considering this, the reversible modulation of the magnitude and even the sign of exchange bias at the $LaSrMnO_3$ (LSMO)/BFO interface has been demonstrated by applying out-of-plane electric fields through BFO[178], albeit under sub-room temperature conditions. To capitalize on the room temperature magnetoelectric properties of multiferroic BFO, the magnetoelectric coupling with a conventional ferromagnet, such as Cobalt Iron (CoFe), exchanged coupled with BFO, has been evidenced through conventional magnetometry, AMR, and X-ray Magnetic Circular Dichroism-Photoemission Electron Microscopy (XMCD-PEEM) imaging[178,246].

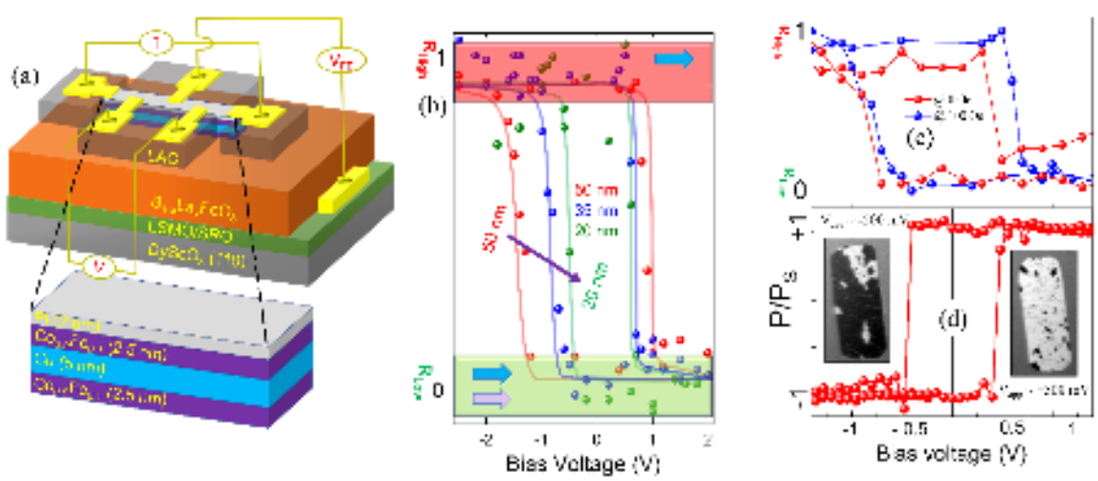

Figure 43: (a) The magnetoelectric testing structure composed of a CoFe–Cu–CoFe spin valve interfacing with a La doped-BFO (BLFO) film surface. (b) The modulation of the spin valve device's resistance (normalized resistance) fabricated on BLFO films when varying bias voltage is applied

across the BLFO layer with different film thicknesses. (c) The resistance modulation trend of a spin valve device, integrated with a 35 nm BLFO film and subjected to a background field of 100 and 0 Oe magnetic fields. This emphasizes that the background magnetic field doesn't influence the electric field modulation of the spin valve's resistance state. (d) A piezoelectric loop of a 20 nm BLFO film shows the ferroelectric switching voltage at 500 mV. The XMCD-PEEM images (seen in the inset) of the Pt/CoFe strips, obtained under a preset magnetic field pulse of 100 Oe, disclose a 180-degree magnetization reversal when 500 mV is applied across the BLFO film[193].

For the development of commercially viable memory/logic technology using magnetoelectric multiferroic systems, it is crucial to integrate spintronic devices with multiferroic materials. The foundational structure of spintronic devices lies in the spin valve. The first instance of deterministic switching of the resistance state of spin-valve devices purely by the applied electric field was demonstrated by Heron *et al*[247]. Subsequent research in this field has focused on the creation of ultra-low power switching architectures to actualize devices with operational energy in the attojoule per bit range[248]. Indeed, a recent demonstration by Prasad *et al*[193]. showcased magnetoresistive switching of spin-valve devices at or below 200 mV, indicating a potential pathway to achieve switching at 100 mV (see **Figure 43**). This was accomplished by fine-tuning the film thickness, the composition of multiferroic films, and performing interface engineering[87]. As previously mentioned, the ferroelectric switching voltage of BFO can be minimized by doping with La or Sm[190]. Another strategy to reduce the switching voltage involves decreasing the film thickness. By optimizing La doping within the 10-20% range and reducing the multiferroic film thickness to 10 nm, it has been possible to achieve attojoule-class magnetoelectric-based non-volatile memory devices. These devices have demonstrated a corresponding switching energy density of approximately 10 μJcm^{-2} (as illustrated in the **Figure 44**)[11].

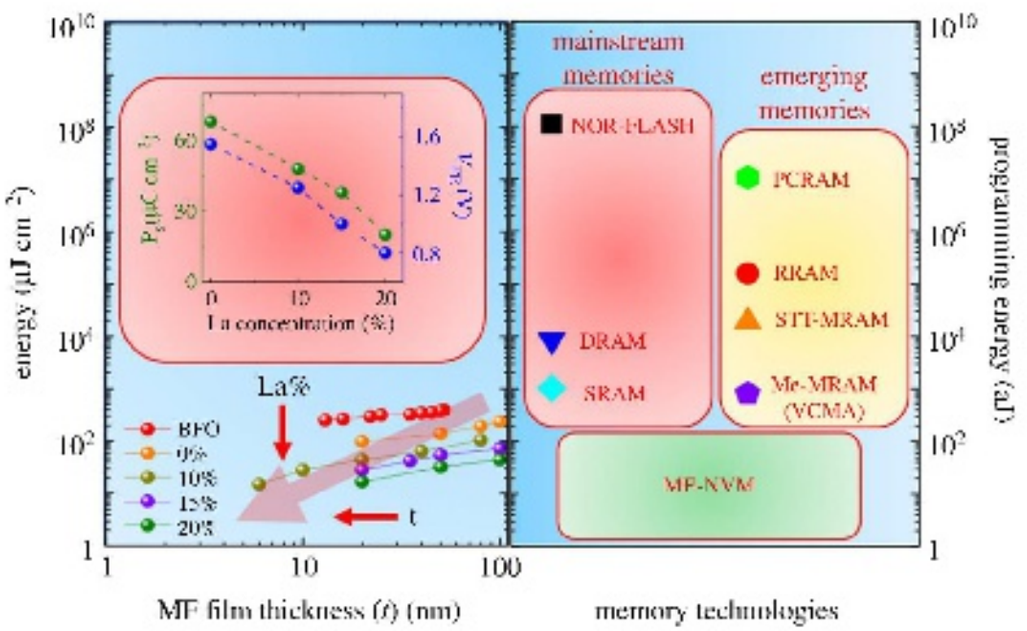

Figure 44: The graphic presents the latest advancements in modulating the switching voltage and spontaneous polarization of BiFeO3 through La-substitution and film thickness alterations at the Bi-site. This, in turn, contributes to decreased energy consumption, as demonstrated in the left panel. The right panel of the figure contrasts conventional memory technologies (NOR-FLASH, DRAM, and

SRAM) with emerging memory options (PCRAM, RRAM, STT-RAM, and ME-MRAM), and includes a comparison with magnetoelectric non-volatile memory-based logic (ME-NVM)[11].

Although progress has been made in achieving electric field-induced deterministic switching of spin-valve devices using multiferroic magnetoelectric materials, their integration with traditional MRAM technology remains to be demonstrated. This is primarily due to the complexities inherent in three-terminal device structures that include an MgO tunnel barrier layer. Furthermore, the weak magnetoelectric coupling in single-phase multiferroic materials poses a challenge to implementing purely voltage-driven switching of the Free Layer (FL) in the Magnetic Tunnel Junction (MTJ) structure. Device endurance is another critical concern that requires resolution, especially with respect to the irreversible oxidation of the ferromagnetic layer under recurring switching electric fields. This issue could potentially be mitigated by utilizing a ferromagnetic oxide electrode[228], yet the realization of an MTJ structure with a decent Tunnel Magnetoresistance (TMR) percentage (exceeding 100%) with MgO-based or even non-MgO-based tunnel junctions is challenging to achieve at room temperature. Another strategy for integrating multiferroic material into MTJs involves incorporating a multiferroic (MF) insulating spacer, serving as a tunnel barrier, between two Ferromagnetic (FM) electrodes[249]. This could result in four resistance states due to the ferroelectric and ferromagnetic properties of the barrier layer. However, no demonstration at room temperature has been reported to date, indicating there are significant strides to be made in the realization of any feasible memory/logic technology employing these devices.

In response to these challenges, there has been a burgeoning interest in examining composite systems that integrate ferromagnetic elements with ferroelectric or piezoelectric materials. An early approach in this vein aimed to create vertically aligned nanocomposite systems that incorporate ferromagnets within a ferroelectric/piezoelectric matrix. In 2004, Zheng H *et al*[250]. reported on such a nanocomposite system where the ferromagnetic spinel, $CoFe_2O_4$ (CFO), was epitaxially embedded within a ferroelectric perovskite matrix of $BiFeO_3$ (BFO). They found that the magnetic state of the ferromagnetic CFO could be switched electrically utilizing the magnetoelectric coupling of the BFO matrix. For deterministic switching of the CFO layer's magnetization direction, a minor magnetic field was needed for the nanopillar arrays during the electric-field-induced switching. While several other vertically aligned nanocomposite systems have been studied for magnetoelectric switching, the integration of spintronic devices into these systems poses significant difficulties[251].

A different method for leveraging composite magnetoelectric systems in spintronics applications involves the use of artificially fabricated ferromagnetic/ferroelectric (FM/FE) multiferroic heterostructures. These structures offer significant technological appeal due to their notable magnetoelectric coupling at room temperature and their compatibility with a variety of ferroelectric and ferromagnetic materials. The underlying physical mechanisms for magnetoelectric coupling in these heterostructures generally involve exchange, charge, and strain-mediated effects.

Electric field control of exchange coupling at the FM/FE interface has been specifically demonstrated with single-phase multiferroic materials (e.g., BFO), as previously noted. For charge-mediated systems, the interfacial electronic structure of the ferromagnet in contact with the ferroelectric material is modulated by toggling the ferroelectric polarization states with an applied electric field. This alteration subsequently changes the magnetic properties (e.g., magnetic anisotropy, coercive field, magnetic moments, etc.) of the ferromagnetic layer[252]. Unlike strain and charge-mediated effects, strain-mediated effects provide an indirect means of controlling the magnetism of the ferromagnetic film in FM/FE heterostructures[253]. In this mechanism, voltage-induced strain in the ferroelectric/piezoelectric film — resulting from the converse piezoelectric effect — is transferred to

the adjacent ferromagnetic film. Consequently, this alters its magnetic properties through the converse magnetostriction effect.

Several studies have demonstrated modulation of the magnetic properties of a singular ferromagnetic layer via exchange, charge, and strain-mediated effects[254]. Nevertheless, the challenge remains to manipulate the giant magnetoresistance (GMR) and tunnel magnetoresistance (TMR) responses of spin-valve/magnetic tunnel junction (MTJ) devices through these mechanisms. These manipulations are essential to creating feasible nonvolatile memory solutions boasting high endurance, reversible switching, minimal energy dissipation, and scalability. Notably, the majority of remarkable multiferroic-based magnetoelectric switching of GMR and MTJ devices has been primarily demonstrated in film stacks possessing in-plane magnetic anisotropy. Until now, MTJ stack switching has been accomplished via the strain-mediated effect utilizing ferroelectric PMN-PT substrates[255]. However, devices with perpendicular magnetic anisotropy (PMA) are deemed more appealing for the creation of next-generation high-density memory solutions. While recent studies have reported electric field manipulation of PMA films through strain-mediated magnetoelectric coupling[253,254], the successful and robust integration of such a switching mechanism into perpendicular MTJs warrants additional exploration.

Currently, single crystalline oxide substrates predominantly serve as the base for the growth of high-quality epitaxial multiferroic oxide materials. However, recent developments have indicated that free-standing multiferroic films may be more energy efficient when it comes to realizing the magnetoelectric (ME) coupling effect[256]. Notably, such free-standing films have helped to mitigate the substrate clamping effect, especially in the context of the strain-mediated ME effect. The endeavor to integrate perovskite-based multiferroic materials with silicon remains challenging, yet ongoing, with the goal of developing complementary metal-oxide-semiconductor (CMOS)-compatible technology. Another hurdle lies in maintaining the stability of polar phases when scaling down the thickness of ferroelectric films. This is crucial to preserving ME coupling in single-phase multiferroic films. Recent studies have reported that such ME coupling in bismuth ferrite (BFO) thin films can be preserved even at thicknesses as low as 5 nm[87,257].

When developing technology with such thin films, it is also necessary to consider potential issues with dielectric leakage. One potential solution could be to reduce the lateral device size to less than 20 nm, although this requires a sophisticated device fabrication process due to the intricacies of three-terminal structures. The challenge of etching oxide film nanopillars of such size, particularly to avoid damaging the films from the sidewall—which could potentially lead to leakage—remains a significant obstacle.

Despite numerous hurdles to be overcome in achieving purely voltage-driven memory technology, the potential for significant energy consumption reductions, compared to current-driven devices, continues to hold the scientific community's attention. To address integration challenges, novel device fabrication strategies for these material systems need to be identified, necessitating more translational research and development efforts. Moreover, the pursuit of novel materials and the investigation of fresh mechanisms and physics continue in the fields of multiferroics and magnetoelectrics. Such ongoing efforts are expected to yield further substantial breakthroughs in this area, contributing to future advancements in the field.

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Ferroelectric devices for low power electronics

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Status

Ferroelectric materials have a non-centrosymmetric crystal structure, resulting in a spontaneous polarization that can be switched by an electric field. Multiple stable polarization states and the electric field-based switching mechanism make ferroelectrics ideal for applications in low-power non-volatile memories[258]. Depending on the read-out mechanism, three basic memory concepts can be distinguished: Ferroelectric random-access memory (FeRAM), ferroelectric tunnel junction (FTJ), and ferroelectric field-effect transistor (FeFET). In FeRAM and FTJs, the polarization state of a ferroelectric capacitor is read out through the displacement current and static leakage current, respectively. In a FeFET, the ferroelectric is integrated into a transistor and the polarization state is read out via the drain current. Ferroelectric memories are of interest not only for von Neumann based computing architectures, but especially for emerging paradigms such as neuromorphic computing, logic-in-memory, and non-volatile logic[259,260]. Additionally, ferroelectrics can exhibit a negative capacitance (NC) when their overall polarization is suppressed[261]. By intentionally suppressing the ferroelectric polarization in a FeFET-like structure, the gate voltage can be amplified through the NC effect without hysteresis[262]. This so-called NCFET exhibits a reduced equivalent oxide thickness (EOT) and operating voltage compared to conventional MOSFETs and can in principle overcome the "Boltzmann-limit" of 60 mV/decade subthreshold swing at room temperature[263]. Therefore, ferroelectric NCFETs are promising contenders for future low power and high-performance logic devices. Additionally, some ferroelectric devices can also be influenced by light through photoferroelectric effects. For example, it has been demonstrated that the storage state of FTJs can be affected by illumination[264]. The underlying mechanism of photoferroelectrics can be either photostriction[241,243,265] or pyroelectricity[266,267], depending on the wavelength of the light used.

Historically, most research on ferroelectrics has been focused on low-power digital memory[258]. While FeRAM based on perovskite ferroelectrics such as lead zirconate titanate has been commercialized in the 1990s, these products could not be scaled beyond the 130 nm node[268]. FeFETs based on perovskite ferroelectrics could not be commercialized due to scaling, integration, and reliability issues. Only the recent discovery of scalable HfO_2 and ZrO_2 based ferroelectrics of fluorite structure led to a resurgence of interest in low-power electronic device applications[269,270]. These CMOS compatible materials can retain their ferroelectricity down to the unit cell limit and can be grown on 3D structures using atomic layer deposition[268,271]. HfO_2 based FeRAM and FeFET memory arrays have been demonstrated on a wafer scale down to the 130 nm and 22 nm nodes, respectively[272,273]. Recently, a 32 Gbit chip with two layers of stacked 3D ferroelectric capacitors and 48 nm pitch has been demonstrated[274]. Ferroelectrics with wurtzite structure such as AlScN have been discovered[275], which exhibit a high spontaneous polarization and temperature stability with possible applications in FeRAM. Furthermore, ultrathin 2D van der Waals ferroelectrics such as $CuInP_2S_6$ and α-In_2Se_3 have attracted attention for applications in FeFETs and FTJs[276]. The following sections aim to give a high-level overview of the challenges, advances, and future directions of ferroelectric devices with a focus on the practically most relevant fluorite structure materials.

Current and future challenges

There are different challenges with respect to the various applications of ferroelectrics in low power electronics (FeRAM, FeFET, FTJ, NCFET). Therefore, this section is divided by application.

1) FeRAM

Due to their CMOS compatibility and relatively high spontaneous polarization, fluorite and wurtzite structure ferroelectrics are most promising for FeRAM applications[269,275]. Currently, one of the main challenges for FeRAM is reliability[258,268]. The electric field needed to fully switch the polarization of fluorite and wurtzite structure ferroelectrics is relatively close to their breakdown field strength, which limits the cycling endurance. However, when the cycling voltage is reduced, partial switching results in a reduced switchable polarization[277]. This trade-off is exacerbated by the polycrystalline film morphology of fluorite structure ferroelectrics, leading to a distribution of switching fields[278]. For wurtzite structure ferroelectrics, further scaling of both the switching field and the film thickness is needed to reduce the switching voltage and to improve reliability. Additionally, fluorite-structure ferroelectrics often exhibit the so-called wake-up effect, where initial endurance cycling increases the switchable polarization[277]. Lastly, good imprint and retention behavior especially for reduced film thicknesses and high temperatures needs to be demonstrated.

2) FeFET

For FeFET applications, fluorite structure ferroelectrics seem most promising for applications due to their similarity to conventional HfO_2 based gate dielectrics[279]. In general, parasitic charge trapping phenomena and limited cycling endurance are the most prominent challenges for reliable FeFET operation. The dielectric interfacial layer (IL) between the ferroelectric and the semiconductor channel often limits FeFET memory performance[280]. Parasitic charge trapping can lead to undesirable read-after-write latency[281]. Furthermore, polarization switching induces a large field across the IL, which can lead to dielectric breakdown[280]. When scaling down lateral FeFET dimensions, device-to-device variation might be a concern due to the multi-phase, polycrystalline nature of fluorite structure ferroelectric thin films[282]. Therefore, improving the film uniformity will be critical for further FeFET scaling. 3D integration of FeFETs in a 3D NAND architecture is promising to increase the bit density, but challenges due to pass voltage disturbs need to be addressed[283]. In general, read and write disturbs need to be improved to increase the size of FeFET memory arrays[284]. For applications of FeFETs in neuromorphic devices, achieving linearity and symmetry of conductance modulation with identical voltage pulses is difficult due to the inherent nucleation limited switching dynamics observed in fluorite structure ferroelectrics[285]. For 2D van der Waals ferroelectric insulators (e.g., $CuInP_2S_6$) and semiconductors (e.g. α-In_2Se_3), wafer scale synthesis and integration into FeFET structures must be demonstrated[286,287]. Additionally, integration into future 3D device structures will be challenging for van der Waals ferroelectrics. Lastly, good reliability of FeFETs based on van der Waals ferroelectrics has not been demonstrated so far.

3) FTJ

Since the read-out mechanism of FTJs is based on tunneling, ultrathin ferroelectrics such as fluorite structure and van der Waals materials are most promising. One of the main challenges for FTJs is to achieve a large read current while maintaining a high tunneling electroresistance (TER) ratio. For fluorite structure ferroelectric FTJs, the relatively low read current as well as limited cycling endurance and retention need to be addressed[268]. In ferroelectric/dielectric double-layer FTJs, electric breakdown of the dielectric layer with endurance cycling often limits reliability[288]. Further reducing the film thickness while still achieving a predominantly ferroelectric fluorite structure film has remained challenging due to the increase in non-ferroelectric and/or amorphous phase fractions. For FTJs based on van der Waals ferroelectrics, high temperature and endurance cycling stability must be demonstrated. So far, the relatively low Curie-temperature of many ultrathin ferroelectrics is detrimental for practical applications[276]. For neuromorphic computing, FTJs have similar challenges compared to FeFETs in terms of linearity and symmetry[285]. Variability in highly scaled FTJs could be an issue as well.

4) NCFET

As in the FeFET case, fluorite structure ferroelectrics currently are most promising for NCFET devices[289]. While improvements of EOT, subthreshold swing, on/off ratio and short channel effects have been demonstrated for fluorite structure ferroelectrics compared to regular dielectric HfO_2, achieving below 60 mV/decade subthreshold swing at room temperature has proved difficult[263]. This has been related to the large change in the semiconductor capacitance between the device on- and off-state, especially when using silicon[290]. Many reported devices show large hysteresis and operating voltages due to transient ferroelectric switching, undesirable for logic devices[291]. Such transient NC in FeFETs must be clearly distinguished from stable NCFETs without hysteresis. To further improve NCFET performance, more insight into the microscopic origin of NC in fluorite structure ferroelectrics is needed[289]. More accurate multi-domain/multi-phase models need to be developed. Additionally, further decreasing the ferroelectric layer thickness will become necessary for applications in advanced FETs with gate-all-around and stacked nanosheet structures. Therefore, ferroelectrics that cannot be grown on 3D structures by atomic layer deposition (such as van der Waals ferroelectrics) are unlikely to be used in advanced logic NCFETs.

Advances and Future Directions

The following presents a brief overview of select advances in the field, again separated by application.

1) FeRAM

To improve cycling endurance without sacrificing switchable polarization, La doping of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) has received significant attention[292]. Recently, recovery of endurance has been shown by cycling with a lower voltage while using intermittent high voltage cycling to recover the switchable polarization[293]. To reduce the switching fields of fluorite structure ferroelectrics, different methods have been proposed and demonstrated. The use of imprinted antiferroelectric films has yielded 10^{12} cycling endurance due to lower operating voltage, compatible with 3D integrated FeRAM architectures[294]. In another approach, HZO/ZrO_2 nanolaminates have been used to reduce the average switching field, resulting in improved speed, and cycling endurance[295]. This effect has been related to an increase in topological domain walls, which can lower the barrier for polarization switching[296]. Recently, HZO films with intercalated Hf/Zr atoms were reported to stabilize the rhombohedral R3m phase, resulting in a lower coercive field (~0.65 MV/cm) and improved breakdown field strength[297]. However, so far, this effect has only been demonstrated for films deposited by physical vapor deposition, which cannot be used for 3D capacitor structures. If this rhombohedral phase can be stabilized in ALD grown HZO films needs to be studied further. Furthermore, inserting different ILs between the ferroelectric and the metal electrodes has been shown to improve both the switchable polarization and the cycling endurance[298]. Such interfacial layers can also result in a change of the film texture. For wurtzite structure ferroelectrics, progress has been made in reducing the film thickness of AlScN down to 10 nm and reduced switching fields in ScGaN compositions[299,300]. Future FeRAM research should aim at further lowering the switching voltages without compromising switching speed, remanent polarization, and reliability, while also targeting further density increase through monolithic 3D integration[274].

2) FeFET

Since the IL is critical for FeFET performance and reliability, IL engineering has shown most promise for improved device behavior. For example, it has been demonstrated that ILs with higher permittivity result in improved cycling endurance, fast read-after-write, and write-disturb immunity[57,301,302]. p-type FeFETs with a SiGe channel also showed reduced read-after-write latency[281]. Furthermore, IL-free FeFETs have been fabricated using oxide semiconductor channels, resulting in excellent cycling endurance, fast read-after-write, and logic compatible write voltages[303]. Integration of fluorite structure

ferroelectrics into advanced transistor structures such as FDSOI, FinFET, and gate-all-around FET has been demonstrated[268]. Oxide semiconductor based FeFETs have been scaled down to 7 nm channel length[304]. 3D NAND-like FeFET integration has been shown[283]. Recently, interest in devices with a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure has increased, which promises higher cycling endurance and reduced charge trapping, with a trade-off in retention[305]. Fluorite structure based FeFETs have been extensively investigated as artificial synapses and neurons, for random number generation, reconfigurable transistors, as well as ternary content-addressable memories[279,285]. Semiconducting van der Waals α-In_2Se_3 has been used as a high mobility ferroelectric transistor channel, promising new FeFET device architectures with reduced depolarization fields[306]. However, more research into the switching speed, reliability and scalability of such devices is needed. Other FeFETs based on van der Waals ferroelectrics have been demonstrated, but generally suffer from lower temperature stability[276]. In terms of future trends, it seems like FeFET research is going in the direction of high permittivity ILs or even IL-free while reducing the ferroelectric thickness to lower the operating voltages. Besides silicon and SiGe based channels, oxide semiconductors as well as ferroelectric van der Waals semiconductor FeFETs seem promising for monolithic 3D integration. Fluorite structure based vertical FeFETs will become increasingly important for 3D NAND like memory architectures. Variability in highly scaled FeFETs needs to be investigated and improved further.

3) FTJ

For FTJs based on fluorite structure ferroelectrics, reducing the film thickness has been pursued to increase the FTJ on-current. Recently, FTJs with 1 nm thick HZO have been grown directly on silicon, for a read current of > 1 A cm^{-2} [307]. Read current increase has also been reported using atomic layer etching of ferroelectric HZO, resulting in more than two orders of magnitude improvement of on-current and TER[308]. Electrode work function engineering has been shown to enable improved retention as well as read-current in double layer FTJs[309,310]. Further engineering of the dielectric layer and increasing the Zr content in HZO based double layer FTJs have been shown to result in improved cycling endurance and TER[311]. Switchable ferroelectric diodes based on fluorite structure ferroelectrics have been shown to exhibit ultrahigh read currents (> 200 A cm^{-2}), good cycling endurance (10^9) in a monolithic 3D integrated structure, without the need for a selector device due to their self-rectifying behavior[312]. Fluorite structure FTJs have also been shown to be promising for applications such as artificial synapses and neurons[285]. The first demonstrations of van der Waals based FTJs showed a giant TER of up to 10^7 [313]. Future research should focus on the FTJ stack optimization to improve TER, cycling endurance and retention. Ultrathin ferroelectrics seem most promising for increased read current.

4) NCFET

Pulsed voltage experiments have demonstrated NC effects in fluorite structure ferroelectric and antiferroelectric heterostructure capacitors[314,315]. However, the origin of NC in these ~10 nm thick films is still debated[316,317]. Thinner films seem to be needed to access the NC region at lower voltages for logic devices[263]. Recently, silicon based NCFETs with an EOT smaller than the SiO_2 interfacial layer thickness have been demonstrated[19]. The stable NC in these 2 nm thick $HfO_2/ZrO_2/HfO_2$ superlattice gate stacks has been related to ferroelectric domain wall movement, which is influenced by the partially in-plane polarization and tetragonal phase fractions[318]. However, the potential role of topological domain walls in these ultrathin mixed phase films needs further investigation[296]. Both p-type and n-type NCFET devices have been demonstrated down to 90 nm gate length, with performance and reliability comparable to conventional devices with 30 nm gate length[319]. Further channel length scaling and FinFET or gate-all-around structures with similar gate stacks need to be demonstrated. Engineering of the IL or the use of other channel materials might result in even lower EOT values or

potentially below 60 mV/decade subthreshold swing. Variability in highly scaled NCFETs needs to be investigated.

Concluding remarks

Ferroelectrics are promising for future low power memory and logic devices due to their electric field control of polarization, resulting in ultra-low switching energies. The availability of scalable and CMOS compatible fluorite structure ferroelectrics enables a straightforward integration of ferroelectrics into advanced semiconductor nodes. To further reduce the operating voltage of such ferroelectric devices, the film thickness and switching fields need to be reduced. The latter could be achieved through topological domain walls, film texture control or the use of imprinted antiferroelectrics. Careful interface engineering seems to be the most promising way to overcome current reliability concerns. More research into the variability of scaled ferroelectric devices is needed. To improve the device density per area, monolithic 3D integration of ferroelectric capacitors and transistors will be crucial. Besides fluorite structure materials, wurtzite and van der Waals ferroelectrics could be promising for certain applications in low power electronics. However, more research is needed to better understand the advantages and limitations of these relatively new materials.

Computational modeling of ferroelectrics: materials, devices, and circuits

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Status and impact to date

The development and design of ferroelectric materials and devices have benefited significantly from the computational modeling at multiple spatiotemporal scales. For example, at the electronic and atomic scale, first-principles density functional theory (DFT) calculation has been used to search for new composition of ferroelectric materials with desirable properties, evaluate the relative thermodynamic stability of different polymorphs, predict the ferroelectric behaviors, including energy barrier for polarization switching[190], structure and energies of ferroelectric domain walls[320], the coupling strength between polarization and other structural/functional order parameters[235], amongst numerous other things that are predictable within the scope of thermodynamics. However, DFT calculations typically can only be performed at 0K and are limited to systems with a small number of atoms and electrons due to the high computational cost.

Complementing the DFT, Monte Carlo effective Hamiltonian simulations (purely lattice-based)[321–324] and second-principles calculations (incorporating both lattice and electronic degrees of freedom)[325–327] can directly take the DFT-calculated parameters as the input, enabling finite-temperature calculations via methods like the metropolis algorithm, and simulating systems of larger spatial scales than DFT due to the fewer number of degrees of freedom (e.g., a local soft mode related to polarization and a displacement related to strain) in each unit cell. Both the effective Hamiltonian and second-principles calculations can be effectively used to predict the stable/metastable atomic-scale polarization configuration under various external stimuli under realistic mechanical and electrical boundary conditions at finite temperature. Moreover, by using effective Hamiltonian within the Hybrid Monte Carlo (HMC) scheme, large-scale simulations of materials systems containing millions of atoms can be achieved due to the computational efficiency of HMC in parallelization (*e.g.*, via graphics processing unit, or GPU) and incorporating long-range (dipolar) interaction [328,329]. Furthermore, by implementing the effective Hamiltonian or advanced interatomic potential in the framework of Molecular Dynamics[330–333], various time-dependent phenomena (e.g., polarization switching, domain wall motion) can be modeled at the atomic scale with first-principles accuracy.

At a larger spatial scale (mesoscale), phase-field simulations[334] have been widely used to understand and predict the ferroelectric phase transition, equilibrium polarization and strain pattern and their dynamical evolution in a wide variety of ferroelectric systems. Numerous successes have been achieved over the past two decades (see recent reviews[335]). Phase-field method leverages the Landau theory of phase transition[336] and diffuse-interface theory[337] to construct symmetry-consistent thermodynamic potential for spatially inhomogeneous materials systems. It enables solving the equation of motion for multiple coupled order parameters to simulate the co-evolution of multiple coupled domain patterns (*e.g.*, ferroelectric, ferroelastic, and ferromagnetic) as well as the properties. The phase-field method is readily applicable to a broad range of ferroelectric systems ranging from single crystals to single- or multi-phase polycrystals. The use of continuum order parameters allows for a coarse graining representation of a material system, which allows simulating systems of larger spatial scales. The thermodynamic and kinetic parameters used in phase-field simulations can either be computed from first-principles calculation or obtained by fitting experiments.

Ferroelectric materials have immense potential in various innovative microelectronics devices, including ferroelectric capacitors (FeCaps), ferroelectric tunnel junctions (FTJs), ferroelectric field-effect transistors (FeFETs), and negative capacitance field-effect transistors (NCFETs). These devices find applications in diverse areas such as memory storage, logic-in-memory architectures, oscillators, and sensors. To integrate them into circuits and architectures, developing Simulation Program with Integrated Circuit Emphasis (SPICE)-compatible circuit models (also referred to as compact models) is crucial. These models aim to optimize system performance by identifying the optimal design parameters. Researchers have made significant strides in developing these models, balancing computational efficiency and physics precision, using notable models like the Preisach model of hysteresis[338], the empirical Kolmogorov–Avrami–Ishibashi (KAI) model, and nucleation-limited switching model[339]. A recent trend is the incorporation of the Landau formalism for enhanced accuracy[340]. Traditional circuit models often lack spatial dependencies, posing challenges in predicting multidomain effects. To address this limitation, the ferroelectric layer is partitioned into multiple capacitors, each governed by an independent single-domain time-dependent Landau-Ginzburg equation[341,342]. Crucially, ferroelectric circuit models must be seamlessly integrated and interconnected with other parts of the circuit models. For instance, in FeFETs and NCFETs, the ferroelectric circuit model must be considered alongside the established MOSFET circuit model, such as Berkeley Short-channel IGFET Model (BSIM) models[339]. Equating the ferroelectric-induced gate charge with that derived from existing MOSFET models allows for the effective capture of the effects of the ferroelectric layer in the gate capacitor. This includes their I-V relationships in the entire FET models. These models have greatly facilitated the design and fine-tuning of circuits with ferroelectric components, expanding the range of potential applications.

Current and future challenges

Materials Modeling Challenges

Hafnia (HfO_2) and its solutions ($Hf_{1-x}Zr_xO_2$) can display ferroelectricity when their non-equilibrium orthorhombic or rhombohedral phase can be stabilized. In contrast to archetypical ferroelectrics ABO_3 perovskites, where ferroelectricity diminishes in ultrathin film due to

depolarization, hafnia displays robust ferroelectricity even when the thickness reduces to only one unit cell[271]. In combination with its high compatibility with existing semiconductor manufacturing platform, hafnia offers an exceptionally exciting prospect for application in a wide range of ferroelectric devices and has attracted a significant amount of attention in the ferroelectrics community. Despite intense theoretical and experimental efforts[343], the fundamental understanding for the origin of the ferroelectricity, mechanisms for stabilizing the metastable ferroelectric phase, and other behaviors (*e.g.*, wake-up) that depart from conventional ABO_3 ferroelectrics are still far from complete[344]. Current status and challenges of computational modeling in addressing these science questions and guide the materials design have been discussed in Ref. [343].

Another promising system is III-nitride (N) ferroelectrics such as $Al_{1-x}Sc_xN$ [275,345–352]. Compared to $Hf_{1-x}Zr_xO_2$, wurtzite $Al_{1-x}Sc_xN$ exhibits a remanent polarization more than three times higher and a back-end-of-line (BEOL) compatible growth temperature of below 350 °C. Furthermore, $Al_{1-x}Sc_xN$ can be naturally integrated with other III-N semiconductors, enabling novel functionalities, such as enhanced sheet charge densities, in III-N heterostructures for applications like high electron mobility transistors. One key challenge facing the application of $Al_{1-x}Sc_xN$ is its large switching (coercive) voltage, which is currently exceeds CMOS compatibility. Challenging questions that computational models can help address include: What novel compositions/interfaces can lead to low switching coercive voltage? How to understand and predict the energetics and kinetics of atomic-scale and mesoscale polarization switching behaviors in such Wurtzite ferroelectrics? How to understand the wake-up behavior? How to understand the effects of point defects and strong temperature dependence[353] on the polarization switching? How to understand the influence of geometrical confinement, size, and strain in AlScN-based nanostructures (*e.g.*, nanowires, nanodots) and heterostructures (*e.g.*, superlattices, thin films)? Despite a few excellent computational works[354–356], these questions still require further clarification.

Van der Waals (vdW) layered materials is another class of promising materials that can display robust ferroelectricity in the two-dimensional (2D) limit[357]. vdW ferroelectrics can also accommodate novel polarization switching pathway and other exotic functionalities. A notable example is the sliding ferroelectricity where the out-of-plane polarization is switched by in-plane interlayer sliding, and the low switching barrier of such pathway offers the exciting prospect of realizing ultra-high-speed polarization switching with low energy cost yet maintaining robustness against thermal fluctuations[358]. Current status and challenges in computational modeling of vdW ferroelectrics have been discussed in recent review and perspective articles[358–360].

Device Modeling Challenges

A key challenge to modeling ferroelectrics-based microelectronic devices is the orders of magnitude of mismatch between the nanometer (nm)-scale heterogeneity inside the ferroelectric material (*e.g.*, domain walls) and micrometer (μm)-scale device structure. Specifically, a rule of thumb for phase-field modeling of ferroelectric materials is that the largest simulation cell size cannot exceed 1/3 of the ferroelectric domain wall width (typically 1-10 nm and down to one- or two-unit cells[361]), since at least three cells would be needed to describe a diffuse interface. When modeling polar vortices in $PbTiO_3/SrTiO_3$ superlattices[362], a simulation cell size as small as 0.4 nm is required to capture the rotation of the polarization vector unit cell by unit cell. This constraint

makes it computationally expensive or even unaffordable to simulate millimeter-scale device architecture even using mesoscale computational models such as phase-field. In addition to the spatial-scale mismatch, the mismatch in the temporal scales of multiple concurrent physical processes in ferroelectric devices would further increase the computational cost. For example, modeling devices like FeFETs is challenging due to their intrinsic multiphysics nature involving ferroelectric polarization switching, semiconductor electron transport, and electrostatics. Accurate numerical coupling schemes are essential, but current approaches lack full 3D consideration of the device structure, especially in complex designs such as FE-finFET. Therefore, there is an urgent need for an accurate and efficient 3D simulation tool capable of modeling ferroelectric-dielectric-semiconductor heterostructures across a range of computing platforms, from laptops to supercomputers. Addressing these challenges can involve harnessing the progress made in contemporary numerical algorithms. This includes the development of sophisticated algorithms aimed at maximizing the utilization of petascale and exascale supercomputing capabilities, implementing adaptive mesh refinement, and utilizing implicit time-marching algorithms. For example, a full 3D exascale model for ferroelectric-based NCFET has recently been proposed, with demonstrated almost-perfect scaling on 512 GPUs and 15X time speedup on GPUs compared to CPUs. GPU-accelerated phase-field models for ferroelectric materials and devices[363–366] have recently been developed, where hundreds of times faster computational speed-up over single CPU has been achieved. To address the complicated geometries associated with finFETs and other non-rectangular gate stacks, the finite-element method (FEM) can also be employed in the phase-field simulation[367]. Another exciting solution is the integration of advanced machine learning (ML) models to accelerate phase-field modeling[368,369] and more generally, address the computational challenges resulting from such spatiotemporal scale mismatch — which has been seen in other fields such as weather/climate modeling[370] but not yet been applied to materials science problems.

Circuit Modeling Challenges

The challenges in circuit modeling are as follows: 1. Integration with CMOS Technology IC Models: Combining ferroelectric technology with CMOS technology, typically guarded by classified parameters, requires collaboration with foundries to access CMOS circuit model cards. Researchers often start with open-source model cards, necessitating intricate curve fitting to match I-V characteristics of MOSFETs. This process is highly case-specific, influenced by device factors like geometry and fabrication technologies. The interplay between ferroelectric switching and CMOS characteristics also remains under-explored. 2. Limited Experimental Validation Data: The lack of experimental data for validating electronics characteristics, such as I-V relations, predicted by circuit models presents a significant challenge. 3. Lack of Comprehensive Multidomain Exploration: Circuit models inherently lack the capability to consider spatial derivatives, leading to a reliance on single-domain assumptions in existing models. While techniques like dividing the ferroelectric layer into individual capacitors have proven effective within certain accuracy limits, this simplification overlooks the time-evolution of domains and the dynamic changes in domain-wall energy. As the demand for high-performance circuits grows, there is a pressing need for models accommodating the complicated nature of ferroelectric devices. These models should consider multi-domain and polycrystalline characteristics, achieved by integrating simulated ferroelectric metrics from material and device modeling into the circuit model, embracing a "codesign" approach. This offers a more accurate portrayal of ferroelectric physics while maintaining computational efficiency in IC-level models and designs. These advanced models are

crucial for precise simulations of FE device performance and their intricate interplay with design parameters.

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Cold-source FET

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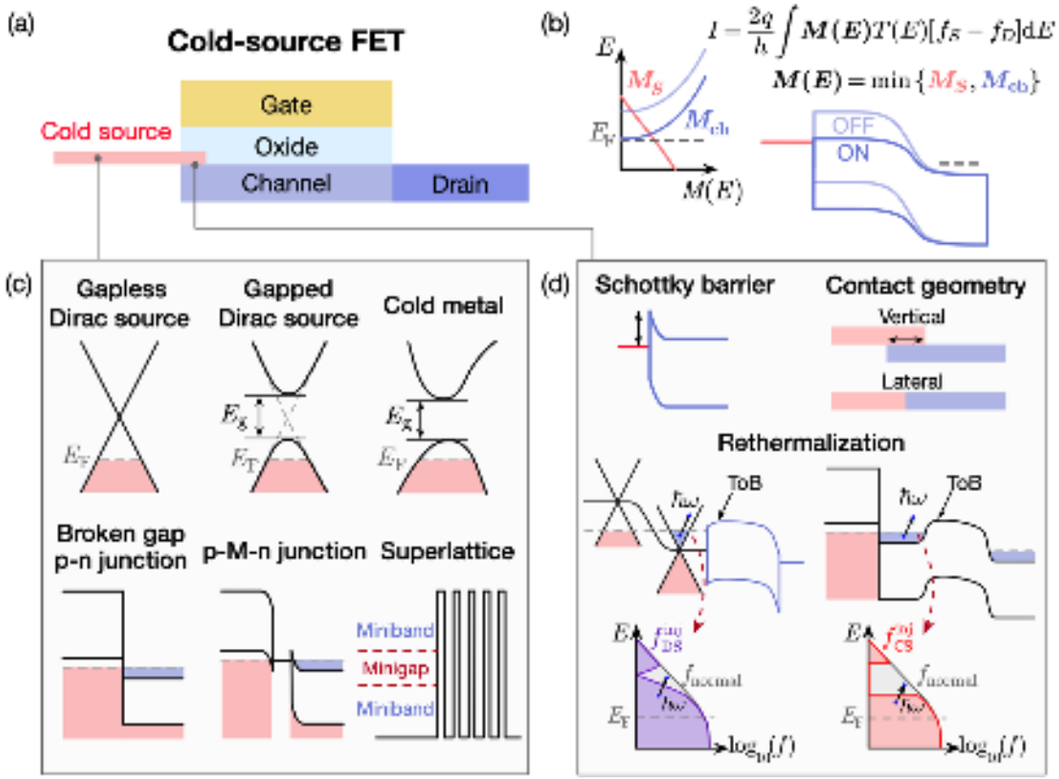

Fig. 45 (a) Device structure of a cold-source FET (CS-FET). (b) Illustration of energy filtering by number of modes in a CS-FET. (c) Different types of cold sources. (d) Challenges of CS-FET associated with cold source (CS)-channel contact interface.

1. Status of the area

Conventional MOSFETs rely on thermionic emission as the mechanism of carrier injection and the subthreshold swing (SS) is limited to 60 mV/dec at room temperature, which hinders the scaling of supply voltage V_{DD}. Therefore, steep-slope devices are highly sought after for lowering the power consumption, and in particular cold-source FET (CS-FET) has been recently proposed as a promising candidate[371]. The device structure of a CS-FET is similar to that of a MOSFET, except that the source is replaced by a cold source (Fig. 45a), in which the number of modes $M_S(E)$ decreases with higher energy E. As a result, the high-energy carriers are partially or completely cut off (depending on whether

a band gap is present) due to the energy filtering of $M_S(E)$, resulting in an effectively "colder" distribution of the carriers injected into the channel, and thus allowing to achieve a steep SS. Note that for the energy filtering of the cold source to be functional, $M_S(E)$ should also be smaller than $M_{ch}(E)$, the number of modes in the channel, within the energy range of interest that contributes to most of the off-state current (Fig. 45b). Compared with tunneling field-effect transistors (TFETs)[372], which also relies on energy filtering to achieve a steep SS, a major difference to the CS-FET is that the energy filtering in the cold source is independent of the gate control of the potential barrier in the channel, thus resolving a common issue in TFETs, i.e. the energy filtering effect (and thus SS) continuously deteriorating due to a widened tunneling window close to the on-state of the device.

An early pioneer of the CS-FET concept can be dated back to a paper in 2011[373], in which a broken-gap p-n junction was proposed to be used as a band-pass energy filter. In 2018, Qiu et al.[371] proposed the Dirac-source FET (DS-FET), a variant of the CS-FET in which the Dirac cone of graphene is used as a low-pass energy filter (and thus named Dirac source). In this paper, the device concept was experimentally demonstrated in a carbon nanotube (CNT) system and a steep SS of 35 mV/dec was achieved (although the detailed mechanism of the steep slope in the experimental device is a subject of debate[374]). In an IEDM paper[375] in the same year, the device concept of DS-FET was extended to include other types of cold sources and the term "cold-source FET" was coined. Multiple cold sources have been explored theoretically up to date, including gapless/gapped Dirac source[371,375,376], cold metals[377–379], broken-gap p-n junctions[373], p-doped-semiconductor-Metal-n-doped-semiconductor (p-M-n) junctions[375] (however, the scattering in the metal may result in re-thermalization of the carriers as discussed in ref.[380]) and superlattice[381,382] (Fig. 45c). On the experimental side, only DS-FETs based on a gapless graphene Dirac source have been demonstrated, including p-type[371] and n-type[383] CNT DS-FETs and n-type MoS_2 DS-FETs[384,385] (although re-thermalization is an alarming issue in these MoS_2 DS-FETs as will be discussed in the next section).

2. Current and future challenges

As Herbert Kroemer puts it – "the interface is the device" – most of the challenges faced by CS-FETs are associated with the interface between the cold source (CS) and the channel, as illustrated in Fig. 45d. One major challenge is the Schottky barrier at the CS-channel interface. As shown in ref.[376], a large Schottky barrier height not only lowers the on-current, but also deteriorates the SS, since carriers with higher energies have higher transmission than those with lower energies, which results in an increase in the temperature of the injected carriers. Therefore, it is critical to have a low (ideally, zero or even negative) Schottky barrier height between the cold source (CS) and the channel to achieve a high on-current and a steep SS.

Another major challenge is the re-thermalization of injected cold carriers. For instance, a typical n-type DS-FET or CS-FET has an n-doped extended source region at the CS-channel interface to lower the Schottky barrier height (Fig. 45d). In this n-doped region, however, any inelastic scattering before reaching the top-of-the-barrier (ToB) in the channel, such as optical phonon scattering, would lead to re-thermalization of the injected carriers from a cold distribution f^{inj} towards the room-temperature Fermi-Dirac distribution f_{normal} (as illustrated in Fig. 45d), which, in the worst-case scenario, results in a deterioration of SS back to 60 mV/dec. Most of the early theoretical and simulation works on CS-FET focus on ballistic transport and ignore the impact of scattering[375,386], while two recent simulation studies that take electron-phonon scattering into account show that carriers are completely re-thermalized over a length scale of a few nanometers after being injected from the cold source into a WS_2 [387] or Si[388] doped extended source region, before reaching the ToB in the channel region. Note

that since the CS-channel overlap belongs to the region of concern for re-thermalization, the overlap length needs to be scaled to much shorter than the mean free path of optical phonon scattering to avoid re-thermalization. In this regard, it is surprising that previously demonstrated steep-slope MoS_2 DS-FETs[384,385] were built with a long graphene-MoS_2 overlap lengths (5~10 μm), since the phonon-limited mean free path in MoS_2 is typically less than 10 nm[389].

3. Advances in science and engineering to meet these challenges

To reduce the Schottky barrier height, for CS-FETs utilizing graphene as cold injector, it is possible to n-dope the graphene due to its small density of states (DOS) in the CS-channel contact region to lower the Schottky barrier height[371,376]. At the same time, the p-doped graphene Dirac source provides the required energy filtering, and the high transmission of Klein tunneling in the graphene p-n junction ensures a large on-current of the device[371]. However, the n-doped graphene segment (as well as the overlapped channel region) is subject to re-thermalization, and therefore its length needs to be aggressively scaled. For CS materials with large DOS, such as cold metals, tuning band alignment by doping the contact region may not be an option, and it is therefore critical to identify CS-channel material combinations that can give rise to small Schottky barrier heights through ab-initio simulation and experimental verification.

To suppress re-thermalization, it is critical, as stated above, to reduce the overlap length in the vertical contact geometry, for instance, by developing a self-aligned process with ~nm accuracy that is beyond any lithographical approach to pattern and align the CS and the channel. Alternatively, the requirement on overlap length can be relaxed by using high-mobility channel materials that have a long mean free path of optical phonon scattering. As an example, a simulation study[378] predicts that Au_2S with a large phonon-limited mobility of 8.45×10^4 $cm^2/(V\cdot s)$ is a suitable channel material for CS-FETs, and device simulations show that steep SS is achieved for devices with an overlap length up to ~50 nm. In addition, another feasible option is to adopt a lateral contact geometry in the CS-FET (Fig. 45d), for instance, via chemical vapor deposition (CVD) synthesis of in-plane 2D heterojunctions[390,391].

To resolve the aforementioned challenges, efforts should also be made on simulation to evaluate different options and provide guidance for experiment. It is crucial to develop multi-physics simulation frameworks that meet the following requirements: (a) accurate prediction of electron and phonon band structures of cold source and channel, as well as band alignment between the two; (b) incorporation of electron-phonon scattering in the device transport simulation to include re-thermalization effect; (c) capability to simulate device structures and dimensions that are realistic and can be made experimentally; (d) incorporation of nonideal effects, such as interface defects, gap states and fringing fields.

In addition, existing experimental demonstrations of CS-FETs are limited to DS-FETs with a gapless graphene Dirac source. Other types of cold sources, such as 2D cold metals (NbX_2 and TaX_2, X = S, Se, Te)[377] and 3D cold metals ($Cu(IrS_2)_2$, $Cu(RhS_2)_2$, $Cu_5Si_2S_7$, La_2MgIrO_6, La_2MgRhO_6, and $Bi_3Pt_3O_{11}$)[379], have been predicted by ab-initio simulation, but more experimental work is needed to confirm those predictions. A more attainable and practical target in the near future is gapped bilayer graphene by electrical gating[392], which could be explored to achieve an even steeper SS[376,386].

4. Concluding remarks

Despite the above challenges, CS-FET holds great promises for steep-slope transistors and low-power electronics. To achieve its full potential, however, requires both experimentalists (material scientists and device engineers) as well as theorists (experts on ab-initio simulation of materials and quantum transport of devices) to work more closely to further investigate the device concept and identify and resolve the challenges.

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Computing with p-bits

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Between a bit and a qubit: A computing paradigm that is attracting attention[393] is based on the concept of ***probabilistic or p-bits***[394] which can be viewed as intermediate between the deterministic bits of digital computing and the qubits of quantum computing. A bit has two values, 0 and 1 while a qubit is a delicate superposition of 0 and 1. A p-bit lies in between: it is a robust classical entity that fluctuates between 0 and 1.

The state of a system of n bits is described by an n-bit binary number like 1001….110. By contrast, a system of n qubits is described by a wavefunction with 2^n complex components whose squared magnitude gives the probabilities of the 2^n possible configurations. A system of n p-bits too requires an exponentially large number (2^n) of components, but they are all positive numbers that constitute the probability density function. Feynman noted that "*… the only difference between a probabilistic classical world and the equations of the quantum world is that the probabilities would have to go* ***negative***" [395]. The power of quantum computing comes from exploiting these negative (more generally complex) probabilities, which in turn requires stringent experimental conditions to protect the phase.

Probabilistic computers are much more robust and have been demonstrated to operate at room temperature using existing technology. They lack the magic of complex probabilities but can function as hardware accelerators for stochastic a.k.a Monte Carlo (MC) algorithms which have been recognized as one of the top ten algorithms of the 20th century[396] with applications in a wide variety of fields such as optimization, inference, quantum emulation and machine learning[397].

Device innovation: The key element in this paradigm is a device whose output s takes on one of two values, 0 and 1, with probabilities p and $(1-p)$ respectively where p lies between 0 and 1 and is controlled by the input voltage v which can be an analog or perhaps a multi-bit digital quantity. Devices like this can be built with existing CMOS technology, but they require ***tens of thousands of transistors*** per p-bit.

By contrast it has been shown that by modifying standard MRAM technology special nanodevices can be constructed which require only ***three transistors and an unstable magnetic tunnel junction (MTJ)***[398] to perform the functions associated with a p-bit, namely a random number generator

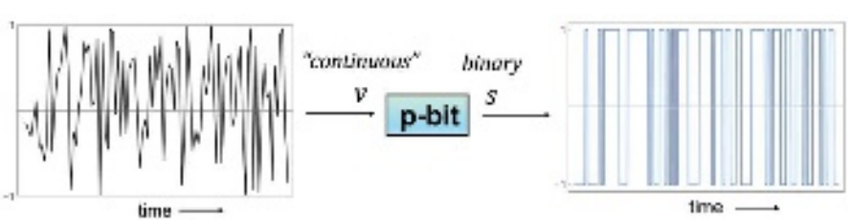

Figure 46: A p- bit takes an input voltage v whose value determines the probability p that its binary output is 1.

(RNG) coupled with a lookup table and comparator that are used to control the probability p. These novel devices have been used to demonstrate small networks with tens of p-bits performing optimization[399] and learning[400]. Other compact implementations may also be possible and could be attractive especially if they can be built with existing technology, unlike the unstable MTJ which requires a modification, albeit small, of MRAM technology.

So far, however, demonstrations of large networks with thousands of p-bits have been based on CMOS implementations with tens of thousands of transistors[401–403]. Even so they have been shown to provide performance that is orders of magnitude better than CPU implementations and comparable to that obtained from standard GPU/TPU-based hardware accelerators[404–406]. Existing CMOS technology only allows us to integrate ten to twenty thousand p-bits, but the use of compact energy-efficient p-bits would enable us to integrate millions of them operating at nanosecond rates[407,408], providing 10^{15} probabilistic flips per second[401]. However, this alone is not enough to achieve increased performance. To see why, we need to consider the algorithm and architecture that can be implemented with p-bits (Figure 47).

Algorithms and architecture: An array of p-bits like the one shown in Figure 47 constitutes a controlled random number generator (RNG) which is a key component in the implementation of any MC algorithm. However, even the simplest algorithms also require an arithmetic function f to be implemented on the output. In the language of neural networks, one could call these binary stochastic neurons and synapses. Together they form a building block that can be used to implement more complex MC algorithms.

For example, Markov Chain Monte Carlo (MCMC) algorithms involve a random walk where each subsequent step depends on the current state and can be implemented with a series of concatenated building blocks (Figure 47) as in deep belief networks (DBN). On the other hand, a restricted Boltzmann machine (RBM) can be implemented using two of the building blocks and feeding the output of the second unit back to the input of the first unit.

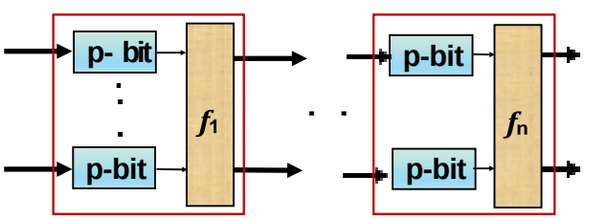

Figure 47: The basic building block for a hardware implementation of an MC algorithm includes an array of p-bits whose output $\{s\}$ is processed to compute a function $f(\{s\})$ which is dictated by the specific algorithm being implemented. Multiple building blocks can be concatenated perhaps with feedback to solve diverse classes of problems.

Looking at the building block in Figure 47 it is evident why an array of compact p-bits providing a large throughput of random numbers is not enough to produce a large number of samples per second. The unit for computing the function f appears in series and can easily create a bottleneck. Sophisticated algorithms often require the computation of elaborate functions f that cannot utilize the large flux of random bits. For this reason, a limited number of RNGs are often time-shared since there is little incentive to provide a dedicated RNG for each thread. For example, in synchronous systems where p-bits are updated in sequential blocks[409], the same RNG units could be shared since they are not accessed at the same time. These tricks allow the scaling of digital p-bit systems, eventually however, natural

analog noise of nanodevices, for example encountered in magnetic tunnel junctions with low-energy barriers will lead to the ultimate scaling of p-bit systems.

The essence of a p-computer, however, lies in the use of large numbers of compact energy-efficient RNGs in parallel followed by an efficient scheme for the computation of the function f that can keep up with it. Our experience suggests that even when everything is implemented with digital components, the performance (samples/ns) can be orders of magnitude better than CPUs, and comparable to optimized GPU/TPUs. Significant improvement beyond this can be achieved if novel mixed signal and/or asynchronous approaches are incorporated into the computation of f along with a tailoring of f through a choice of algorithms. These approaches should also enable orders of magnitude improvement in energy efficiency by reducing the energy needed to generate correlated random numbers.

A toy example: Figure 48 shows a toy example of a two p-bit network where two p-bits are recurrently connected.

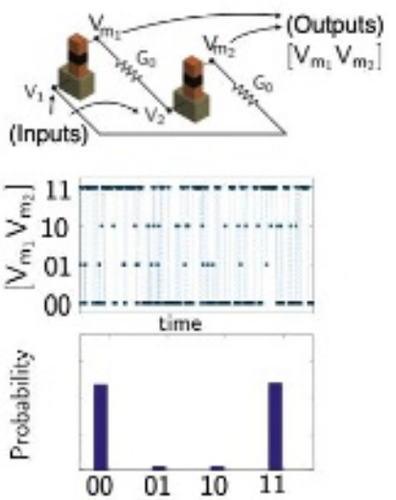

Figure 48: A simple two p-bit network where the conductances, G_0 play the role of f and in a two p-bit network. This model assumes the p-bits have "current" inputs that are obtained from a "voltage" output going through conductances, G_0. The selection of conductances selects the 00 and 11 states to be emphasized by the network.

In this network, the role of f is played by the conductance between the p-bits that take the output of a p-bit and turn it into a current proportional to the p-bit state. Assuming the outputs take positive and negative voltage values represented by logic 1 and 0 respectively, we observe that the p-bits as a system will emphasize agreement (00 and 11 states), much like spins in a ferromagnet that are interacting with a positive exchange interaction. Unlike natural magnets, the interactions can be engineered in p-bit networks to represent much more complicated problems that are mapped to combinatorial optimization and machine learning tasks.

One important consideration in optimizing the calculation of f and parallel RNGs is the ***sparsity in the network architecture***. Similar to digital VLSI circuits where fan-in is restricted, limiting the number of neighbors in p-bit networks leads to a high degree of sparsity. This allows distributing and parallelizing the f computation without having to slow down the parallel operation of p-bits[403]. Such sparse and asynchronous networks bear a strong resemblance to the statistical physics of classically interacting particles, where interactions are local, asynchronous (without a global clock), and massively parallel[410]. The design and implementation of future asynchronous p-computers may benefit from these physics-inspired concepts, akin to the ideas explored in the related field of thermodynamic computing[411,412].

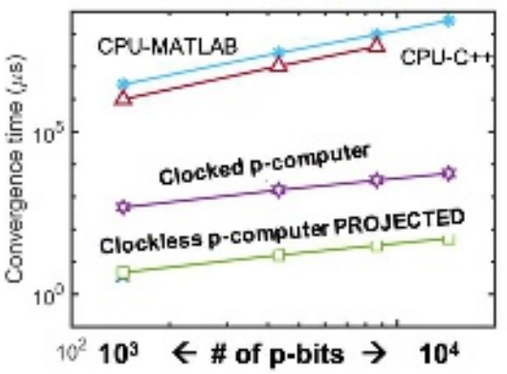

Figure 49: Adapted from Ref.[413]. Time is required to converge to an acceptable solution as a function of the size of the problem. The improvement from "GC-C++" to "clocked p-computer" comes from parallelism, while the improvement from "clocked p-computer" to "clockless p-computer" comes from asynchronous operation using resistor networks to implement the functional computation.

An example: Let us end with a concrete example illustrating the choice of algorithms and architecture that can make use of a large throughput of random numbers. We note, however, that this work is still in its infancy and much remains to be done. Figure 49 shows a figure adapted from a recent paper[413] addressing a quantum problem[414] which is first mapped onto a system of N p-bits using standard methods from the field of quantum Monte Carlo. The problem then becomes a generic one involving the generation of n-bit binary samples with probability $P \propto \exp(-E)$, E being the energy or cost function associated with each of the 2^n possibilities.

What makes this problem relatively simple is that the evaluation of the function E involves a small number of p-bit pairs and this makes the corresponding function f relatively simple, making it easier to keep up with ultrafast RNGs. But this example provides a blueprint for what it takes to design a p-computer that can truly enhance the performance. The first metric is the time rate of random bit generation given by the number of p-bits (n) multiplied by their fluctuation rate ($1/\tau$). A million p-bits fluctuating every nanosecond can provide $n/\tau = 10^{15}$ flips per second far in excess of the state-of-the-art which stands at $\approx 1 - 10 \times 10^{12}$ flips per second (see Table I in [401] and [404-406] for GPU/TPU benchmarks). But to take advantage of the petaflips per second enabled by compact efficient p-bits it is essential to integrate it with efficient schemes for the f-computation, by taking advantage of mixed signal and/or clockless operation. Figure 49 is based on a specific problem, but it illustrates a general paradigm that can be extended to other problems as well based on parallelism, pipelining and clockless operation. Just like quantum circuits, general and scalable probabilistic circuits of the type we discuss in Figure 47 could be useful for a wide range of applications including quantum simulation[414], approximate combinatorial optimization[409], machine learning and AI.

New Structures and Materials for Spintronics Computing

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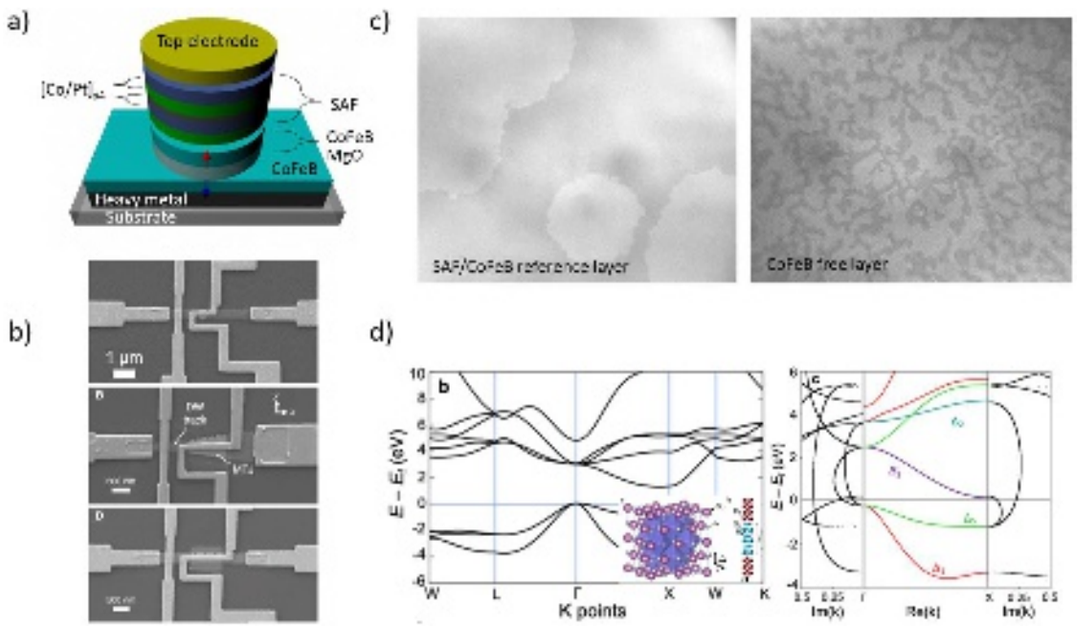

Figure 50. (a) Stack structure of perpendicular MTJ with bottom Ta/CoFeB(free)/MgO/CoFeB(pin) layers continued to synthetic antiferromagnet (SAF, $[Co/Pt]_{\times n}/Ru/[Co/Pt]_{\times n}$) layers for top pinning and capping layer with top electrode (TE). (b) Three different shaped DW-MTJ devices: general rectangular shaped MTJ on DW track, notched rectangular MTJ on DW track, and notched trapezoidal shaped DW-MTJ device[101,415]. (c) Kerr microscope shows a circular domain expansion in the MTJ film that is etched up to CoFeB(pinned)/MgO layer by ion-milling technique. The bottom MgO/CoFeB (free) layer shows stripe domains formation that can be utilized to create skyrmion bubbles. (d) Scandium nitride (ScN) is being explored as an alternative tunnel barrier material for the MTJ: here the ScN band structure is plotted with 4.5 eV Hibbard potential added to the 3d orbital of Sc[416].

I. Status of Domain Wall Structures in MTJs

Both MTJ and DW device operation are well explained with spin dynamics and corresponding micromagnetic simulations based on the Landau-Lifshitz-Gilbert (LLG) equation. Spin torques such as spin transfer torque (STT) and spin orbit torque (SOT) are fundamental methods to induce magnetization switching of the ferromagnet (FM) or DW motion by applying current or voltage. For the prototype devices, the performance of magnetic random access memory (MRAM) and racetrack memory (RM) are strongly related to the device structure and magnetic material properties[417,418].

The magnetic tunnel junction (MTJ), as well as MRAM, are quantified by device properties such as the tunnel magneto-resistance (TMR) and resistance area (RA) product, which can be improved by insertion/replacement of layers in the thin film stack structures shown in Fig. 50(a)[419,420]. STT/SOT-MTJ devices that switch their magnetization based on current pulses have been successfully developed to create deterministic resistive bits with rapid resistance switching between parallel (P) and anti-parallel (AP) magnetic energy states corresponding to the magnetization relation between the MTJ free (FL) and pinned layers (PL)[421]. The MTJ deterministic resistive switching has been widely demonstrated in the applications of non-volatile random access memory, logic devices, and unconventional computing, and has benefits such as energy-efficient sub-nanosecond/nanosecond speed operation, scalability, thermal stability, high endurance, and compatibility with CMOS[422–426].

Magnetic spin textures such as magnetic domain walls (DWs) and skyrmions can be used to increase the functionality and dynamical response of magnetic spintronics devices. Domain wall (DW) racetrack memory has also been introduced over the past ten years[430]. The DW motion between two domains is classically used to create a bit by deflation and expansion of domains in the ferromagnetic and synthetic antiferromagnetic nanowires[431,432]. The DW motion is well characterized and explained in terms of DWs types relevant to the DW shape and energy due to magnetic material properties[433,434], such as the magnetic anisotropy energy, exchange coupling, and Dzyaloshinskii Moriya interaction (DMI). For example, a transverse domain wall (TWD) is introduced in in-plane magnetic anisotropy (IMA), and Bloch/Neel DWs in perpendicular magnetic anisotropy (PMA) films and nano-patterned ferromagnetic wires[435–437]. Magnetic skyrmion bubbles in PMA heterostructures have been studied, especially created and controlled by current pulses and ultrafast lasers[438,439]. However, the DW and skyrmion bubbles dynamics are still under investigation, especially in the case of extremely narrow nano-scale dimensions in scaled spintronic devices[440,441]. For example, interfacial DMI can modulate DW formation and the skyrmion Hall effect determines the trajectory of movement of skyrmion bubbles[442,443]. In spite of this room for further understanding, the DW is one of the promising components for spintronic applications for in-memory and neuromorphic computing, because of the controllable dynamics, high speed, and low energy consumption.

II. Challenges and Opportunity for New Materials

The conventional MTJ operates deterministically, associated with robust magnetization states, 0 and 1, of PMA/IMA nanomagnets and single magnetic domain reversal. On the other hand, p-bit computing utilizes non-deterministic switching such as incomplete switching or random telegraph noise (RTN). Thus, probabilistic computing can leverage non-deterministic MTJ switching. Recently, MTJ cells have been applied to realize random number generators and non-linear output generators for probabilistic computing (e.g., p-bits), with advantages of low energy consumption and sampling rate in the nano-second scale[399,427]. These new applications of MTJs and MRAM are paving the way toward future electronics in machine learning and neuromorphic computing[428,429].

The MTJ-based probabilistic computing bit (p-bit) has two essential characteristics: 1) random output generation between 0 and 1, and 2) output distribution that follows a non-linear, sigmoidal curve in response to the input[400,429]. The p-bit computation approach requires a vast number of independent sources or random probability distribution signals for machine learning algorithms[444]. Commercially available and emergent MTJ devices are suitable for the optimization of high-dimensional algorithms of machine learning or sampling problems due to their low-power operation at room temperature and high density of random noise source hardware[101,445].

Interestingly, the combination of DWs and MTJs (in the DW-MTJ device) provides unique functionalities to apply to neuromorphic and probabilistic computing. Nucleation and control of the

DW are fundamental for these applications. While DW motion can be electrically detected via anomalous Hall effect (AHE) measurement, the Hall resistance switching due to DW motion is currently too small[415], hence a MTJ readout is required. Conventionally, the MTJ free layer consists of a ferromagnetic CoFeB layer with an adjacent heavy metal. Therefore, the free layer of the MTJ can be utilized as the DW nano-track. The pinned reference layer of the MTJ is also commonly comprised of a CoFeB layer with a synthetic antiferromagnet (SAF, Co/Pt multi-layer with spacer) layer as shown in Fig. 50(a). These two CoFeB layers can host different types of DWs and domains in the DW-MTJ, which could eventually both be utilized. For example, Fig 50(b) shows two different patterns of the domains creation in the DW-MTJ stack. The stripe domains in the free layer of the MTJ indicate that it can nucleate or create both DWs and skyrmion bubbles. Fig.50(c) shows DW-MTJs of various shapes, which can be used to tune the device for application-specific functions[446,447].

The sensitivity of MTJs to the need of 1-2 nm-thin barriers has been a major bottleneck for industrial implementation of MTJ devices. Magnesium oxide (MgO) is a wide bandgap (7.8 eV) insulator that limits its thickness to 1-2 nm for a reasonable resistance-area (RA) value for MTJ devices. MgO is challenging to grow 1-2 nm while being pinhole-free. Besides, required high annealing temperatures result in the degradation of the interface and diffusion from the MgO causing oxidation of the ferromagnetic electrodes[426,448]. Scandium nitride (ScN) is a potential material of choice as a tunnel barrier due to its narrower bandgap (~2-2.9 eV) shown in Fig.50(d), similar rock salt crystal structure of MgO, and the diffusion of nitrogen is not crucial while annealing. Spin dependent tunneling calculations of ScN junctions showed transmission via Δ_1 and Δ_2' symmetry waves and a high MR response competitive to MgO junctions. Therefore, ScN is an exciting new material for MTJ device since it can be used as a thicker tunnel barrier while maintaining a high MR ratio with low RA product in a field where few alternative materials to MgO have been developed[416].

Additionally, multiple steps of thin film growth, characterization, and device fabrication processes are used to fabricate the DW-MTJ device. While it can currently be patterned in the few tens of nanometer scale, improved nanofabrication processing is needed for selective etching in the Angstrom scale while preventing damage to the nanometer thick FL DW track. Improvements in the passivation layer are also needed to prevent of leakage current through MTJ the sidewalls.

Various emerging spintronics devices are being developed for next-generation non-volatile storage, logic, in-memory computing, and neuromorphic computing. The combinations of magnetic nanomaterials and their novel properties, such as spin dynamics in ferromagnetic and antiferromagnetic layers, are encouraging[449]. Specially, MTJs and DW-MTJs can provide robust huge random sampling in nano/micro-seconds timescale, useful for applications in security and probabilistic computing.

Process and integration challenges for low power electronics

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Abstract

The quest for novel functional materials is combined with innovative deposition and patterning approaches to pave the way for industry adoption of disruptive low power electronic devices and circuits. Apart from demonstrating device operation and performance, the fabrication of demonstrator devices is essential to explore the viability of integration processes in an industry relevant environment. Metrology and patterning solutions become an essential part in the characterization and monitoring of process impact. Scalability is defined by the maturity level reached for material deposition up to access to advanced fab integration flows. By addressing four different case studies, different technology challenges are reviewed and highlight significant steps forward, and open challenges to be handled moving away from lab-scale research to fab-scale manufacturing.

1. Introduction

For many decades, progress in the semiconductor industry has been achieved by miniaturization of semiconductor devices. However, for over two decades, the lithography driven miniaturization has been complemented by the introduction of novel device architectures in parallel with novel materials and processes. Examples of novel materials and processes are high-k dielectrics and metal gates[450] or Cu damascene interconnects[451]. It can be anticipated that this will only accelerate in the future, requiring further advancements in process innovation not only for material growth, but also for etching, planarization, and cleaning techniques. Disruptive concepts such as ultralow power devices and circuits strongly rely on novel functional materials and require, as a consequence, also novel processes for deposition or patterning. In some cases, the required materials and processes can also be considered as disruptive since they strongly deviate from current CMOS manufacturing, leading to considerable challenges for process integration and development. Attempts to use Ge and III-V compound semiconductors in CMOS logic circuits[452] were hindered by the lack of suitable gate dielectrics and contacts and processes to obtain them, despite the widespread use of III-V materials in optoelectronics.

A major challenge for advanced semiconductor devices is the increasing complexity of the novel functional materials. Below, we present some examples for different future technology options, including, *e.g.*, complex oxides, 2D semiconductors, or topological insulators. Complexities of these compound materials include not only the natural control of the stoichiometry but also the crystalline phase, order (or disorder). Moreover, properties of these materials can be anisotropic, so the orientation of single crystal or the texture of polycrystalline films need to be considered. Also, functional films become increasingly thin in scaled devices, leading to an overall device behavior determined by interfaces rather than the thin film properties themselves. These aspects are often interdependent, can reduce process windows, and greatly increase complexities for process development and integration.

They can be frequently considered to be roadblocks for the adoption of disruptive technologies in commercial applications.

Besides process integration and development, important challenges exist also for materials characterization and process metrology. The characterization of order and disorder in ultrathin films of compound materials with high accuracy remains an open issue. In many cases, the sensitivity of established techniques, for example to detect misoriented crystalline grains in cases where film texture is critical, needs to be improved to assess defectivity. Hence, characterization and metrology research and development need to go hand in hand with process development to successfully bring advanced ultralow power logic technologies from lab-scale research into fab-scale manufacturing. Below, we introduce materials and process challenges for four specific examples with increasing degree of disruptiveness, as depicted in Fig. 51. Representative transmission electron micrographs of sample devices are shown in Fig. 52. The described process challenges are meant both to emphasizes the known or expected key process challenges of the given device concepts while also serving as a broad reflection on challenges associated with introducing new materials or designs into advanced flows. These considerations are often not thoroughly addressed at the fundamental concept level.

2. Spin-torque majority gate

At a low entry point are spin-based approaches taking a direct benefit from achievements in MRAM technology. The implementation of dedicated developments provides for the non-conventional device geometry and high requirements regarding process and interface control. Significantly different is the device architecture for logic applications compared to their use in memory technologies. Single magnetic tunnel junctions (MTJ) are used in MRAM for memory units. Spin Torque Majority Gates (STMG) rely on the tunnel magneto resistance (TMR) for readout and Spin Transfer Torque (STT) for writing, like STT-MRAM. Fast domain wall (DW) motion is crucial for information transport between the different MTJ pillars. In the work of Raymenants *et al*[453]. the integration viability has been demonstrated by careful selection of the functional materials allowing for optimal performance and their resilience towards etch conditions employed in the pillar patterning.

A very strong requirement of the STMG device concept as shown in Figure 51(1) is to enable a nm-precise etch stopping on the MgO barrier, which leads to ultra-narrow process margins when considering non-element selective ion beam etch techniques (standard method for MRAM). In absence of such a process, the alternative was to design a free layer that would be more robust against potential etch damage. The common MRAM MTJs composed of CoFeB/MgO-based free layer (FL) are replaced using the hybrid free layer concepts to enable the integration of high DW velocity materials like Pt/Co/Ru/Co forming the synthetic antiferromagnetic (SAF), as shown in Fig. 51(2). The thicker magnetic conduit enables the first magnetic layer (CoFeB) to become sacrificial. Access to state-of-the-art physical vapor deposition (PVD) tools, allows for excellent process control to ensure deposition control to the Angstrom level. Additionally, the composition of the stack is tuned to preserve the magnetic conduit from deterioration induced by the ion beam etch (IBE) process. This is combined with the optimization of the IBE conditions itself, allowing soft landing on the free layer and preserving the integrity of the pillar side wall. Moreover, applicability at scaled dimensions and complex device architectures (*e.g.,* cross bar geometry) is demonstrated. These findings pave the way towards

scalability of other majority gates concepts like spin-wave majority gates[454] (SWMG) and magnetoelectric–spin-orbit majority Gates[11,250] (MESO).

Many process steps and methods have been developed starting from MRAM technology. However, selective chemical etching of key junction materials (CoFeB, MgO, ...) would be needed to improve process windows and overall interface quality. The no-selectivity of Ion beam etching implies in fact a very narrow, close to impossible (sub-nm) process window. While developing element selective etches for all the elements present in the MRAM stack may not be practically feasible, finding a chemical etch method enabling selective removal of CoFe while preserving CoFeB will be at least needed to enable a workable process window for manufacturing. Metrologies enabling a good diagnostic of nanoscale magnetic domain wall track still need to evolve from R&D lab-based research to fab operation.

3. Magnetoelectric logic

The domain wall based logic approaches described in the previous section employ spin transfer torque magnetic tunnel junctions (MTJs) as transducers for information writing and reading in the magnetic domain. Technology benchmarking has found that the energy dissipated in MTJ derived transducers significantly contributes to the energy dissipation of the entire circuit[455]. To achieve ultralow power operation, the transducer efficiency must be reduced. For this purpose, magnetoelectric transducers have been proposed that operate based on voltages (rather than currents), as discussed in detail above, both as the input stage in MESO logic gates[6] as well as transducers spin waves majority logic[80].

Two magnetoelectric approaches have been pursued in the recent past, based on multiferroics[250,456] as well as on magnetoelectric compounds consisting of piezoelectric and magnetostrictive components[457,458]. Although other materials have been examined in the past, the most promising multiferroic and piezoelectric materials are complex oxides, typically perovskites. Examples are the multiferroic $BiFeO_3$ or piezoelectric solid solutions of $Ba(Zr_{0.2}Ti_{0.8})O_3$ and $(Ba_{0.7}Ca_{0.3})TiO_3$ (BCZT). The material choice for piezoelectrics is complicated by the issue that oxides with large piezoelectric response often contain Pb (*e.g.*, $Pb[Zr_xTi_{1-x}]O_3$, PZT, or $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ solid solutions, PMNPT), which needs to be avoided in consumer products due to environmental and toxicity reasons[459,460]. By contrast, many magnetostrictive metals are based on lanthanoid and transition metals (*e.g.*, Galfenol, $Fe_{0.8}Ga_{0.2}$, or Terfenol-D, $(Dy,Tb)Fe_2$)[461], although also complex oxide ferrites (*e.g.*, $CoFe_2O_3$) have been studied[462].

Thin films of (multiferroic) complex oxides have been typically deposited by pulsed laser deposition (PLD)[87,463] on a lab scale due to excellent stoichiometric control. While PLD is being introduced in MEMS manufacturing[464], integration into a logic circuit processing flow still requires many obstacles to be overcome. A key challenge may also be the required deposition temperatures for high quality complex oxide thin films, which typically exceed the thermal budget of back-end of line processing (typically 420°C). Hence, coprocessing with conventional charge based circuits, which are needed for interfacing with the electronic system[80], needs to be carefully considered. The control of the oxygen content is a key requirement since it typically strongly affects leakage currents and limits thickness scalability of complex oxide films[87].

The integration of functional complex oxide films in logic circuits thus necessitates establishing manufacturable deposition techniques with excellent cation stoichiometry, oxygen content, and phase control characteristics at low temperatures. In addition, etching or cleaning processes are not yet well established for such materials. Hence, significant process challenges remain to integrate complex

oxides as functional materials in scaled logic or memory devices and circuits. By contrast, the deposition and the patterning of magnetostrictive metals is compatible with established MRAM manufacturing processes. In addition to unit step processes, the thin film characterization and metrology of order, polarization, and magnetoelectric coupling at the nanoscale and at high frequencies should be considered as an open challenge.

We finally remark that for devices based on magnetoelectric compounds that used mechanical degrees of freedom to couple electric fields to magnetization (dynamics), the mechanical design of the devices is also today only in its infancy. To optimize the stress and strain transfer from piezoelectric to magnetostrictive components (and *vice versa*), the mechanical properties of surrounding layers (*e.g.*, insulating dielectrics or metal electrodes) become critical[465]. Therefore, it can be envisaged that novel dielectrics or metals with tailored mechanical properties (*e.g.*, Young's modulus) need to be researched to avoid (or sometimes introduce) mechanical clamping in the structure, which can lead to a strong reduction of the magnetoelectric coupling. While well-established materials may often be acceptable (SiN_x, SiCOH low-k dielectrics, ...), this topic may require more attention in the future to achieve manufacturable magnetoelectric devices. Here, insights from MEMS/NEMS design and processing may become useful.

4. Transistors based on 2D semiconductors

Even more disruptive is the implementation of van der Waals materials into emerging technologies. Conveniently, these layered materials can be fabricated to cover a broad range of properties, ranging from metallic, semi-metallic, semi-conductor, insulator, and dielectric, depending on the elemental composition. Their intrinsically atomically thin nature allows them to be easily integrated at various locations in the device, like active components, functionality boosters or simply as thin liners or barriers[466,467]. Graphene and hexagonal boron nitride (hBN) are well known examples of materials that require CVD-like processes deposited on metal surfaces or templates. Commercially available materials are typically grown on Cu or Ni foils and transferred via wet chemical methods making them accessible for back end of Line (BEOL) integration flows. Surface roughness and layer control, both for inter layer rotation and uniformity over the number of deposited layers, are key parameters directly impacting performance[468,469], and impact variability[470,471]. Transition metal dichalcogenides (MX_2) consisting of a transition metal (M = Mo, W, Pt, ...) and chalcogenide atoms (X = S, Se, Te), are enriching the family of materials of choice. Focusing on semiconducting materials[472], these high mobility channels have the potential to continue scaling in a beyond Si era[473] or find a niche application in BEOL transistors.

MoS_2 is the material with the best understanding of the role of nucleation density, growth kinetics, and second island growth, on crystallinity, grain boundaries effects and defectivity level. Most applied techniques are chemical vapor deposition (CVD) or chemical vapor transport (CVT). While CVD is a well-established deposition method used in CMOS fabs, CVT is a novelty in industry relevant environments[474]. Today's best performing MoS_2 layers[475] are obtained epitaxially on sapphire[476–478] or directly deposited on amorphous substrates[479]. [480,481]In case of templated growth, an elevated growth temperature budget (700-1000˚C) is allowed, with a layer transfer step to a target wafer enabled[480,481]. Attention towards thermal budget and chemistry selection is essential in direct deposition methods. While CVT methods are typically yielding better performance devices in the lab, these methods suffer today from the use of Na^+-containing precursor salts, hindering the compatibility for integration in CMOS fabs.

The intrinsic passivated surface of 2D materials, having no dangling bonds, forces creative solutions for gate stack scaling. Typically, the implementation of interlayers allowing a smooth transition from a 2D surface to a 3D environment is used. Here, choices are made between a 2D interfacial layer like hBN or AlN[482], reducing the lattice mismatch; or simply use self-oxidized evaporated Si or metallic seed layers. Most engineering friendly toward high mobility channel devices, is the use of convention ALD methods[483] relying on physisorption of the precursor species to form the interlayer. Similarly, the best contact metals demonstrated in lab devices are Bi[394], Y[484], or Sb[485] deposited by evaporation or MBE techniques to force an epitaxial relation; typically, these are non-fab friendly approaches. Expecting a wraparound contact geometry is required to allow sufficiently high drive current, smart engineering solutions are to be developed for selective etch processes combined with ALD-like metal deposition approaches[486]. Importantly, defectivity healing, doping and functionalization methods are essential topics for further research exploration.

The major challenge for thin channel devices is adhesion and interface control. Minor variations in stress and strain, induced by topography or local anomalies (*e.g.*, stress in encapsulation layers, friction forces from the contacts) cause an immediate drop of the channel mobility. A well-designed process and material selection procedure for key integration processes like etch selectivity, surface cleaning, dedicated low mechanical force CMP techniques combined with smart integration choices will alleviate (some of the) current constraints.

5. Topological insulators for spin-orbit-torque-based magnetic devices

SOT-MRAM memory devices are currently explored at both academic and industrial level, primarily as a potential embedded SRAM-cache replacement. This 3-terminal device concept switches the magnetization of a magnetic free layer by passing a current through an adjacent metal line. The efficiency of this switching is directly linked to the efficiency of generating spin current at the metal surface for a given charge current through the line. Conventional materials used for the SOT track rely on high spin-orbit coupling materials such as Ta, W and Pt. However, the switching current achieved by these conventional materials remains relatively high and limits power gains and bit cell scaling potential of this technology. A much more efficient switching has been advertised using topological insulator (TI) material[487]. This is presumed to be linked to the predominantly surface conductivity of the TIs complemented by a spin-locking mechanism leading to opposite and complete electron spin polarization at the bottom and top interface of the film. However, this suggests the effect should occur mainly in single crystalline/epitaxial form of thin films, strongly complexifying its integration in a BEOL flow. Despite this, relatively high spin hall angles, a measure of the switching efficiency, have been observed in sputter deposited Bi_2Se_3 films[224]. Path to integration into a real SOT-MRAM flow remains difficult. While BEOL processing implies thermal budgets as high as 400°C, BiSb has a melting temperature of less than 300°C. Bi_2Se_3, one of the other main TI candidates seem to be unstable against 400°C thermal anneals. As shown in panel 7 Fig. 52, strong Bi and Se segregation is visible in the TEM cross section. Hence, further material research in thin topological insulator film growth is still very much needed.

Further down the line, one can anticipate that specific etching or passivation methods may be required. A standard SOT-MRAM flow includes the ion beam etching (MTJ) of the magnetic tunnel junction (MTJ) stopping precisely on the SOT track. While going away from IBE for the MTJ etch seems not to be possible for the foreseeable future, the increased sensitivity of the TI surface to damage can be expected and may require specific etch and passivation development.

6. Conclusions

When reviewing the potential of disruptive technologies, it is relevant to push the evaluation of complex functional materials beyond the classical materials screening in lab-research environments. A comprehensive understanding and the precise control of interfaces, as well as of the material composition and structure are crucial for achieving reliable device operation and performances. Therefore, process integration techniques play an important role in the fabrication process of relevant demonstrator devices, paving the way towards process scalability in industry relevant environments.

Acknowledgements

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Figures:

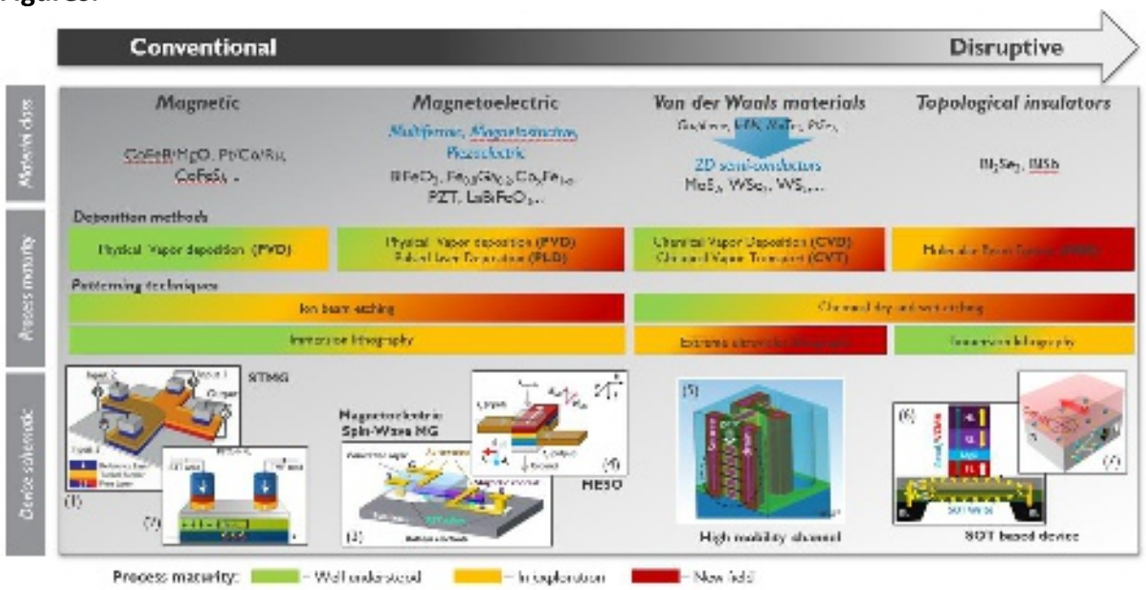

Figure 51. Overview of the materials, integration process maturity with matching schematic of representative devices: (1) Spin-transfer torque majority gate (STMG) (2) Schematic of a Domain-wall-based devices (from Ref. [453], see also Ref. [488]), (3) Magnetoelectric spin wave majority gate (from Ref. [80]), (4) Magnetoelectric spin–orbit element (from Ref. [11]), (5) Stacked MX_2 device-based inverter with four MX_2 layers (from Ref. [473]), (6) Field-free switching Magnetic Tunnel Junction with hybrid SOT track (from Ref. [489]), (7) Spin Hall magnetoresistance in TI/FM bilayer (from Ref. [490]).

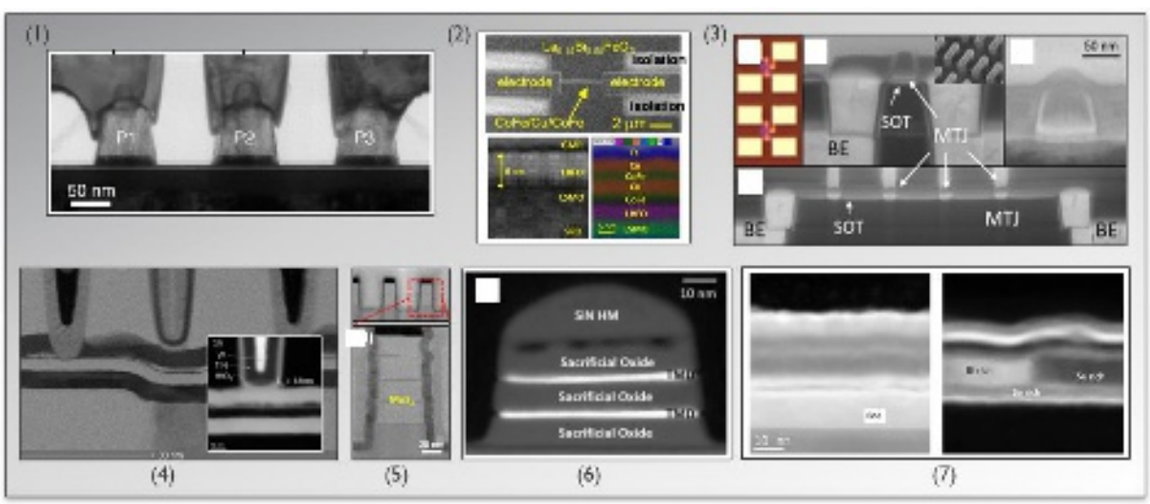

Figure 52. Transmission electron micrographs of different types of devices: (1) Three MTJs sharing the same magnetic free layer (from Ref.[453]); (2) SEM images of the fabricated GMR – Magnetoelectric device (top), Cross-sectional HR-TEM and EDX elemental of the ME stack (from Ref. [227]); (3) Multi pillar magnetic tunnel junctions sharing an SOT track (from Ref. [489]); (4) Integrated WS_2 single sheet transistor integrated in a 300 mm fab (from Ref. [483]), inset: HAADF of a full back gate device with SiO_2 cap; (5) 3-tier monolayer MoS_2 fin structure (from Ref. [491]); (6) A two-layer transition metal dichalcogenides stacked nanoribbon structure(from Ref. [492]); (7) PVD sputtered Bi_2Se_3 film prior (left) and after a 400°C anneal (right) (IMEC data, unpublished).

Fabrication and Manufacturing Aspects of Future Low-Power Electronic Devices

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Decades of transistor scaling on power and performance has prompted tremendous investment and R&D efforts that result in unprecedented advancement in precision materials engineering and unprecedented productivity that are enabled by the development of dedicated semiconductor manufacturing technology and equipment. Forecasted to grow to $100B by 2030, the industry has developed and refined specialized processing equipment for more than five hundred individual process steps typical for advanced technology node. Considering the emerging low power electronics technology, key technical challenges and recent advancements in processing and equipment are summarized.

Low power devices, such as Magnetic Tunnel Junction (MTJ) based devices are expected to adopt 300mm platform to leverage the advanced processing and metrology technologies developed for cutting CMOS, DRAM and NAND nodes.

CHALLENGES of FABRICATION

Fabrication of magnetic tunnel junction (MTJ) based devices poses challenges ranging from material complexity of the structure to process integration considerations. Indeed, state-of-the-art MTJ stacks involve dozens of atomically thin layers, with sharp interfaces and well-controlled crystal structures which are different in various part of the stack. Furthermore, this intricate multilayered material must be patterned into 30 to 80 nm pillars and withstand up to 400 ℃ during subsequent BEOL processes. Interface engineering will be crucial to successfully combining these materials by achieving a satisfactory balance between surface roughness and good magnetic properties[493].

Deposition and etching processes will have to achieve virtually atomic scale process control to ensure extreme uniformity and negligible surface roughness. For example, tunneling barrier uniformity is crucial for high tunnel magneto-resistance (MR) and depends primarily on the roughness of the bottom electrode[494].

Given the extreme thinness of the layers, etching must employ ultra-clean processes to avoid re-deposition of by-products or residue as this could lead to shorting. Cell profile control must be extremely exact to achieve consistency across large arrays. Several characteristics of the magnetic films in the stack pose further challenges. They are thin and susceptible to corrosion; hence effective passivation is of great importance to protect them from penetration or diffusion of such process chemicals as oxygen, chlorine, and bromine, which can alter the structure and properties of the films to reduce the MR effect. The magnetic moments of magnetic films depend strongly on the domains (grains) and grain boundaries of these materials that affect programing current. In addition, magnetic coupling between the fixed layer and the free layer through the tunneling oxide is greatly reduced by the grain boundaries. Signal-to-noise ratio also degrades as grain boundary increases or the number of grains within a MTJ cell varies significantly when MTJ cell size scales

down. Thus noise levels or signal inconsistency across the array increases as these variations becoming relatively larger.

From the integration standpoint, MTJ processes (typically <350°C) are compatible with CMOS back-end-of-line (BEOL) thermal budgets[495]. However, a holistic approach should be adopted, taking into account the total thermal budget including post-MTJ processing, to protect against adverse effects. For example, thermal fluctuation of magnetization can be caused by subsequent high-temperature processing; exposing the wafer to physical stresses can also induce altered magnetic properties as a result of changes in grain boundaries and interface properties. Additional challenges arise in large array operation. Besides increasing power consumption, large arrays drawing high current density exacerbate electrical stress and reduces transistor lifetime. Another consideration will be provision of magnetic shielding during assembly and testing to protect pre-magnetized cells from external magnetic fields.

RECENT ADVANCEMENT IN FABRICATION EQUIPMENT

Fortunately, recent advances in unit and integration processes, as well as ongoing development work, address many of the challenges cited above. Ultra-thin deposition of ultra-pure metals as well as metal oxides, metal nit rides, binary alloys, and magnetic materials has been made possible in volume production by RF sputtering, an adaptation of conventional DC physical vapor deposition (PVD) that enables virtually damage-free processing. RFPVD employs lower power levels than conventional DCPVD, which reduces the risk of plasma damage while enabling exacting control of thickness, stoichiometry, and deposition rate (on the order of 0.1-2Å/sec) for layers less than 10A thick. Low-temperature deposition also offers the advantage of producing smoother surface morphology. Rotating the wafer during deposition can improve within-wafer uniformity to the required 0.5 percent range. Surface roughness can be further reduced by rotating the wafer while exposing it to a mild argon sputter. With its ability to create highly uniform and conformal films with atomic level control, atomic layer deposition (ALD) has become an important thin films deposition process. This method uses pulses of gas to deposit material one atomic layer at a time. ALD can be enhanced with the application of plasma energy that promotes attraction of the required species to the wafer surface and accelerates the react ion (deposition cycle) while also improving film uniformity and quality. In STT-MRAM, plasma-enhanced ALD (PE-ALD) offers a good low-temperature approach for depositing thin spacer and passivation layers without adverse reactions to underlying metals[496]. In-situ annealing of the ALD film to achieve proper crystalline structure complements the uniformity of the deposition process in achieving the uniformity requirement for thin (<1nm) films in the MTJ cell stack.

The Endura® Clover® MRAM PVD system is the first production-worthy equipment for high-volume manufacturing of MTJ devices. The Clover system accommodates production of the entire MTJ stack, which can consist of more than 30 layers—most of which are just a few Angstroms thick—without a break in vacuum. The vacuum environment preserves the quality of the films (which inevitably degrade to some degree if removed from a system during processing), creating high-quality interfaces between layers, reducing the risk of defects, and enhancing the accuracy of the metrology that verifies deposition thickness precision and uniformity—essential for ultimate device performance.

The heart of the Endura Clover system is a chamber capable of depositing up to five different materials with outstanding uniformity. Several of these materials have not previously been used in CMOS technology. To ensure that each film is pristine, a rotating shield above the wafer exposes only one target material at a time to plasma bombardment which allows controlling thickness and uniformity of ultra-thin films. This creates optimal interfaces between the layers, essential for device reliability. The performance-critical tunnel barrier layer of magnesium oxide (MgO) tunnel barrier is deposited in a separate chamber equipped with specialized hardware that permits one-step deposition of the compound that allows good barrier integrity, stoichiometry, and particle control. This improves film integrity and uniformity, minimizes defectivity, and improves the memory read signal by increasing tunnel magnetoresistance (TMR). Subsequent annealing and cryogenic cooling further strengthen the film, fortify the TMR, lower the resistance to facilitate low power consumption, and create high thermal stability for better data retention.

The MTJ device can be tailored to emphasize data retention, low power and/or write speed, depending on the application. To deposit MTJ film with low resistance-area (RA) product, a co-optimization of MgO barrier/MgO cap thickness and additional buffers underneath is necessary to reduce effective barrier thickness while keeping good TMR.

As features become more densely packed, the gaps between electrical components become narrower, aspect ratios greater, and re-entrant profiles more common. This continuous challenge for scaling dielectric gap fill from each node to the next has driven innovation in chemical vapor deposition (CVD) to produce a fluid-like, profile-insensitive film that can be deposited at low temperatures, consistent with reduced thermal budgets at advanced nodes. Beyond achieving complete gap fill, dielectric films must satisfy additional requirements to be integrated into a device. They must have a high breakdown voltage to ensure electrical robustness. They must also possess good film density to ensure stability after chemical mechanical planarization (CMP), reactive ion etch, and wet cleans. The new flowable CVD film is comparable in these respects to high-quality, industry-standard high-density plasma CVD silicon dioxide[497].

High-temperature etching (150-250 °C), developed and proven for high-k/metal gate applications[498], is also being applied to such materials as magnesium oxide, ruthenium, cobalt-iron-boron, palladium, and platinum, manganese used in MTJ structures. Non-halide-based chemistries generally used in high-temperature etching do not adversely affect magnetic films and the tunneling dielectric as do the chlorine and fluorine chemistries typical of lower-temperature etch regimes. These high-temperature chemistries combined with precise plasma energy control throughout the entire stack etching sequence can create a smooth-walled and residue-free MTJ cell. Plasma pulsing is also being studied as a means of further optimizing this performance[499].

Low-temperature annealing processes are also required. Minimizing the thermal budget while sustaining minimum reaction temperatures for quality interfaces and proper material crystalline structures, in particular, necessitates low-temperature (<400°C) processes with fast and accurate control. Rapid thermal processing technology now accommodates processes at temperatures as low as 150°C , with transmission pyrometry enabling closed-loop monitoring of wafer temperatures as low as 75°C and multi-point measurement capability helping to improve die-to-die and wafer-to-wafer repeatability[500].

CMP is becoming a more frequent and challenging process in advanced integrations, such as FinFETs and MTJ devices. As features become smaller and more fragile, preservation of device topography through precision planarization end-pointing is crucial to successful device performance. Addressing this requirement. in-situ, high-resolution sensors now enable closed-loop, real-time thickness control during planarization by means of incremental changes to polishing conditions in multiple zones of the polishing head[501].

Depositing the MTJ film stack and creating the cell structure in a cluster platform can bring significant benefits. Integrating on one platform the entire stack with a pre-treatment process greatly reduces interface roughness between successive depositions. In addition, process monitoring, such as optical spectroscopy and wafer surface particle inspection, can be integrated into the system to enhance manufacturing quality. As for cell formation, similar clustering could combine low-temperature spacer/passivation PE-ALD with high-temperature etching. Multiple etch technologies, as described above, can be integrated onto the same platform for etching complicated stacks with accurate end point control to achieve high productivity.

CONCLUSION

CMOS, DRAM and Flash are facing serious limitations beyond the 2nm technology node, prompting the need for new devices, such as MTJ or spin-based low power electronics. While the material complexity and 3D architecture of this new structure pose challenges, many recent advances in deposition, etch, and related integration processes enable device manufacturers bring this technology to mass production on cluster-chamber platforms.

Ultrafast probes

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In the quest to develop next generation low power electronics, there exists often a fundamental correlation between devices which operate at low powers and devices which operate at high speeds. For example, the functionality, bandwidth, and power efficiency of phase-change memory (PCM) or ferroelectric devices for information storage technologies depend upon the energy barriers that separate different structural phases/atomic cell arrangements. These can be simply encoded in the latent heat of the transition in the case of a PCM device but can also involve more complex electronic contributions[502]. Quasi-isostructural phases associated with small atomic motions and low energy barriers / switching costs then lead to improvements in energy efficiency and are correspondingly faster in their evolution. Under equilibrium conditions, such speed improvements can be estimated by an effective Arrhenius factor or inverse reaction rate $\tau_{switch} \approx 1/\nu\, e^{\frac{\Delta G^*}{k_B T}}$ where ΔG^* is the free energy barrier and ν is an effective attempt frequency[503,504]. In this model the effective time-scale is determined by thermal, equilibrium fluctuations. In contrast, the switching times and energy costs can be engineered to take advantage of non-equilibrium drives which control the pathway for the transition or even reshape the potential barrier itself[190,505–509]. To enable such approaches, operando characterization techniques which can resolve the non-equilibrium transition states during the switching process are required.

Two examples of these concepts are shown in Fig. 53. First, we consider the prototypical insulator-metal switching process in VO_2 under pulsed electrical biases. These changes in the electrical properties are correlated with significant structural changes involving a monoclinic-to-rutile transition. Therefore an understanding of the dynamics and energy costs associated with this switching process require correlated dynamic probes of electrical transport and atomic-scale structure. Fig. 53a,b shows one such experimental effort in which femtosecond electron scattering sensitive to the changes in the structural properties are measured within an operating device enabling correlated probes of transport under pulsed electric field biases[507]. While there are many prior examples of photoinduced insulator-to-metal phase transitions in VO_2 and other complex oxides, the dynamics of electric-field-driven phase transitions remain much less understood. Fig.53a shows the experimental setup used for this work in which two-terminal devices were fabricated using 60-nm-thick polycrystalline VO_2 films deposited on 50-nm- thick free-standing silicon nitride membranes to enable a transmission-mode pump-probe electron diffraction measurement. The device was pumped stroboscopically by a 180 Hz train of voltage pulses and the time-dependent resistance across the device was simultaneously measured. Fig. 53b shows results correlating the dynamic drop in resistance, which occurs after some voltage dependent incubation time, with changes in several diffraction peaks sensitive to the unit cell structure. By analyzing crystallographically the relative changes in the measured diffraction peaks and building on prior photo-induced studies[510] it is concluded that the transition is not characterized solely by the formation of the rutile phase at short times but rather requires an intermediate pathway through a monoclinic metallic phase with similar atomic-scale structure but dramatically modified electronic properties. This work thus defines new possibilities for low energy switching, taking advantage of electric-field-induced metastable phases within solid-state devices. Similar possibilities have been

discussed in the context of prototypical phase-change materials in the context of threshold switching[511]. Given the unique ways in which both applied electrical biases and light can be used to modulate the structural properties of this material, future efforts could usefully explore the combination of pulsed electrical and optical fields to dynamically tune these structures and transiently reconfigure the logical state of an associated device depending on the time-delay between optical and electrical bias pulses.

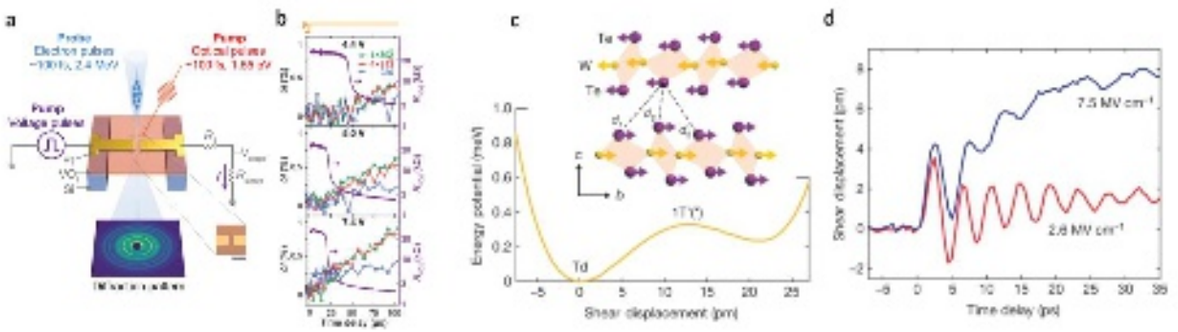

Fig. 53. a) Experimental setup for correlated dynamic structural and transport measurements of the voltage-driven insulator-metal switching process in VO_2. b) Measured changes in resistance (right axis) correlated to changes in intensity of several Bragg peaks for different applied voltages indicative of induction of metastable monoclinic metallic phase. Figure adapted from Sood et al., Science **373**, 352 (2021)[507]. c) Theoretical energy barrier separating equilibrium topological Td phase of the layered 2D material WTe_2 from centrosymmetric metastable phase accessed through interlayer shear motion. Inset shows associated atomic motion along b-axis of orthorhombic structure. d) Reconstructed interlayer shear motion under weak and strong field THz pulse excitation indicative of transient ultrafast switch to a centrosymmetric, topologically-distinct phase.

A second example demonstrating the power of coupling ultrafast characterization approaches towards the development of new types of low power and high speed non-volatile switches is shown in Fig. 53c,d. In this work[507], THz-frequency light pulses are used to induce a topological switch to a metastable phase in the Weyl semimetal WTe_2[507]. WTe_2 is a layered quasi-two-dimensional semimetal which has an equilibrium orthorhombic (Td) non-centrosymmetric unit cell with corresponding topological and ferroelectric properties. An interlayer sliding motion along the b-axis of the orthorhombic unit cell takes the structure towards a centrosymmetric 1T' phase. Continuation of this interlayer shear motion eventually forms an equivalent Td structure with inverted out-of-plane ferroelectric polarization[512]. The theoretical energy barriers for this transition correspond to energies of order 1 meV/unit cell[513] and corresponds to a soft phonon mode with frequency ~0.2 THz. Here the low energy barriers for this transition are associated with the weak van der Waals bonding of this 2D structure. In this work, the THz field induces a field-driven reversible transition on time-scales corresponding to this phonon period as shown in Fig. 53d, corresponding to transiently switching into a topologically-distinct, non-polar phase on picosecond time-scales mediated by high frequency interlayer strain. We note that this transition can also be driven by pulsed quasi-DC fields[512] and novel possibilities for device-scale switching similar to the VO_2 case discussed above could be usefully applied here, for modulating the coupled ferroelectric and topological properties of this material and other related 2d ferroelectrics[358].

The above examples represent two cases among many where ultrafast approaches sensitive to atomic-scale motion can enable new types of high speed, low power electronic switches. Important directions

for the future in the context of low power electronics should explore ways of doing more quantitative ultrafast calorimetry of these dynamic switches. The non-equilibrium phase transitions that often underlie these processes require efforts to go beyond the types of crystallographic approaches described above to track the intrinsic heterogeneity of these transitions and the role of fluctuations and disorder. For example, x-ray/electron diffuse scattering approaches[514,515] and various forms of coherent scattering techniques like x-ray photon correlation spectroscopy[516] enable access to the dynamic structure without providing an effective ensemble-averaged result. These approaches can extend the ultrafast calorimetric approaches described above to track entropy growth and production during materials switching events[517,518], dissipation losses, and the coupling to external environments while also providing sensitivity to dynamic heterogeneous processes at domain walls[519] and other defect states.

Synchrotron-Radiation Characterization of Low-Power Electronic Materials and Devices

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A. Status and impact to date

The development of low-power electronics poses characterization challenges that can be addressed in part by applying synchrotron radiation techniques. The challenge arises because low-power devices increasingly involve three-dimensional structures, subtle chemical and structural variations at the nanometer to submicron length scale, and time-dependent dynamics of structural and chemical properties. There have been rapid advances in synchrotron-based techniques, including in the use of tightly focused x-ray nanobeams, x-ray coherent diffraction techniques, and *in situ* experiments[520].

The challenge associated with the three-dimensional structure of devices has become particularly clear in the development of CMOS semiconductor devices based on FinFETs and similar architectures. Synchrotron-based nanobeam diffraction experiments with Si/SiGe nanosheets for gate-all-around devices have revealed the mechanisms of strain relaxation in these devices. These mechanisms are lateral deformation due to the lattice mismatch between Si and Ge and an out-of-plane distortion along the layering direction[521]. Nanobeam diffraction techniques have revealed the distortion resulting from the formation of complex electrode structures in SiGe and GaAs-based qubits. The nanoscale variation of the stress due to the electrodes results in a distortion that propagates to the depth of the two-dimensional electron gas in these structures and produces strain sufficient to affect the low-temperature operation of the devices[522–525]. Semiconductor devices also rely on precise nanoscale distribution of dopant atoms with nanoscale control. Dopant characterization using x-ray fluorescence provides spatially resolved maps of the distribution of dopants in Si devices[526].

The neuromorphic and resistive memory devices underpinning future low-power electronic technologies rely on precise nanoscale changes in stoichiometry and structure that can be difficult to control and characterize. Particular challenges have been in the device-to-device variation of these structures and in the quantitative comparison of models of the device operation with the nanoscopic features of the device. The variation in the valence can lead to structural changes that can be imaged using nanobeam x-ray diffraction[527]. The variation in valence can be imaged directly using x-ray absorption spectroscopy using tightly focused nanobeams[528]. Multimodal approaches correlate the structural and spectroscopic methods[529]. Crucially, both spectroscopy and diffraction can be used *in situ* during the operation of devices under ambient conditions appropriate to device applications. The operation of ferroelectric low-power devices depends on structural changes associated with the development of piezoelectric distortion and polarization switching. X-ray nanobeam techniques image the nanoscale ferroelectric domain distribution with spatial resolution on the scale of tens of nanometers[530].

In one particular study, the variation of the oxygen vacancy concentration *in situ* in a $WO_{3-\delta}$ test device was measured using simultaneous x-ray diffraction and x-ray absorption spectroscopy measurements with a nanofocused x-ray beam [531]. The results of this study reveal the existence of a threshold oxygen vacancy concentration for switching between the low-resistance and high-resistance states and the structural differences between electroformed state and these operation states. Images acquired using this approach, Fig. 54, reveal the structural and chemical differences between resistive states. The

impact of these in operando measurements of device switching lies in the ability to design mechanisms for the transformation between switching states.

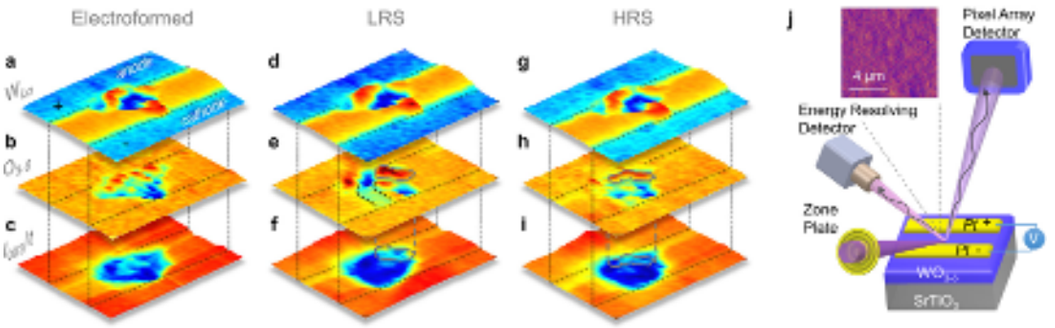

Fig. 54 Multimode x-ray nanobeam imaging of $WO_{3-\delta}$ test devices in the electroformed condition, low-resistance state (LRS), and high-resistance state (HRS). X-ray nanobeam methods provides the means to reconstruct the distribution of W x-ray fluorescence ($W_{L\alpha}$, panels a, d, and g), the oxygen deficiency ($O_{3-\delta}$, panels, b, e and h) and structural distortion (I_{003}/t, panels c, f, and i). Nanobeam imaging (j) allows this information to be collected simultaneously during device operation. After ref. [531].

A further aspect of *in situ* x-ray spectroscopy and scattering approaches is that the coherent scattering signature captures the fluctuations of the order parameters underpinning device operation, including nanoscale features of the ferroelectric polarization[532,533] and defect valence[534,535]. Equilibrium fluctuations provide insight into the free-energy landscape impacting devices and can be observed *in situ* using x-ray photon correlation spectroscopy. In particular, fluctuations between oxidation states of $SrCoO_x$ reveal that local considerations including the elastic state of the system, i.e. the distortion imparted by epitaxial strain must be considered in the free-energy landscape[534]. *In situ* studies also reveal that the dynamics of the transformations between relevant states can be highly heterogeneous. A recent ultrafast time-resolved x-ray nanodiffraction study revealed a localized phase competition and nucleation and growth dynamics[536]. Further studies of the dynamics promise to enable the selection of local structural configurations optimizing device operation[537].

B. Current and future challenges

The structural specificity of x-ray characterization of low-power devices will benefit significantly from the further development of structural analysis techniques that employ the optical coherence of x-ray beams. The development of fourth-generation synchrotron radiation sources is providing far higher coherent x-ray flux than the previous generations of light sources. Further development of coherence-based techniques also holds great promise. X-ray ptychography techniques can already be used to characterize the distortions of nanoscale semiconductor structures with a spatial resolution smaller than the x-ray spot size[538]. Coherent diffraction imaging techniques also provide strain information in stressed Si structures with nanoscale spatial resolution[539]. With further development coherence-based techniques can image more complex structures associated with nanoscale devices. Further developments in x-ray tomography employing diffraction and chemical contrast also benefit from the next generation of light sources and promise to address the challenge associated with the creation of three-dimensional devices.

A further ongoing challenge involves matching the timescale of x-ray characterization with the operating frequencies of emerging low-power electronic devices. Nanosecond time-resolved x-ray nanobeam diffraction techniques have been developed to probe polarization dynamics in conventional ferroelectric capacitor devices[540]. An important continuing challenge is to adapt and develop sub-nanosecond-scale characterization methods for emerging ferroelectrics such as HfO and for low-power electronic devices.

A complementary set of challenges arises in the development of insight into the growth mechanisms of materials relevant to low-power electronics. *In situ* x-ray diffraction revealed the role of polarization in the ferroelectric epitaxy[541]. Spectroscopy studies have probed the formation of $LaAlO_3/SrTiO_3$ interfaces hosting two-dimensional electron gases (2DEGs)[542]. In this case, the combination of structural information obtained using the analysis of Bragg rods arising from the thin film structure and spectroscopic information from x-ray photoelectron spectroscopy revealed the critical thickness for the formation of the 2DEG and the existence of multiple 2DEGs in a system with multiple interfaces[542]. A key aspect of the sensitivity of x-ray spectroscopy techniques to electronic phenomena is that photon energies resonant with electronic transitions in the atomic constituents of the materials can provide additional insight, including into band-splitting phenomena in semiconductor devices[543] and enhancement of the signals from thin layers[542]. Further developments of *in situ* synthesis methods can probe structural and electronic phenomena during synthesis and can shorten the materials development cycle.

Advances in Transmission Electron Microscopy Applicable to Low-Power Devices

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Transmission electron microscopy (TEM) is a technique that uses magnetic lenses to form images from electrons accelerated between 60 to 300 keV with sub-Angstrom to nanoscale resolution. TEM was critical to the improvement of previous generation microelectronics due to their high resolution capabilities for imaging manufacturing defects, understanding the effect of strain on channel resistance, understanding backend line edge roughness, and many more[544]. A cornerstone technique of materials science, the ability of TEM to directly image structure, composition, and bonding at high resolution make it indispensable as electronic devices continue to shrink and incorporate more elements from the periodic table. New computing, communication, and sensing devices based on quantum phenomena beyond charge pose challenges in manufacturing and materials discovery that require the application of advanced TEM techniques currently available and the development of new capabilities. Here, we briefly describe the impact of TEM on microelectronics investigations and recent developments that could impact the low-power electronics community.

Improvements in TEM over the last two decades stem from greater environmental and electronics stability, aberration correction, and better electron sources which together pushed resolution to below 0.5 Angstrom, reduced energy spread, and improved beam current such that most atomic spacings could be easily imaged[545–547]. Structural analysis can now be routinely accomplished at the sub-Angstrom scale using conventional TEM and scanning TEM (STEM) with the possibility to measure atomic shifts as small as 1 picometer[548–550]. This has been used to discover polar vortices in superlattices and investigate interfaces, among many other examples[362]. Many electronics structures with nanometer critical dimensions also exhibit a three-dimensional structure. Electron tomography was developed with nanoscale resolution based on annular darkfield (ADF-) STEM capable of differentiating materials in 3D based on Z-contrast[551,552]. Resolution in tomography has now been pushed to atomic resolution to image crystalline and amorphous solids[553,554] and can be used to measure 3D magnetic fields[555–557] and plasmon losses[558]. A technique known as electron energy loss spectroscopy (EELS) can map chemical composition and bonding with nano- to atomic-resolution based on energy loss to the primary beam[559–561]. Monochromation of the primary beam from 1 eV energy spread down to 0.1 eV provides access to regimes where bandgaps and plasmon resonances could be mapped and understood[562–564]. Energy dispersive spectroscopy (EDS) of x-rays generated by primary electrons has also seen a large improvement in collection angle improving signal and resolution allowing compositional maps of whole devices to be mapped in fractions of the time previously required[565–567]. The S-curve of technological development provided by aberration correction is leveling out and many would consider the resolution problem (posed by Richard Feynman in his famous lecture “Plenty of Room at the Bottom”) solved. However, the field of electron microscopy is currently poised at the start of two new technology development S-curves due to the recent introduction of direct electron detectors and improvements in monochromators that could have important impacts on materials discovery and low-power device development.

Direct Electron Detectors

Image acquisition in TEM initially used film which provided high dynamic range but had obvious drawbacks compared to the supplanting technology of digital charge coupled device (CCD) cameras. The

changeover to digital provided improvements in speed, immediate feedback, and access to larger datasets. Drawbacks of CCDs were their relatively slow readout speed, low duty cycle, and relatively poor sensitivity (compared to film). The recent introduction of a new detector technology based on complementary metal-oxide-semiconductor (CMOS) technology called direct electron detectors (DED) lead to the awarding of the 2017 Nobel Prize in Chemistry to cryoEM for the ability to solve macromolecular structures at nearly atomic resolution. A similar revolution is ongoing in the field of STEM where the introduction of DEDs is leading to new imaging capabilities with potential applications to low-power electronics[568,569]. The technique has become known as four-dimensional STEM (4D-STEM) because a two-dimensional diffraction pattern is acquired at every position in a two-dimensional grid of probe positions. This allows the capture of large amounts of information from highly localized regions of a sample where post-processing is then used to extract meaningful information.

Virtual detectors can be used that mimic traditional round bright field and dark field STEM detectors, but any detector shape can technically be utilized to generate contrast[569]. This also provides access to a new form of imaging generally called phase contrast STEM which is more sensitive to light elements such as oxygen that were previously difficult to image. In one simple technique, the shift of the center of mass (CoM) of the diffraction pattern is used to generate differential phase contrast and was first demonstrated on $SrTiO_3$. This is becoming a ubiquitous imaging method for light atoms and defects which are important in low-power materials[570,571]. The CoM method is also sensitive to magnetic and electric fields inside and outside samples providing the potential to measure quantities beyond structure[572–575]. The CoM technique is limited by the size of the electron probe such that imaging bonding at deep sub-Angstrom scales requires further development of aberration correctors to produce even smaller electron beams[576].

A more powerful method called ptychography utilizes overlap of information between neighboring electron beam positions to improve contrast, resolution, and dose efficiency[577–579]. This technique has pushed resolution beyond the intrinsic resolution of the microscope set by the electron beam diameter to a limit set by thermal atomic motion[580]. Similarly to CoM, ptychography can also be used to image fields and when used in concert with Lorentz STEM (where the sample is in a field free environment) the ability to improve resolution beyond the diffraction limit could provide critical insights into the workings of new devices[581].

Data organization and analysis is a major issue facing the TEM community due to the rapid expansion of DED technology where faster detectors allow the production of ever larger datasets. Over the last decade, single data sets have increased from megabytes to hundreds of Gigabytes and the amount of data acquired per session will only increase with newer detectors and automation[582]. Rapid development of open-source software that can handle large data sets at scale with rapid interactive feedback to users[583,584] during a microscope session will be critical to the wide-scale use of the benefits provided by DEDs.

Electron Energy Loss Spectroscopy

The speed and sensitivity of DEDs is also being utilized to improve EELS[585]. It is now routinely possible to measure weak core-loss signals indicative of complex bonding at atomic resolution[586,587], but the sensitivity also allows energy loss features far beyond traditional limits to be measured[588,589]. This expands the usefulness of EELS for interrogating materials composition and bonding across the periodic table especially useful due to the non-standard materials used in low-power electronics.

In tandem to the improvements provided by DEDs, recent advances in monochromation of the primary election beam are providing access to energy loss regimes never before possible in TEM[590]. Many important energy loss transitions such as vibrational losses to phonons occur in the sub-100 meV regime inaccessible using previous monochromators. Although optical and scanned probe techniques provide very high energy resolution, they either have micron-scale spatial resolution or are limited to surface investigations. The

ability of STEM to confine an electron beam to the atomic scale and image through 10-100 nanometers of material are a unique combination of capabilities. The limits are then set by sample-beam interactions at the nanometer scale[591]. Field emission electron sources typically have an intrinsic 0.3 – 1.0 eV energy spread which could be reduced by monochromation to about 100 – 300 meV as mentioned previously. A new generation of monochromators reaches below 10 meV resolution opening STEM-EELS to an entirely new regime of energy loss transitions at the nanometer scale[592]. Phonon transitions occur in this new regime such that vibrational spectroscopy has been used to image the influence of defects on phonon scattering[593], and resolution has been pushed to the atom level[593,594]. Isotope analysis at high resolution has also been proven[595] and could be a powerful technique to investigate issues with decoherence channels and quantum noise in quantum color centers or other exotic low-power devices. New materials systems and structures provide the ability to create and control exotic quasi particles at the nanoscale with potential applications in quantum technologies and other applications. Further improvements in superconducting electron sources[596] and microscopy cryogenic technology could push EELS to study emergent quantum phenomena that can only be investigated at low temperatures[597].

Concluding Remarks

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The need for Energy Efficiency in Computing: In this Roadmap exercise, we have attempted to capture some of the key issues that we believe are critical for the field of Microelectronics. It is by no means comprehensive: indeed, we believe trying to make this Roadmap comprehensive is futile, given the pace at which innovations are occurring globally. Many of the authors we sought reports from just did not have the time to contribute to this roadmap. Thus, it is simply a set of "snap-shots" of the field. As one looks to the future, this field is emerging as a critical focal point (if not THE focal point) not just for companies and research organizations, but at the national level. Nations are bringing their resource base to bear to establish R&D as well as design and manufacturing capabilities, while large corporations are deploying microelectronic devices at an exponential rate, both in numbers and in size. This roadmap was pulled together just to ensure that amidst this global race for "computing supremacy" (with obvious implications in national security), one does not forget the Energy and Climate Change implications of this exponentially growing field.

Pathways to Energy Efficiency: Energy efficiency in computing can be achieved by many pathways. Indeed, for the field this is opportune, since it provides us with multiple directions to pursue. This roadmap does not provide a deep-dive into 3-D architectures as a pathway to energy efficient electronics, mainly due to the Applied Physics/Materials focus of the journal. There are indeed significant activities on-going worldwide that are focused on this (a great example is the 2018 Turing Prize talk by Hennessy and Patterson). It is becoming increasingly clear that going Beyond-CMOS requires going to CMOS+X, where X is adding additional functionality or exploring additional fundamental degrees of freedom, in addition to the electronic charge. In doing so, this is already opening up vistas that were heretofore not explored. While there is a plethora of approaches for memory applications, logic has, so far, been focused on CMOS transistor as the building block. Will this change, going into the future? Can we access the spin degree of freedom, as discussed by Nikonov and Young as well as other authors? We will need new process integration tools to bring in these new materials and functionalities. Do we have to change the architecture to take advantage of new materials physics? How about the substrates themselves? Given the explosion of flexible electronics, it is very likely that a host of flexible substrate platforms are added to the standard Si-CMOS platform. This brings with it a host of processing issues, including the interface chemistry, thermal expansion mismatch related stresses, and so on.

The role of New Materials and Materials Physics : can we bring the full power of fundamental materials physics to bear? We believe there will be a strong push towards seeking the limits of fundamental phenomena, as we gracefully transition from the digital domain into the quantum. There is still quite a bit of room between these domains that can be tapped into. A good example is the case of topological insulators: is there a possibility of introducing such exotic electronic materials into applications, for example as the spin-orbit layer in spintronics (see article by Nikonov and Young) or as interconnects that have no scattering? How does one enable significant advances in spin-to-charge conversion for energy efficient spintronics: are there fundamental limits to this process OR can one design innovative heterostructures to resonantly enhance this process? What are the limits to the voltages required to manipulate ferroelectrics and multiferroics: can we get to below 100mV and beyond? Accomplishing all of these and more will require a significant amount of both fundamental and applied science. So, an exciting journey waits us…

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