PERFORMANCE EVALUATION OF DIFFERENT SRAM CELL STRUCTURES AT DIFFERENT TECHNOLOGIES

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ABSTRACT

In recent years the demand for low power devices has been increases tremendously. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area, thus designers are required to choose appropriate techniques that satisfy application and product needs. The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System On-Chip and high-performance VLSI circuits. This paper represents the simulation of different SRAM cells and their comparative analysis on different parameters such as Power Supply Voltage, area efficiency etc to enhance the performance. All the simulations have been carried out on BSIM 3V3 90nm, 45nm and 32 technology at Tanner EDA tool.

KEYWORDS

CMOS Logic, Low power, Speed, SRAM and VLSI.

1. INTRODUCTION

The term memory is usually used as a short hand for physical memory which refers to the actual chips capable handling data. The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. Solutions involving additional transistors, i.e., 8T, and 9T, 10T, Differential 10T have been explored to lower power consumption while reducing these adverse effects in the cell performance. We will therefore look into a couple of these SRAM Cells topologies that allow the analysis and simulations of different parameters at 90nm, 32nm and 45nm technology successfully on the basis of the power dissipation, speed and their temperature dependence with the area efficiency of the circuit.

2. LITERATURE REVIEW OF DIFFERENT SRAM CELLS

2.1 6T SRAM Cell

In such a case, the SRAM voltage does not scale with technology and could even be increased as variability intensifies. The schematic diagram of 6T SRAM cell is shown in Figure.1 [1]. During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and QB. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD.

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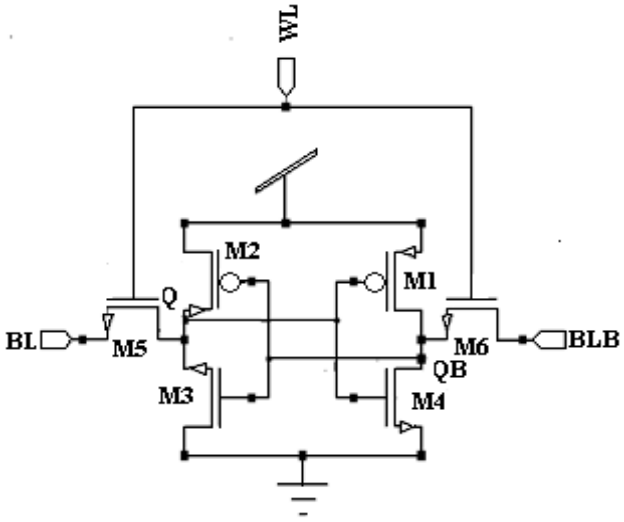


Figure 1. Schematic of 6T SRAM Cell

2.2 8T SRAM Cell

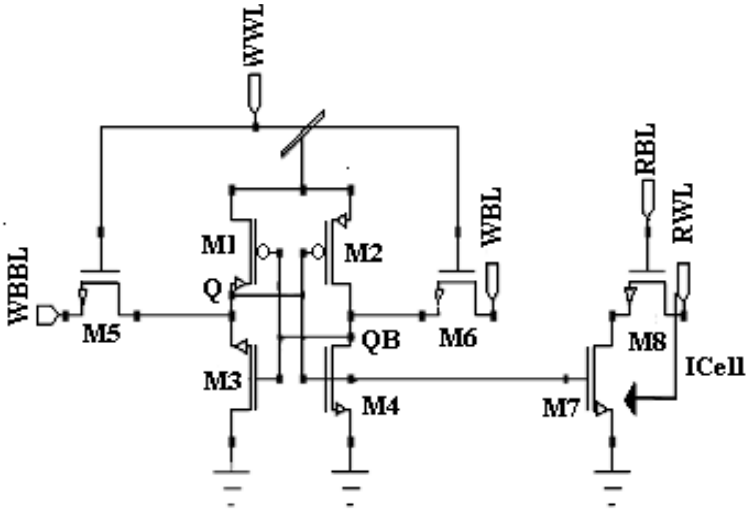


Figure 2. Schematic of 8T SRAM Cell

A dual-port cell (8T-cell) is created by adding two transistors, the read can be entirely decoupled from the write operation in an 8T cell by sensing the data through a separate read stack controlled by a separate read wordlines (RWL).The remaining 6T portion of the cell is optimized for write, resulting in an overall lower Vmin. Separation of data retention element and data output element means that there will be no correlation between the read SNM Cell and I Cell. Thus, an 8T SRAM design [5] contains a write assist in which a horizontally routed VDD line is collapsed during write. As a result, the bit cell array Vmin is limited by the hold margin.

2.3 9TSRAM Cell

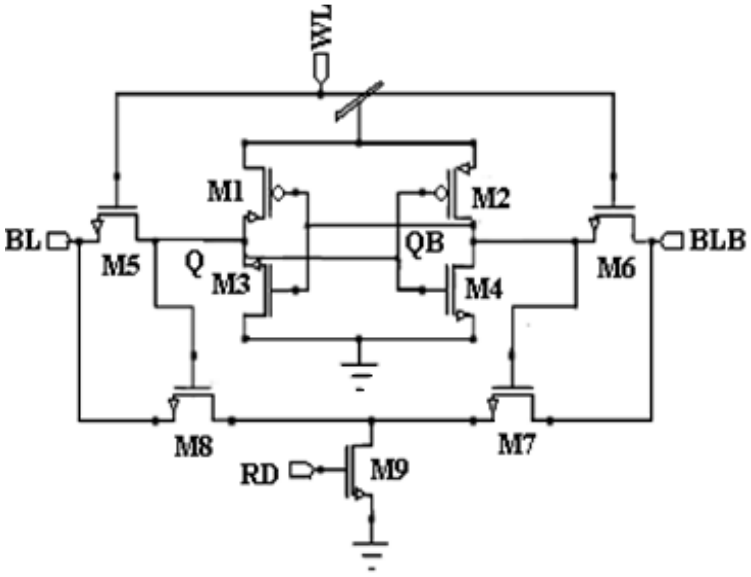


Figure 3. Schematic of 9T SRAM Cell

The schematic of the 9T SRAM cell, for CMOS technology, is shown in Figure.3. The upper sub-circuit of the 9T memory circuit is essentially a 6T SRAM cell with minimum sized devices (composed of M3, M4, M5, M6, M1 and M2).The two write access transistors (M5 and M6) are controlled by a write signal (WL). The data is stored within this upper memory sub-circuit. The lower sub circuit of the new cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9). The operations of M7 and M8 are controlled by the data stored in the cell. M9 is controlled by a separate read signal (RD) [7].The 9T SRAM cell completely isolates the data from the bit lines during a read operation.

2.4 10T SRAM Cell

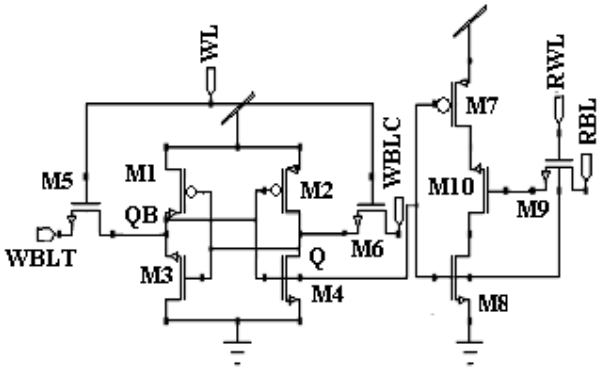


Figure.4 Schematic of 10T SRAM Cell

Figure.4 shows the schematic of the 10T sub threshold bit cell.[6] Transistors are identical to a 6T bit cell except that the source of M1 and M2 tie to a virtual supply voltage rail Vdd. Write access to the bitcell occurs through the write access transistors, M5 and M6, Transistors from the write bitlines, WBLT and WBLC. Transistors M8 through M10 implement a buffer used for reading.

Read access is single-ended and occurs on a separate bitline, RBL, which is precharged to prior to read access. The wordline for read also is distinct from the write wordline. One key Advantage to separating the read and write wordlines and bit lines is that a memory using this bit cell can have distinct read and write ports.

2.5 Modified 10T SRAM Cell

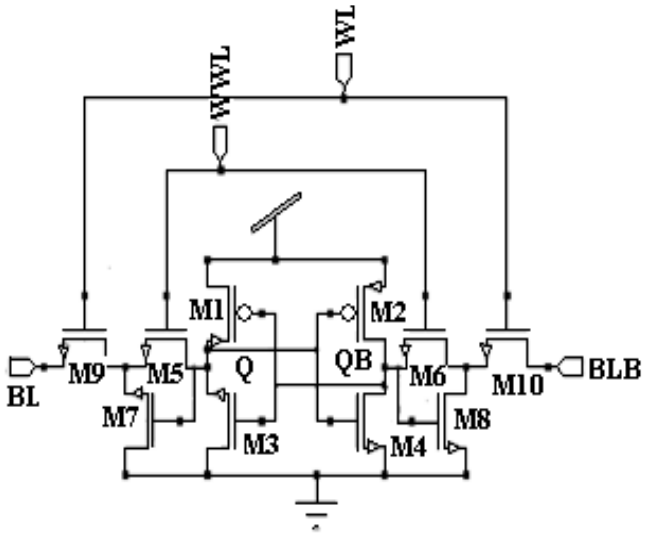


Figure.5 Schematic of Modified 10T SRAM Cell

Figure.5 shows a schematic of a 10T SRAM with differential read bitlines (BL and BLB) [6].Two NMOS transistors (M9 and M7) for the RBL and the other additional NMOS transistors (M8 and M10) for BLB are appended to the 6T SRAM. The 10T cell permits bit interleaving and exhibits superior sense margin with a differential read path based on a DCVSL (differential cascade voltage-switch-logic level) structure at the column periphery [8].There is a performance degradation from stacked transistors that requires boosted WL voltages, but BL leakage is reduced at the same time.

3. SIMULATION PERFORMANCE AND ANALYSIS

All the circuits have been simulated using BSIM 3V3 90 nm, 45nm and 32nm technology on Tanner EDA tool with supply voltage ranging. To make the impartial testing environment all the circuits has been simulated on the same input patterns. Figure 6-Figure17 shows comparative analysis of the circuits stated above at 90nm, 45nm and 32nm technology. The simulation results reveal that 10T Modified SRAM Cell at 90nm and 45nm technology and 10T SRAM Cell at 32nm technology shows always best performance for the range of power consumption, operating frequency and temperature [3, 9].

3.1 Simulation of different SRAM cells at 90nm technology.

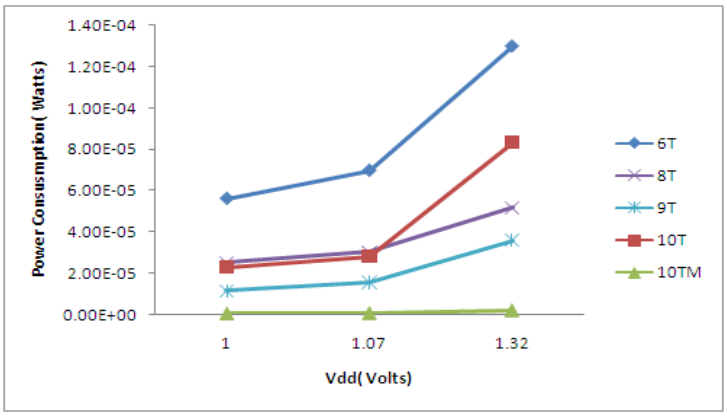


Figure 6. Power Consumption vs. Vdd for Different SRAM Cells

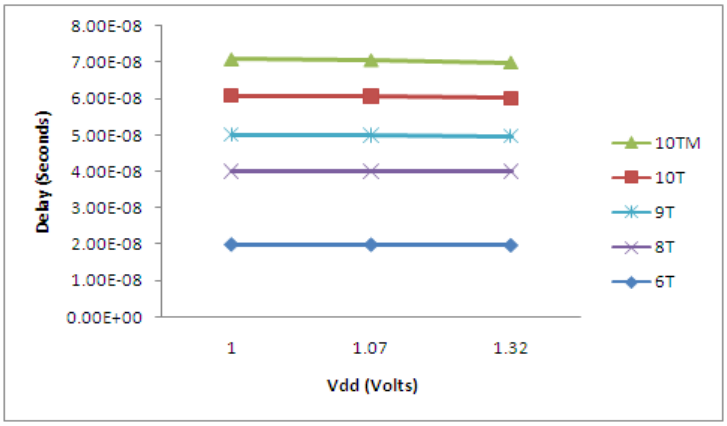


Figure 7. Delay vs. Vdd for Different SRAM Cells

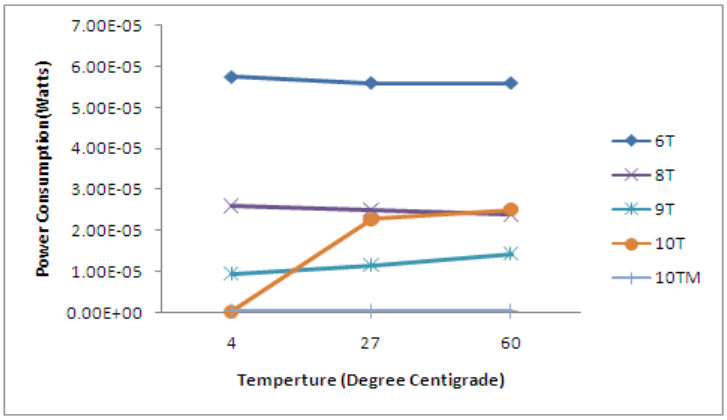


Figure 8. Power Consumption vs. Operating Temperature for Different SRAM Cells.

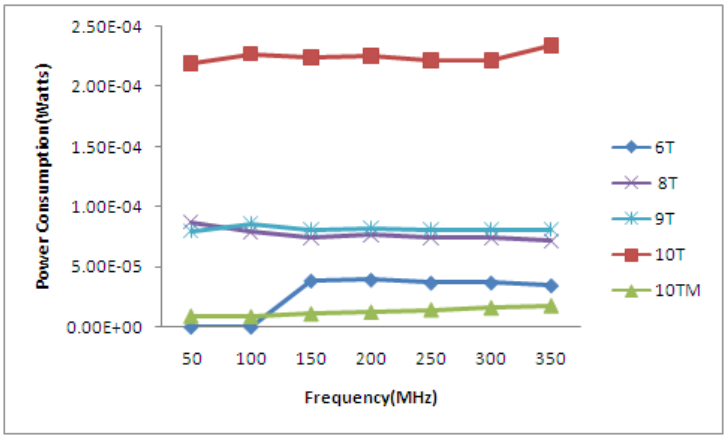


Figure 9. Power Consumption vs. Operating Frequency for Different SRAM Cells

3.2 Simulation of different SRAM cells at 45nm technology.

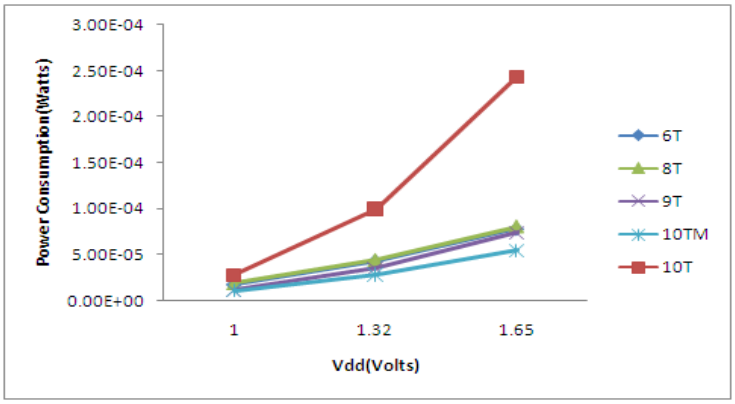


Figure 10. Power Consumption vs. Vdd for Different SRAM Cells

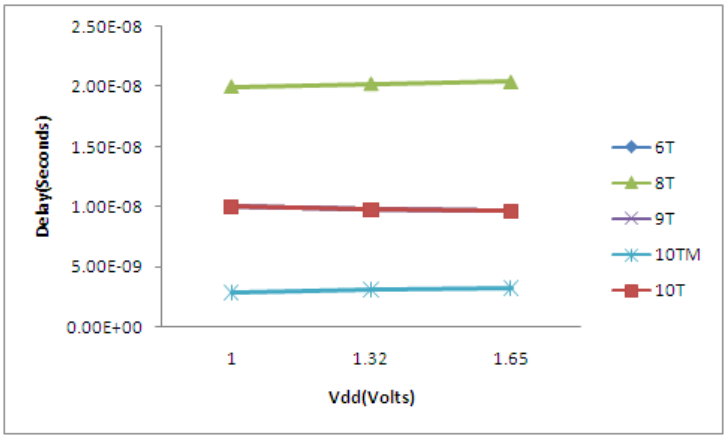


Figure 11. Delay vs. Vdd for Different SRAM Cells

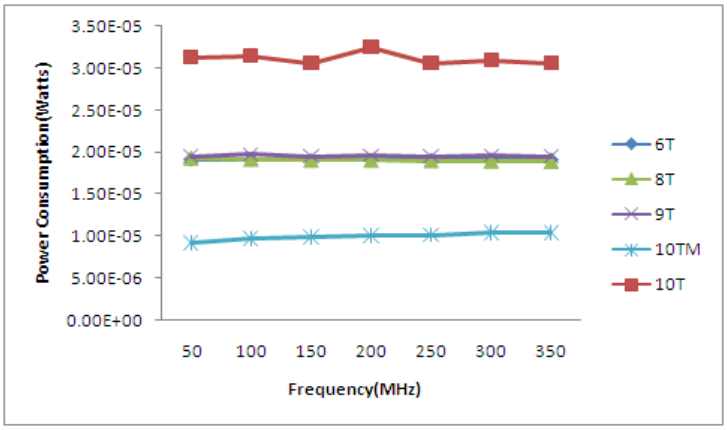


Figure 12. Power Consumption vs. Operating Frequency for Different SRAM Cells.

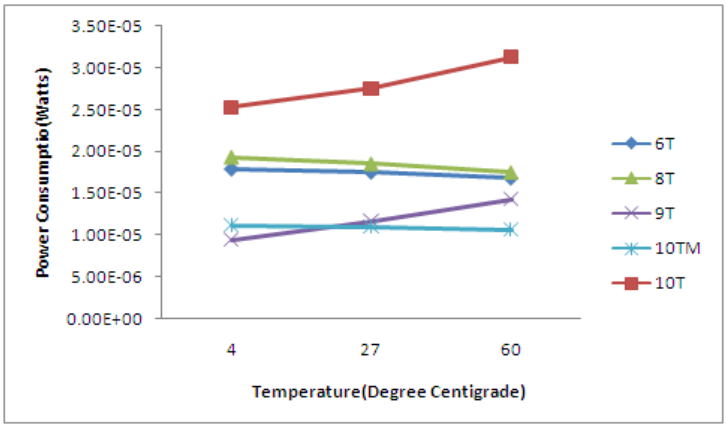


Figure 13. Power Consumption vs. Operating Temperature for Different SRAM Cells

3.3 Simulation of different SRAM cells at 32nm technology.

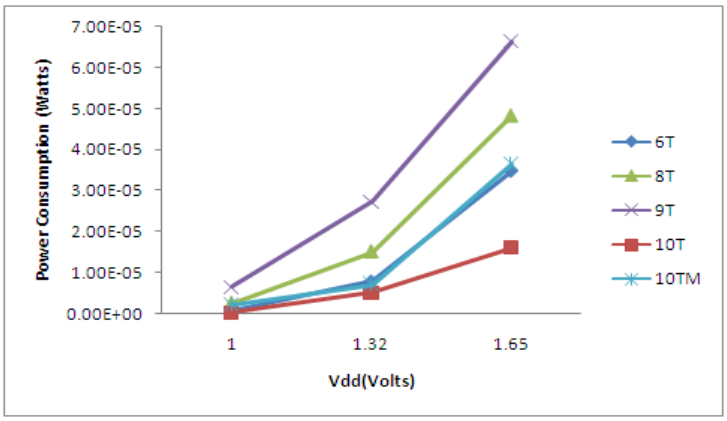


Figure 14. Power Consumption vs. Vdd for Different SRAM Cells

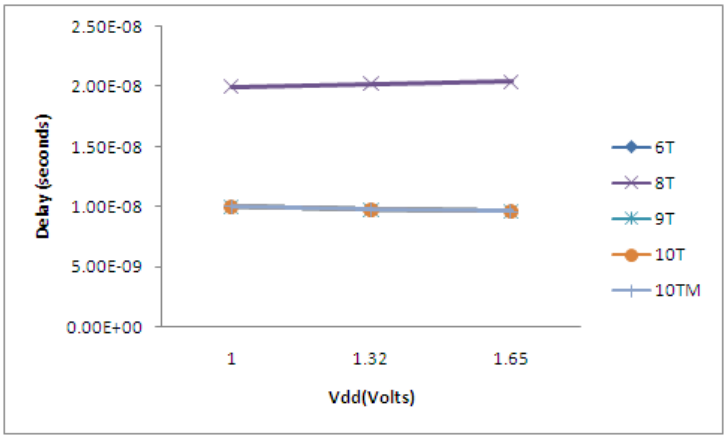


Figure 15. Delay vs. Vdd for Different SRAM Cells

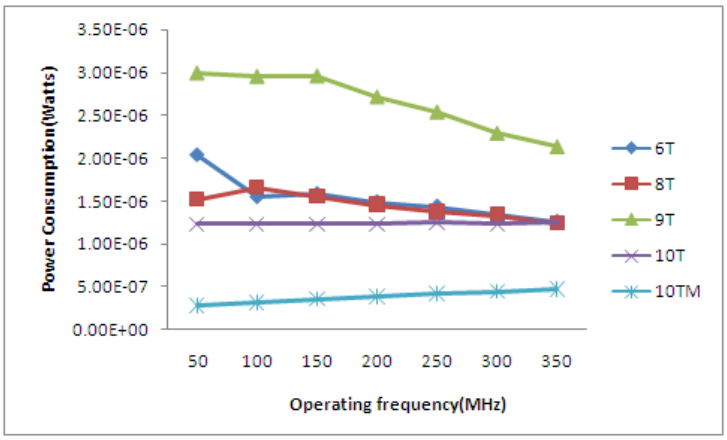


Figure 16. Power Consumption vs. Operating Frequency for Different SRAM Cells.

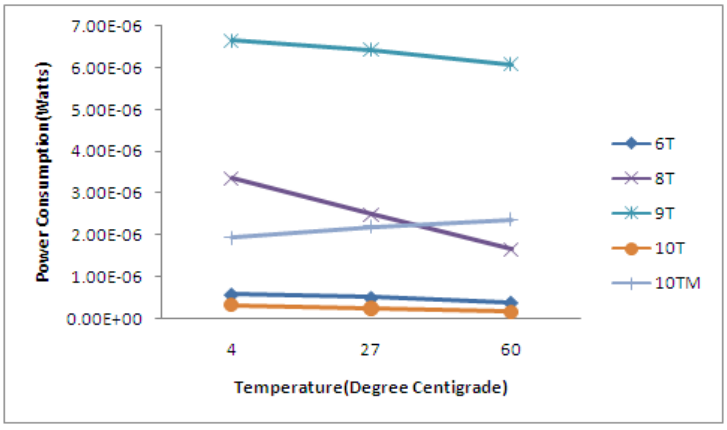


Figure 17. Power Consumption vs. Operating Temperature for Different SRAM Cells.

4. OBSERVATIONS

The following are the observations of power delay product of different SRAM cells at different technologies with supply voltage ranging.

Different SRAM Cells	Power Delay Product(watts-seconds)		
	Vdd=1v	Vdd=1.07v	Vdd=1.32v
6T	1.12E-12	1.39E-12	2.57E-12
8T	5.03E-13	6.06E-13	1.05E-12
9T	1.16E-13	1.56E-13	3.49E-13
10T	2.46E-13	3.00E-13	8.60E-13
10TM	**3.04E-15**	**4.85E-15**	**1.78E-14**

Table 1. Power Delay Product comparison of different SRAM cells at 90 nm technology.

Different SRAM Cells	Power Delay Product(watts-seconds)		
	Vdd=1v	Vdd=1.32v	Vdd=1.65v
6T	1.75E-13	4.19E-13	7.05E-13
8T	3.70E-13	9.72E-13	1.65E-12
9T	1.16E-13	3.49E-13	7.11E-13
10T	2.75E-13	9.74E-13	2.34E-13
10TM	**3.08E-13**	**8.54E-13**	**1.74E-13**

Table 2. Power Delay Product comparison of different SRAM cells at 45 nm technology.

Different SRAM Cells	Power Delay Product(watts-seconds)		
	Vdd=1v	Vdd=1.32v	Vdd=1.65v
6T	4.97E-15	7.55E-14	3.33E-13
8T	5.00E-14	3.05E-12	9.85E-13
9T	6.43E-14	2.66E-13	6.37E-13
10T	**2.52E-15**	**4.91E-14**	**1.57E-13**
10TM	2.21E-14	7.02E-14	3.50E-13

Table 3. Power Delay Product comparison of different SRAM cells at 32 nm technology.

5. SIMULATION RESULTS

Figure 18-Figure 22 shows output waveforms of different SRAM cell structures stated above at 90nm, 45nm and 32nm technology.

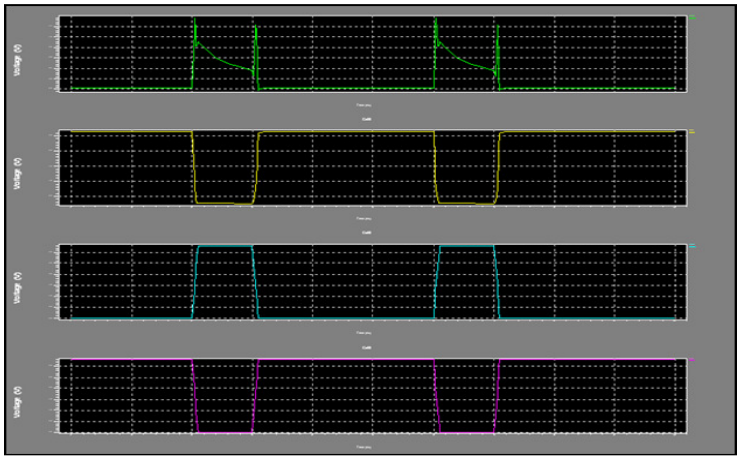
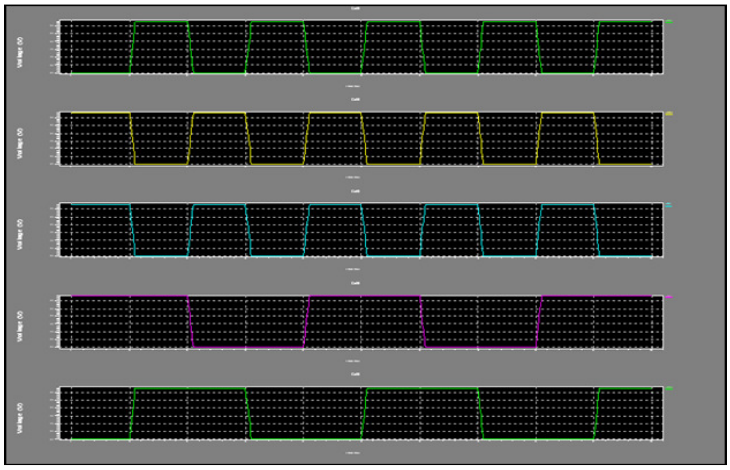


Figure 18. Output waveform of 6T SRAM cell.



. Figure 19. Output waveform of 8T SRAM cell

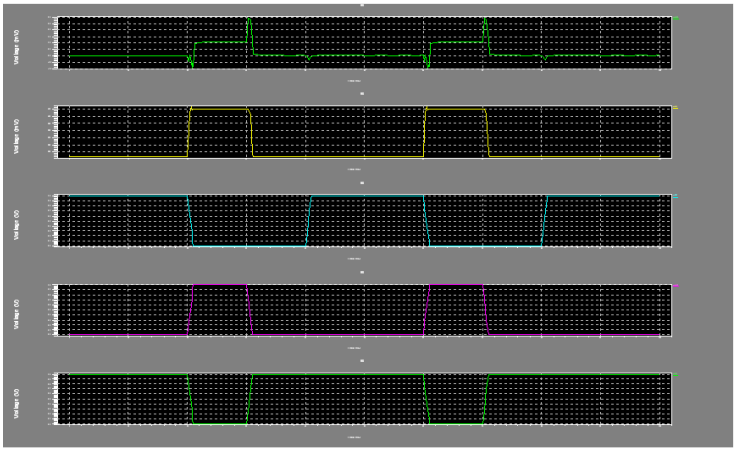


Figure 20.Output waveform of 9T SRAM cell

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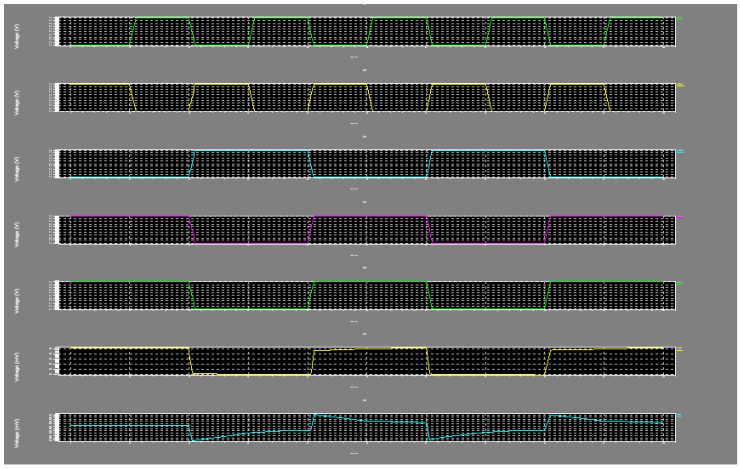

Figure 21.Output waveform of 10T SRAM cell

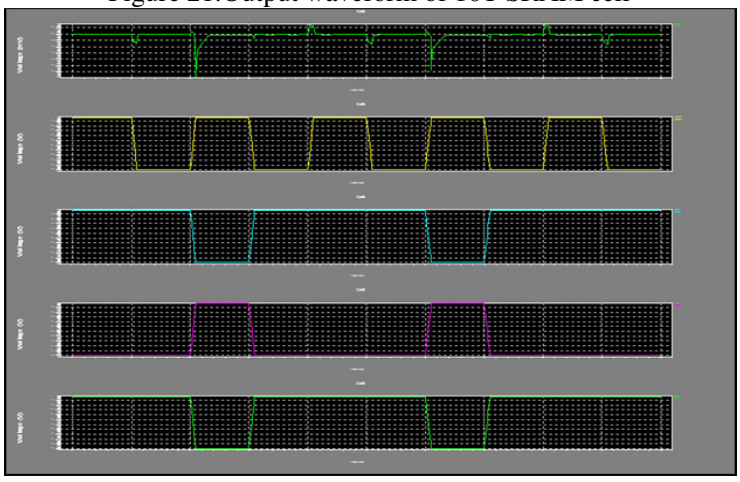

Figure 22.Output waveform of Modified 10T SRAM cell

6. CONCLUSION

A conclusion section must be included and should indicate clearly, the most efficient technique to reduce the power dissipation is the reduction of the supply voltage. The power dissipation reduction in SRAMs is not only due to power supply voltage reduction, but also to operating frequency and temperature. All the above figures depicts that 10T Modified SRAM cell at 90nm and 45nm technology and 10T SRAM cell at 32nm technology shows better performance for the range of frequency and temperature among all the other design approaches for SRAM cell. This paper tries to find out an efficient SRAM memory cell in both the aspects power consumption and speed in terms of power delay product at different technologies.

7. ACKNOWLEDGEMENT

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