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High Efficiency Class-F Power Amplifier Design

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***Abstract*—**Due to the high increase in and demand for a wide assortment of applications that require low-cost, high-efficiency, and compact systems, RF power amplifiers are considered the most critical design blocks and power consuming components in wireless communication, TV transmission, radar, and RF heating. Therefore, much research has been carried out in order to improve the performance of power amplifiers. Classes-A, B, C, D, E and F are the main techniques for realizing power amplifiers.

An implementation of high efficiency class-F power amplifier with Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) was realized in this paper. The simulation and optimization of the class-F power amplifier circuit model was undertaken using Agilent's Advanced Design system (ADS). The circuit was designed using lumped elements.

***Keywords*—**Power Amplifier (PA), Gallium Nitride (GaN), Agilent's Advanced Design system (ADS) and lumped elements.

I. Simulation Methodology Class-F PA Design And Choosing of Operation Frequency

TO configure and design class-F PA, a non-linear model, EGN030MK GaN-HEMT by Modelithics was used. This model is prepared for use to operate from 0.1 to 4.0 GHz with low current, wide band and high power design [5]. Hence, 1.7GHz was chosen as an operation frequency in this paper.

A. Choice of Bias Point

From Figs. 1 (a)-(c), gate to source voltage (Vgs) was chosen -0.6V when drain to source voltage, Vds was chosen 35V.

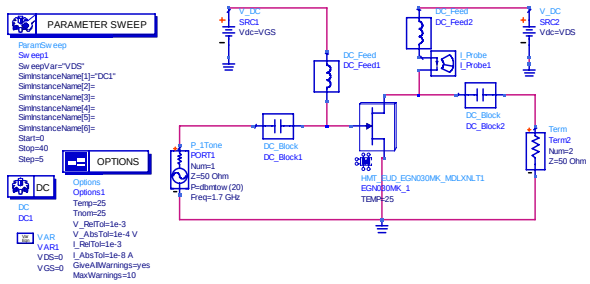

Fig. 1 (a) Schematic of Transistor Biasing

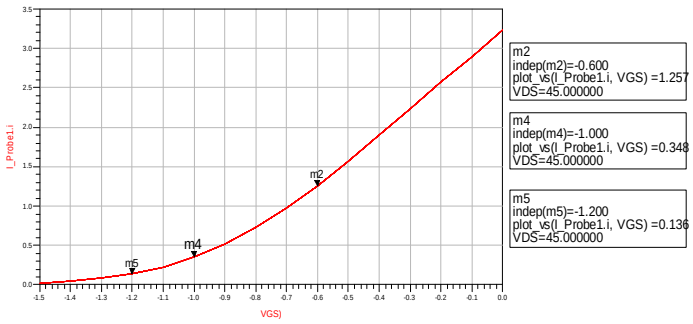

Fig. 1 (b) I_{ds} vs. Vgs Characteristics for V_{ds}=35 V

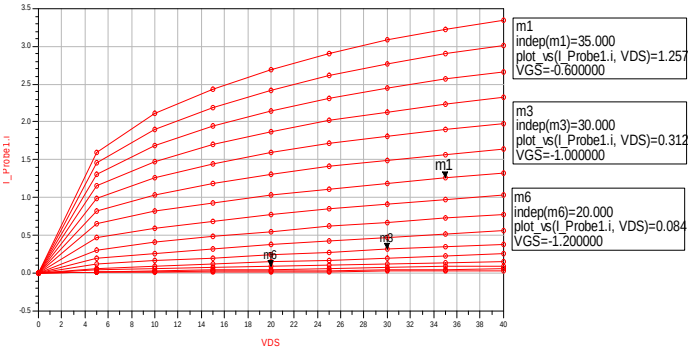

Fig. 1 (c) I_{ds} vs. V_{ds} Characteristics for Different Vgs Values

B. DC-Bias Circuit Design

In lumped elements configuration, DC-block acts as an ideal capacitor used to oppose varieties in voltage while DC-feed acts as an ideal inductor used to oppose varieties in current. Therefore, preventing DC current from affecting the input and output lines is done by DC block while the AC current is allowed to pass throw. DC current is allowed by DC-feed in order to bias the transistor while the AC current is blocked from passing throw [1], [2].

C. Output Matching Network

In Fig. 2, output network was done using lumped elements. The first tank was tuned at 5.1GHz which is the 3rd harmonic frequency ($3f_0$). The assumed value of C is 33pF and calculated value of L is 0.0295nH.

R_L can be measured at chosen bias point as following [3]:

$$R_L = \frac{V_1}{I_1} = \frac{\left(\frac{4}{\pi}\right)V_{DD}}{\left(\frac{\pi}{2}\right)I_{dc}} = \frac{8\,V_{DD}}{\pi^2 I_{dc}}$$

$$R_L = (8 \times 35) \div (\pi^2 \times 1.257) = 22.57\Omega$$

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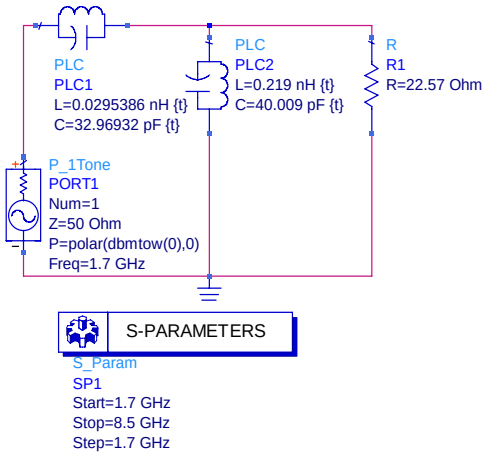
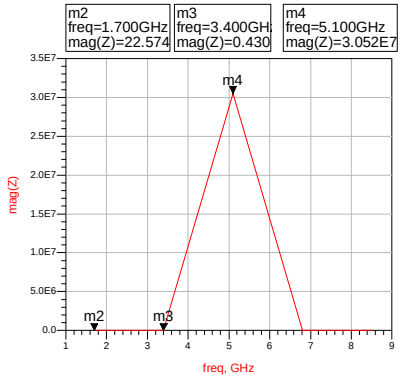


(a)

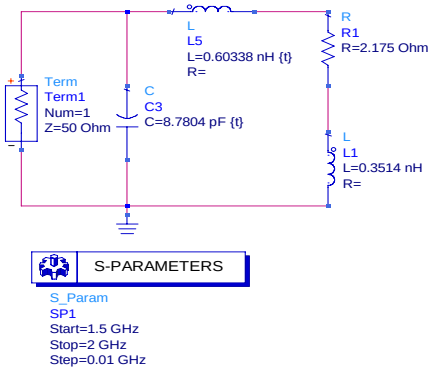


(b)

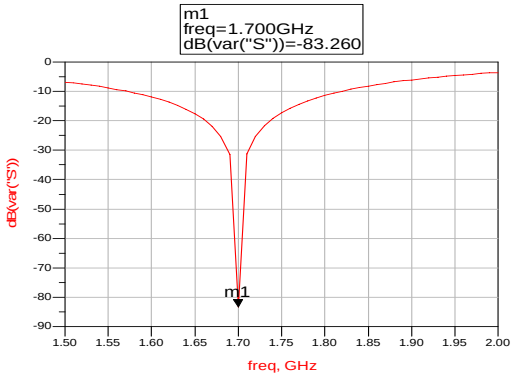
Fig. 2 (a) Schematic of Output Network for Third-Harmonic Peaking Circuit; (b) Output Impedance of the Schismatic

Input Matching Network

Fig. 3 shows the response of the input matching circuit. It can be seen that the minimum value of the reflection coefficient, -42.138 dB, occurs at 1.7 GHz, which means that the load is matched at that frequency.



(a)



(b)

Fig. 3 (a) Schematic of Input Matching Network Using Lumped Elements; (b) S-Parameters Output of the Schematic

D. Integration of Amplifier Components

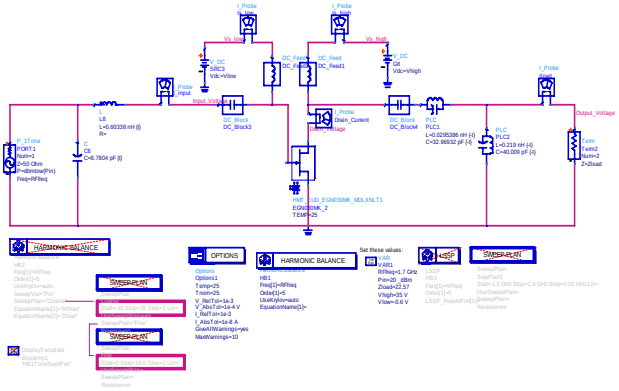


Fig. 4 Schematic of the Lumped Elements Class-F PA Circuit

E. Simulated Results

Drain voltage and current waves were achieved in the following figure after running Harmonic Balance (HB) simulation of the three different circuits. This was done with, f_0=1.7GHz, Pin=20dBm, Vgs=-0.6V and Vds=35V.

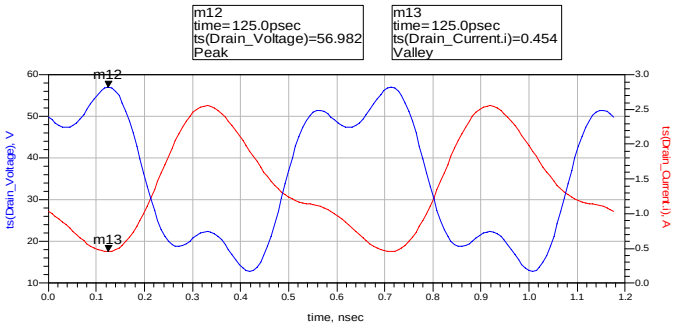


Fig. 5 Simulated (Time Domain) Drain Voltage and Current Waveforms of the Lumped Elements Circuit.

F. Input and Output Voltage Waveforms Simulation Results

Input and output voltage waves were achieved in the following figure after running Harmonic Balance (HB)

simulation of the three different circuits. This was done with, f_0=1.7GHz, Pin=20dBm, Vgs=-0.6V and Vds=35V.

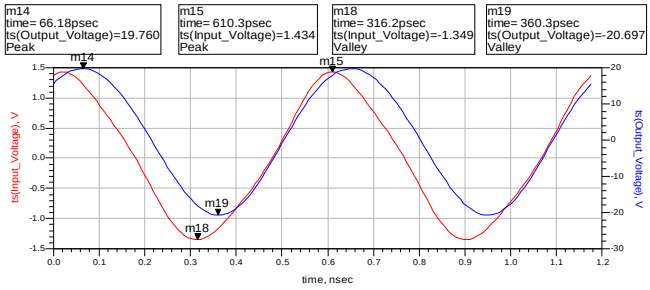


Fig. 6 Simulated Input and Output Voltage Waveforms of the Lumped Elements Circuit.

G. PAE vs. P_{in} Simulation Results

The effect of increasing Pin on PAE were achieved in the following figure after running Harmonic Balance (HB) simulation with SWEEP PLAN of the three different circuits. This was done with, f_0 = 1.7GHz, Pin = [-10 to 35dBm], Vgs=-0.6V and Vds=35V.

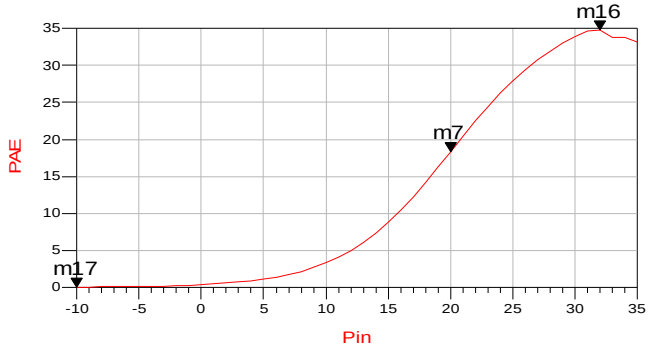


Fig. 7 PAE(%) vs. Pin(dBm) Simulation Results of the Lumped Elements Circuit.

II. Conclusion

This paper has presented the analysis and design methodology for a Class-F PA. In ADS software, Class-F PA was configured using lumped elements. Maximum output power, gain and power added efficiency of 39.57 dBm, 19.57 dB and 18.38% respectively were obtained by the lumped elements Class-F PA circuit at an operation frequency of 1.7 GHz, an input power of 20 dBm and a bias point of Vds=35 V and Vgs=-0.6 V.

III. Future Work

As mentioned in [6] and [4], a series capacitor and shunt inductor can be included in output network as a compensation circuit in order to absorb the effect of the internal parasitic components of the packaged transistor. This in turn increases the complexity of the output network, but improves the efficiency of Class-F PA.

References

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