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Reduction of Leakage Power in Digital Logic Circuits Using Stacking Technique in 45 Nanometer Regime

P. K. Sharma, B. Bhargava, S. Akashe

***Abstract*—**Power dissipation due to leakage current in the digital circuits is a biggest factor which is considered specially while designing nanoscale circuits. This paper is exploring the ideas of reducing leakage current in static CMOS circuits by stacking the transistors in increasing numbers. Clearly it means that the stacking of OFF transistors in large numbers result a significant reduction in power dissipation. Increase in source voltage of NMOS transistor minimizes the leakage current. Thus stacking technique makes circuit with minimum power dissipation losses due to leakage current. Also some of digital circuits such as full adder, D flip flop and 6T SRAM have been simulated in this paper, with the application of reduction technique on 'cadence virtuoso tool' using specter at 45nm technology with supply voltage 0.7V.

***Keywords*—**Stack, 6T SRAM cell, low power, threshold voltage.

I. Introduction

CMOS is simply a combined circuit formed by P-type and N-type Metal Oxide Field Effect Transistor [1]. The Portability of digital designed circuits place restriction on size, weight and power, since power is very much important as the conventional Ni-Cd (nickel cadmium) battery technology provides 20w/h of energy for each pound of weight [2]. Today we have number of leakage control techniques such as keeping high threshold voltage and scaling supply voltage [3]. Scaling of supply voltage can reduce up to 30% of leakages in digital circuits. Also stacking of OFF transistors can reduce the leakage current which is mainly focused and analyzed [4].

Scaling is necessary to minimize the power consumption and to increase life time of the CMOS designed circuits. Supply voltage always scaled along with the threshold voltage so as to minimize the propagation delay which is an imparting and most controllable significant factor. This subthreshold scaling causes to an increase in leakage current. This results to dissipation of power in the digital circuits, when resided in sleep or standby mode [5].

We prefer CMOS to design the digital circuits because of fabulous advantages, as it is easy to implement and occupy less space when laid over IC chip, dissipates less power when static and for same set of functionality. It assumes to be large density comparatively. Today integrated circuits are replacing with CMOS to all previous implementations [1].

Pradeep Kumar Sharma, Bhanupriya Bhargava, and Shyam Akashe are with the ITM Universe, Gwalior (e-mail: prdpsharma690@gmail.com, bhanupriya.190@gmail.com, shyam.akashe@itmuniversity.ac.in).

II. Implementation of Logic Gates with Stacking

The paper here describes the analysis of leakage power consumption for following logic gates and digital devices with and without the application of reduction techniques.

A. CMOS Inverter

A CMOS inverter gives output high for low input and vice versa. As shown in Fig. 1, the pull up network gives output high for low input pair of combinations and it has seen that the leakage current is a result of function of input values in the logic gate. Because the input pair only decides the number of OFF transistors in the pull up and pull down network of logic gates [6]. More number of available inputs reduces the leakage current to more significant level in the circuit. The reason is effective resistance offered by the stacking of transistor while OFF causes to reduce leakage current. Therefore in standby mode leakage power can be controlled [7]. The schematic of conventional CMOS inverter is shown in Fig. 1 (a) and Fig. 1 (b) shows the schematic of stacked CMOS inverter. Also, output waveform of CMOS inverter is shown in Fig. 1 (c).

TABLE I
Truth Table for CMOS Inverter

Input	Output
0	1
1	0

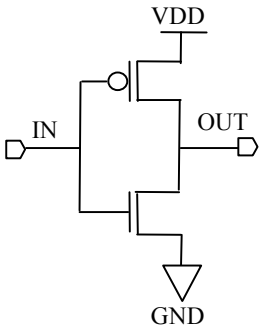

Fig. 1 (a) Conventional CMOS Inverter

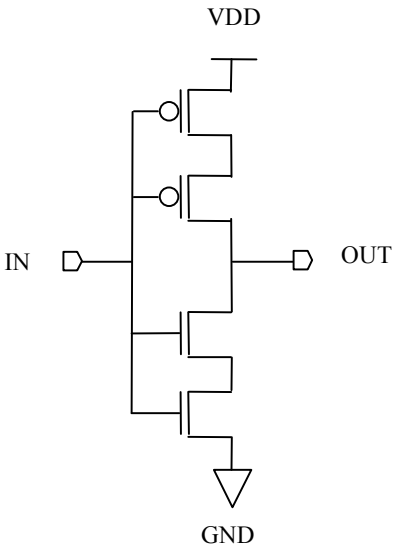

Fig. 1 (b) Stacked CMOS Inverter

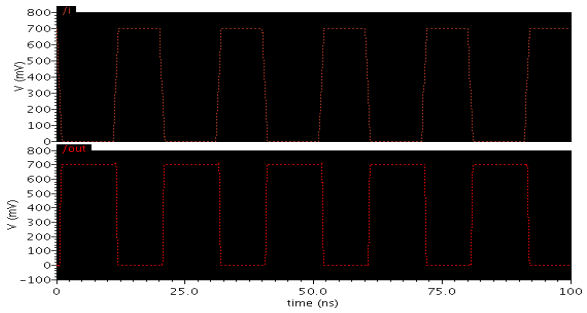

Fig. 1 (c) Output waveform of CMOS INVERTER

B. AND Gate

The PMOS and NMOS in stacking technique are split into two transistors for implementing AND gate. Fig. 2 (a) shows the schematic of conventional AND gate and Fig. 2 (b) the schematic of stacked AND gate. The leakage power of conventional AND gate is 1.28pw and using proposed technique the leakage power of AND gate is reduced down to .94pw. The output waveform of AND gate is shown in Fig. 2 (c).

TABLE II
TRUTH TABLE FOR CMOS AND GATE

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

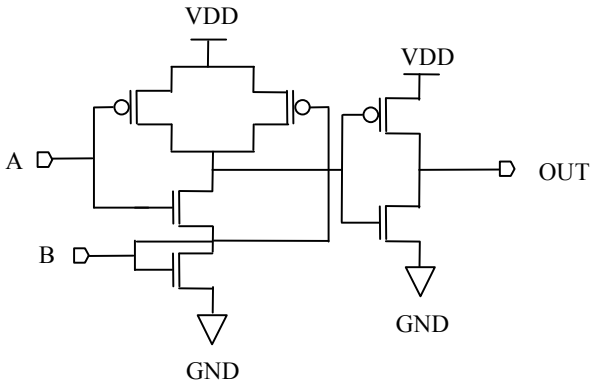

Fig. 2 (a) Conventional CMOS AND Gate

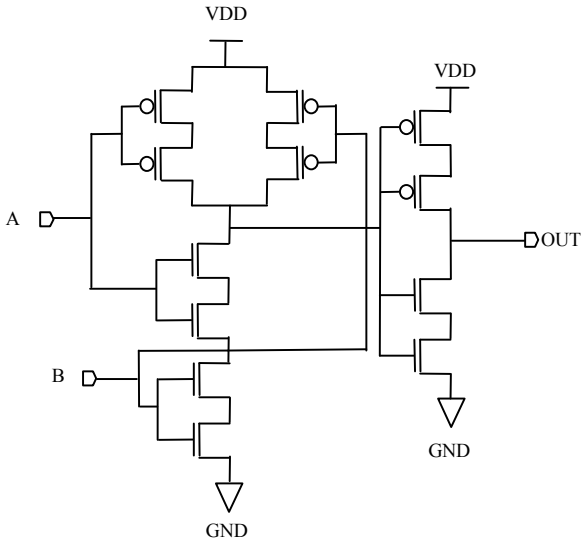

Fig. 2 (b) Stacked CMOS AND Gate

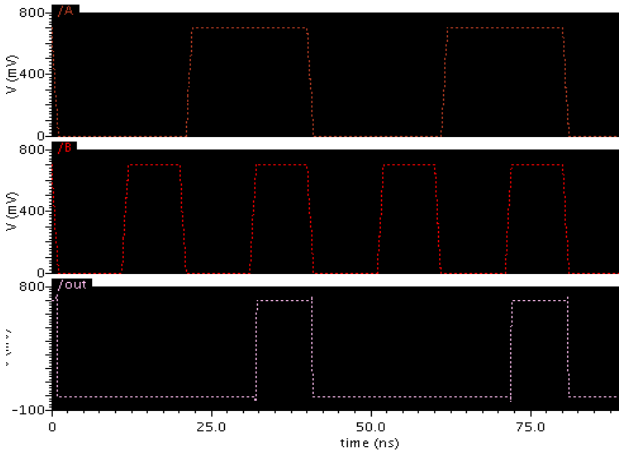

Fig. 2 (c) Output waveform of AND gate

C. OR Gate

By using stacking technique, the leakage power of OR Gate is reduced down to 1.14pw from 2.87pw. Figs. 3 (a) and (b) show the schematic of conventional OR gate and stacked OR

gate respectively. And the output waveform of OR gate is also shown in Fig. 3 (c).

TABLE III
TRUTH TABLE FOR CMOS OR GATE

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

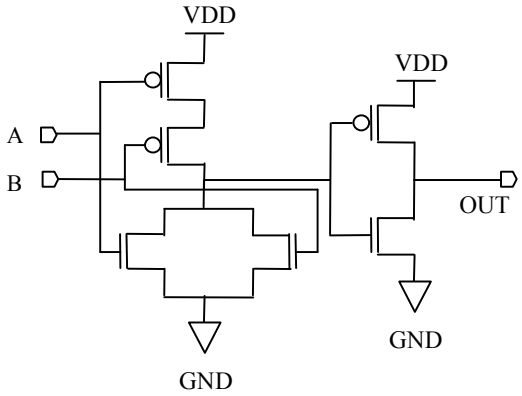

Fig. 3 (a) Conventional CMOS OR Gate

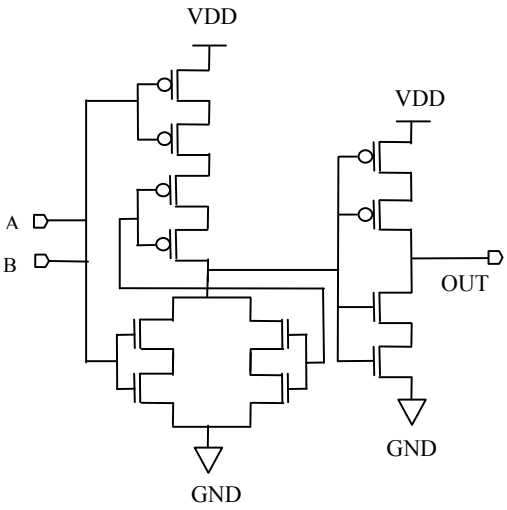

Fig. 3 (b) Stacked CMOS OR Gate

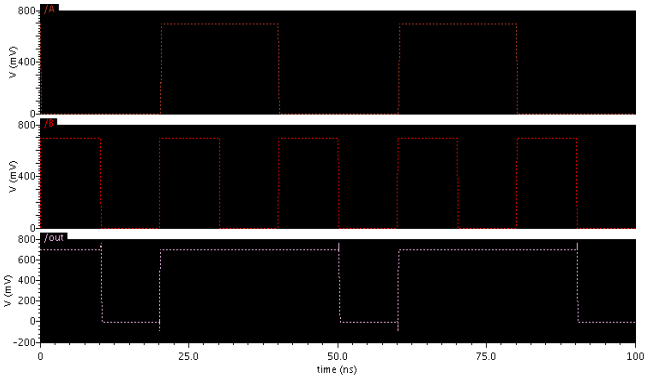

Fig. 3 (c) Output waveform of OR gate

D.XOR Gate

This technique brings the leakage power again down to 1.62pw from 1.97pw. Schematic of conventional XOR gate and stacked gate of the same is shown in Figs. 4 (a) and (b) respectively along with the output waveform shown in Fig. 4 (c).

TABLE IV
TRUTH TABLE FOR CMOS XOR GATE

Input		Output
A	B	Y=A'B+AB'
0	0	0
0	1	1
1	0	1
1	1	0

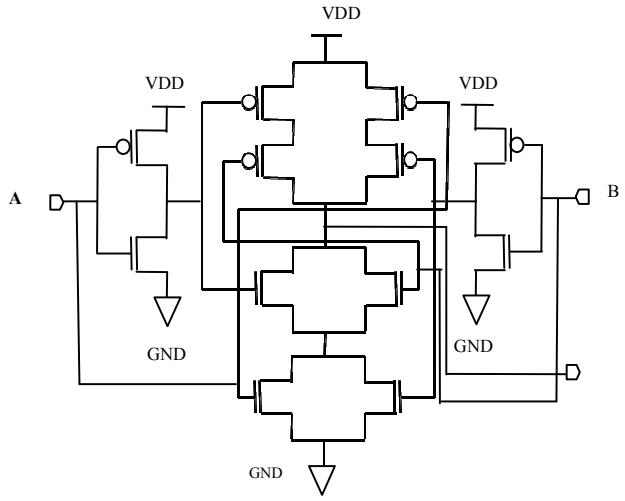

Fig. 4 (a) Conventional XOR Gate

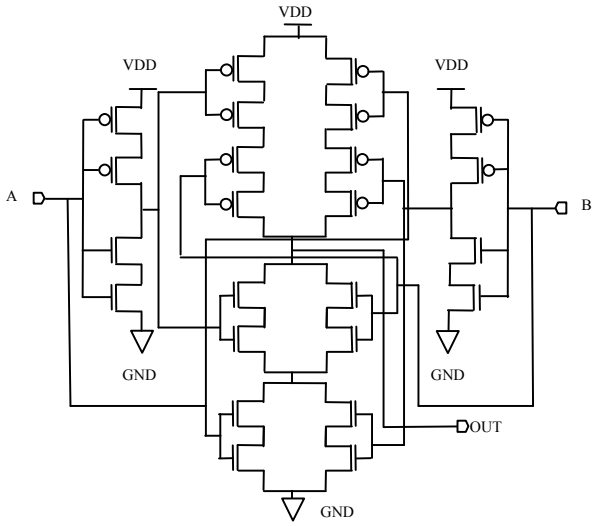

Fig. 4 (b) Stacked XOR Gate

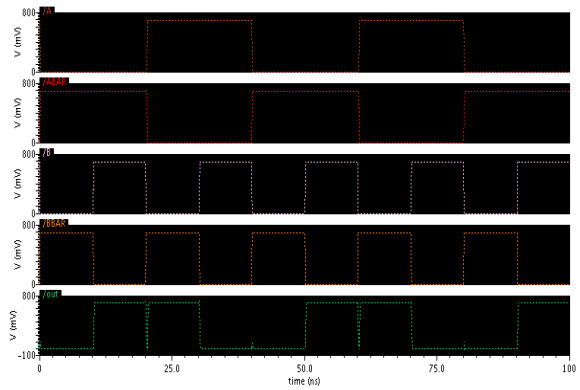

Fig. 4 (c) Output waveform of XOR gate

III. Implementation of Combinational Circuit with Stacking

Combinational logic elements are the simple devices consisting of logic circuits, and are utilizing mostly in this digital era. These circuits consume power at significant level and result in overall power dissipation in the complete device wherever they were used. Reduction in power consumption in these circuits would reduce power of the devices to a appreciate level. The paper here describes the analysis of various combinational circuits with and without the application of the reduction technique.

A. Full Adder

In many VLSI systems, addition is a basic fundamental arithmetic operation used in a various digital applications. Some of these applications are digital signal processing system, computers and microprocessor. In many digital circuits, addition is performed by using full adder [8]. The basic operation of full adder is to perform 3 bit addition [9]. Fig. 5 shows the schematic of basic 3 bit full adder using logic gates. The leakage power of conventional full adder circuit thus minimizes to 2.23pw, which is largely differentiated from 2.23pw. The logic circuit and output waveform is shown in Figs. 5 (a) and (b) of full adder circuit.

$$\text{Sum} = A'B'C + A'BC' + ABC + AB'C'$$
$$C_{OUT} = A'BC + AB'C + ABC' + ABC$$

TABLE V
Truth Table for Full Adder

Input			Output	
A	B	C_{IN}	SUM	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

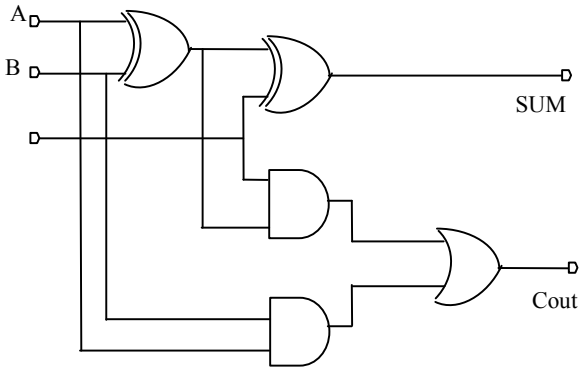

Fig. 5 (a) Schematic of basic Full Adder Circuit

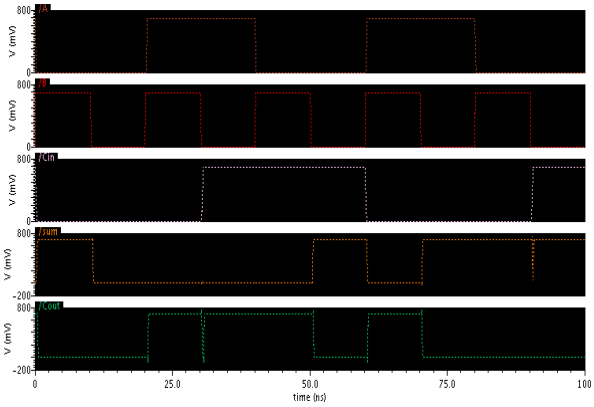

Fig. 5 (b) Output waveform of Full Adder

IV. Implementation of Sequential Circuits

Sequential circuits are nothing but the combinational circuits with feedback. These circuits form the basis of memory element in digital devices. Sequential circuits are utilized in different structures like memories, flip-flops, counters and registers. Improvement in power performance of these circuits is thus necessary to improve the performance of the digital circuits utilizing them. This paper here, deals with

few of them with and without the application of the reduction technique.

A. D Flip Flop

To design integrated circuits the flip flops are used to store binary data [10]. This storage element is capable to store 1 bit data. The D flip flop is mostly used in digital circuit. Output waveform of D flip flop shows that, when the clock inputs is logic 'LOW' the output of D flip flop holds the previous state and when the clock input is logic 'HIGH' the output of D flip flop follows the input of D flip flop which is clearly defined in the Truth Table VI. Thus it is observed power reduction of 2.06 pw occurred instead of 2.07pw of D flip flop. The logic circuit of D flip-flop shows in Fig. 6 (a) and the output waveform of D flip-flop show in Fig. 6 (b).

TABLE VI
TRUTH TABLE FOR D FLIP FLOP

Input		Output
CLK	D_{IN}	Q_{N+1}
0	X	$Q_{(PREVIOUS\ STATE)}$
1	0	0
1	1	1

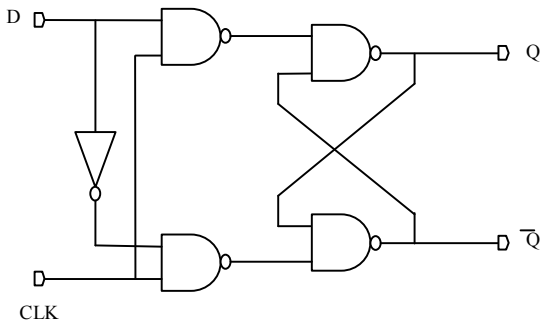

Fig. 6 (a) D Flip-Flop Circuit

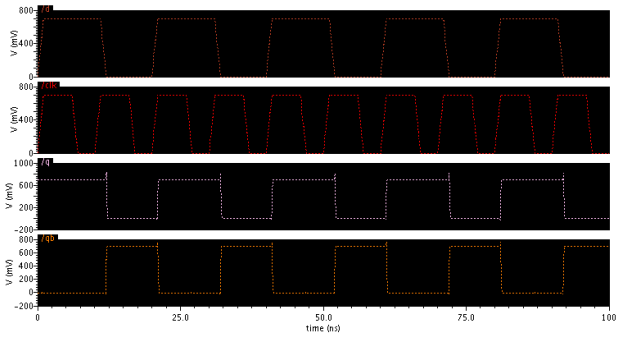

Fig. 6 (b) Output waveform of D Flip Flop

V. MEMORY CELL STRUCTURES

Memory cells are elementary unit of a complete memory. The smallest unit of memory is known as memory cell which stores a single bit. Present digital electronic circuits like microprocessors and microcontrollers utilize these memory elements to carry out the operation. Reduction in power consumption of these memory elements would lead to improvement of power efficiency of the device making them useful for low power practical circuits.

A. SRAM Cell Structure

Use of stacked transistors instead of single transistor would reduce leakage power in the circuit to a significant level. SRAM'S have been utilized in various electronic devices. Improvement in SRAM cell thus becomes an important objective in terms of speed and power consumption [11]. Reduction in leakage current would result in significant power consumption [12]. The leakage power of stacked SRAM is 5.09pw is less than the leakage power of conventional SRAM i.e. 5.20pw. The paper here would now describe the reduction techniques to be applied in the conventional 6T SRAM cell to fulfill the aim of reducing leakage power. Fig. 7 (a) shows the schematic of 6T SRAM. And the output waveform of 6T SRAM has shown in Fig. 7 (b).

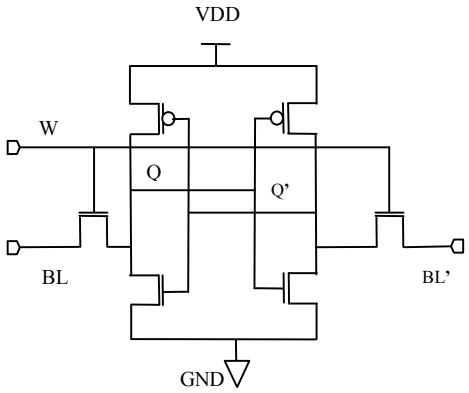

Fig. 7 (a) Conventional 6T SRAM Cell

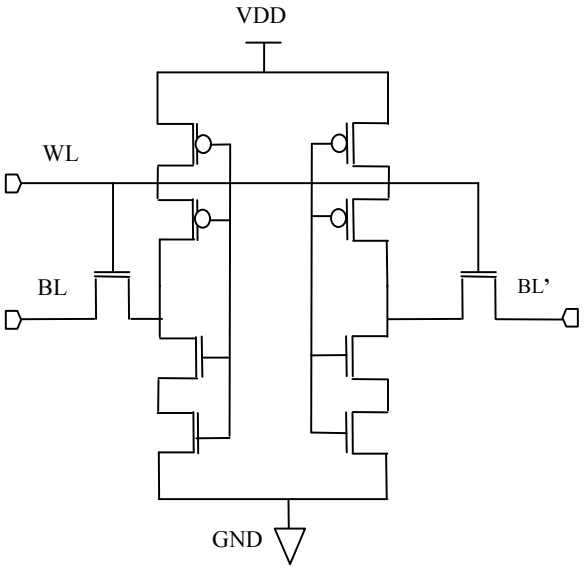

Fig. 7 (b) Stacked 6T SRAM Cell

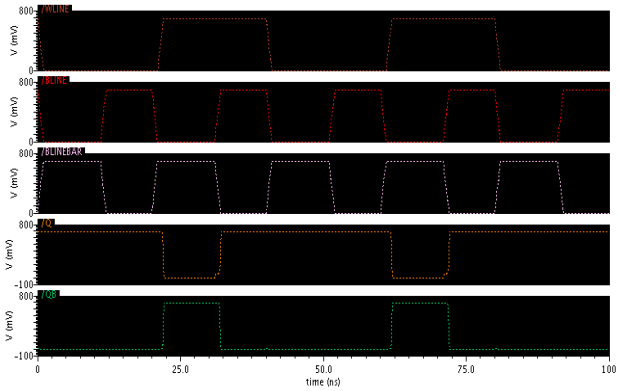

Fig. 7 (c) Output waveform of 6T SRAM

VI. Simulation and Result

TABLE VII
CALCULATION RESULTS FOR LEAKAGE POWER IN BASIC GATES TRUTH

S.No.	Basic Gate	Conventional (pW)	With Stack (pW)
1	INVERTER	0.57	0.52
2	AND	1.28	0.94
3	OR	2.87	1.14
4	XOR	1.97	1.62

TABLE VIII
CALCULATION RESULTS FOR LEAKAGE POWER IN COMBINATIONAL, SEQUENTIAL AND MEMORY CELL STRUCTURE

S.No.	Gate	Conventional (pW)	With Stack (pW)
1	FULL ADDER	2.31	1.81
2	D FLIP FLOP	2.07	2.06
3	6T SRAM	5.20	5.09

VII. Conclusion

It is observed that the leakage power of the digital circuits reduced by using the stacking technique. Thus it is easy to compare the Reduction in leakage power in conventional circuits and logic circuits designed using stacking technique such as combinational circuits, sequential circuits and memory cell structure. The complete observed result has been simulated on specter at 45nm technology.

Acknowledgment

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Pradeep Kumar Sharma (M'24) was born on 28th August 1988. He has completed his Bachelor of Engineering from B.V.M. College of Technology and Management, Gwalior. He joined M Tech VLSI with ITM Universe Gwalior, India. His major field of interest is Low power VLSI design.

Bhanupriya Bhargava (F'22) was born on 25th June 1990. She has completed his bachelor of Engineering from MITS, Gwalior, India. She joined M Tech VLSI with ITM Universe, Gwalior, India. Her major field of interest is Low power VLSI design.

Shyam Akashe (M'36) was born on 22nd May 1976. He received his M Tech from ITM, Gwalior in the year 2006. The author is pursuing Ph. D from Thapar University, Patiala, India on the topic Low Power Memory Cell Design. The Author's major fields of study are Low power VLSI design, VLSI signal processing FPGA design and communication system.

He is working as Associate Professor in Electronics and Instrumentation Engineering Department of institute of Technology and Management, Gwalior, India. His important research publications are; Implementation of technology scaling on leakage reduction technique using cadence tool with 45nm technology, IEEE 2011; High density and low leakage current based 5T SRAM cell using 45nm technology, IEEE 2011; Multi Vt 7T SRAM cell for high speed application at 45nm technology, IEEE 2011.