Charting a New Era in Chip Design: SiPearl's Collaborative Drive Towards European Microprocessor Sovereignty

Best practice category: New impetus for chip design

Stakeholder group: SMEs and start-ups

Value chain position: Chip design

General Information

SiPearl is a private company created by Philippe Notton in June 2019 and headquartered in France (Maisons-Laffitte), with subsidiaries in Germany (Duisburg) and Spain (Barcelona). SiPearl was established to bring to life the European Processor Initiative (EPI) project, which focuses on deploying high-performance and low-power microprocessor technologies in Europe. SiPearl is supported by the EU through multiple the Horizon 2020 program, as well as funds from the European Innovation Council, and participates in EU-funded consortia like the European High Performance Computing Joint Undertaking (EuroHPC JU) to make European supercomputers with exascale power a reality. SiPearl is designing and will bring to market the European microprocessor that will help Europe's supercomputers to achieve exascale power.

SiPearl is highlighted here for providing a Best Practice in the New impetus for chip design category for its collaborative work with local and global industrial, academic and research partners to advance Europe's high performance and low power microprocessor technologies.

Activities and best practices

SiPearl contributes to 8 European and 2 regional projects which cover areas that range from HPC applications, cloud server infrastructure, energy and performance optimisation or exascale biomolecule simulations. Importantly, as the driver behind EPI, the company works through close collaboration with 27 partners from the EPI consortium (including the scientific community, supercomputing centres and industry leaders in the IT, electronics and automotive sectors) to further the Initiative's goals.

- As part of the EuroHPC JU, SiPearl will provide its general purpose processor to JUNIPER, the first European exascale supercomputer. JUPITER will be the first European system capable of one exaflop (one billion billion calculations per second) and will be installed at the campus of the Forschungszentrum Jülich research institute in Jülich (Germany).

- As part of Riser, SiPearl will help develop the first all-European RISC-V cloud server infrastructure. This will leverage and validate open hardware high-speed interfaces in a novel, energy-efficient cloud architecture. Riser will combine a fully-featured operating system environment and runtime system, thus enabling the integration of low-power components, including RISC-V processor chips from the EPI and European PILOT projects. By relying on RISC-V's open standards and integrating the results of other EU-funded projects, Riser fits seamlessly into the chip landscape and enables the consolidation of multiple research streams.
- With OpenCUBE, Si Pearl and participating partners (Technical University Munich, Semidynamics, ECMWF and Hewlett Packard Enterprise) are building a full-stack solution of a validated European cloud computing blueprint that will be deployed on European hardware infrastructure. OpenCUBE's work focuses on developing a custom cloud installation with the guarantee that an entirely European solution can be deployed with reproducible effects and can provide a solid basis for the European cloud services, research, and commercial deployments. To remain competitive for the European Green Deal, OpenCUBE is designed to make energy awareness a core feature at all levels of the stack.

As part of the Helios project, SiPearl aims to develop a next-generation platform that will reduce the development time and cost of microprocessor design. Launched in July 2022 as part of the European Innovation Council's Accelerator program, Helios is working on the development of the next-generation HELIOS platform to reduce the cost and time needed to develop new chip designs. Overall, the project aims to facilitate the design of high-end microprocessors to strengthen Europe's chip sovereignty.

Challenges addressed with this practice

SiPearl is providing new impetus for chip design through its broad engagement in EU-funded consortia and projects, and active pursuit of the most efficient design routes. Moreover, the company is contributing greatly to the reduction of the EU's chip design deficiencies by harnessing the collaborative nature of open source whenever possible. Its contributions to powering the homegrown cloud and HPC infrastructure allow for strengthening of Europe's strategic autonomy in the semiconductor space.