World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:3, No:4, 2009

Active Power Filter dimensioning Using a Hysteresis Current Controller

Tarek A. Kasmieh, Hassan S. Omran

***Abstract*—**This paper aims to give a full study of the dynamic behavior of a mono-phase active power filter. First, the principle of the parallel active power filter will be introduced. Then, a dimensioning procedure for all its components will be explained in detail, such as the input filter, the current and voltage controllers. This active power filter is simulated using OrCAD program showing the validity of the theoretical study.

***Keywords*—**Active power filter, Power Quality, Hysteresis current controller.

I. Introduction

ELECTRICAL loads are becoming nonlinear in industry, household applications and in other sectors; this makes the phenomenon of power networks harmonic distortion a problem with increasing importance. These loads absorb nonlinear currents and distort the sinusoidal voltage wave form. Harmonics of the electrical network voltage and current have many harmful effects: they may disturb control signals and data transmission lines, they may damage power factor correction capacitors, electrical motors and transformers, and they also cause power lines and electrical devices overheating.

Traditional solutions have been adopted and implemented for long time like passive filters, anti-harmonic reactors and resonant shunt filters, [1]. Although these solutions where effective in reducing harmonics, they still have limits and disadvantages. They are not able to eliminate all harmonics and they usually have big size and high cost,[2].

Due to the fast progress in semiconductors and power converters industry, it became possible to manufacture devices that can eliminate the disturbances at the point of the coupling. The main two structures of these devices are the active power filters and the unity power factor rectifiers, [3].

The paper focuses on a special structure of the active power filter called parallel active power filter, Fig. 1.

T.A. Kasmieh is with the Higher Institute for Applied Sciences and Technology (HIAST). He is now the head of the Electronic and Mechanical Department, HIAST, Damascus, Syria, P.O 60318. Tel: +963 11 311 23 42. Fax: +963 11 223 77 10. Email: tkasmieh@netcourrier.com.

H.S. Omran is with the Higher Institute for Applied Sciences and Technology (HIAST). He is an engineer with the Electronic and Mechanical Department, HIAST, Damascus, Syria, P.O 31983. Tel: +963 11 512 46 39. Fax: +963 11 223 77 10. Email: hassan.samir.omran@gmail.com.

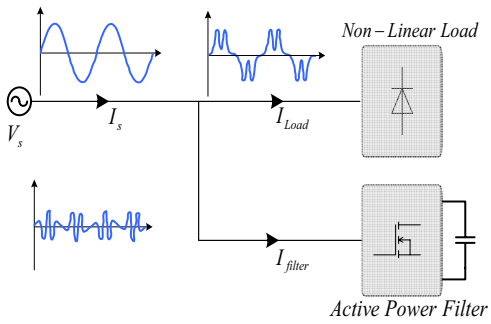

Fig. 1: Parallel active power filter: harmonic compensation principle.

II. Parallel Active power filter theoretical study

A. The Structure:

Fig. 2 shows the structure of the studied filter. It mainly consists of a 4-quadrant chopper that permits all energy transfer between storage capacitor and power network. The passive input filter absorbs the high frequency harmonics of the controlled current $I_{rectifier}$ caused by the chopping. The control block regulates the storage capacitor dc voltage, and controls the filter input current that compensates the loads harmonics.

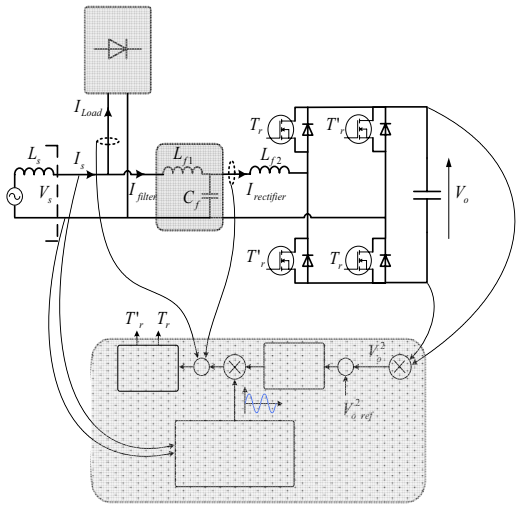

Fig. 2: Mono-phase parallel active power filter structure

B. The input passive filter:

The objective of the input passive filter is to eliminate the high order harmonics of the active filter current caused by the chopping, so that it will only contain the low order harmonics of the controlled current $I_{rectifier}$ as shown in Fig. 3.

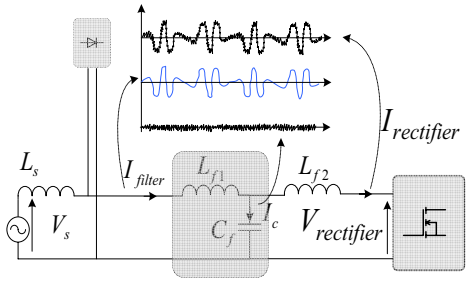

Fig. 3: Input passive filter currents

In practice, the network inductance Ls is very small. The equivalent circuits for the input passive filter from the rectifier side, and from the network side are shown on Fig. 4: (a) and (b) respectively.

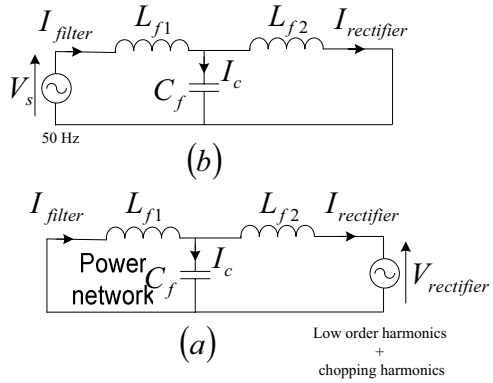

Fig. 4: Input passive filter equivalent circuits

The value of L_{f2} can be calculated according to the desired dynamic behavior of the current controller. The L_{f1} and C_f dimensions can be calculated to satisfy the waveforms presented in Fig. 3.

First, from Fig. 4, circuit (a) the ratio:

$$\frac{I_{filter}(p)}{I_c(p)} = \frac{1}{p^2 C_f L_{f1}}$$

should be as high as possible for the main frequency f_0 and all non-linear load harmonics, and as low as possible for the chopping frequency. This means that the frequency $f_{c1} = 1/2\pi\sqrt{C_f L_{f1}}$ must be placed between the low order harmonics and the chopping frequency, Fig. 5. Thus, the low order harmonic currents pass through L_{f1} and the chopping frequency current passes through the capacitor C_f.

From the other hand, Fig. 4 circuit (b), the ratio:

$$\frac{I_{rectifier}(p)}{I_c(p)} = \frac{1}{p^2 C_f L_{f2}}$$

should be as high as possible for the main frequency f_0, so that no reactive current passes through the capacitor C_f. This can be achieved by placing the frequency $f_{c2} = 1/2\pi\sqrt{C_f L_{f2}}$ far enough from the main frequency, Fig. 5.

The resonance frequency that may cause high amplitudes for input and output currents should be taken into account when dimensioning the input passive filter. The expression of resonance frequency for these two currents is:

$$f_{resonance} = \frac{1}{2\pi\sqrt{C_f.(L_{f1}//L_{f2})}}$$

$f_{resonance}$ should be placed far from $V_{rectifier}$ low harmonics frequencies and chopping frequency.

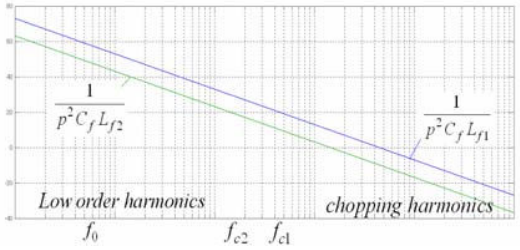

Fig. 5: The passive filter currents ratios

C. The Voltage controller:

It is very important to do a closed loop for the capacitor voltage. This will help compensating any active power transferred from the active filter capacitor to the load during a sudden change in the load.

The dynamic behavior of the capacitor voltage can easily be modeled, assuming that the current is controlled and the changes of the output voltage are very slow comparing to T_0, where T_0 is the period of the power network voltage. Taking into account the previous conditions:

$$p_{in}(t) \cong p_{out}(t)$$

where $P_{in}(t)$ is the average power absorbed from the active power filter, and $P_{out}(t)$ is the capacitor average power.

Considering $I(t)$ is the **amplitude** of the rectifier **active** current, V_{sM} is the amplitude of input voltage, and $\omega_0 = 2\pi / T_0$:

$$p_{in}(t) = \frac{1}{T_0}\int_{T_0} V_{sM}.I(t)\sin^2(\omega_0\tau).d\tau = \frac{V_{sM}.I(t)}{2}$$

$$p_{out}(t) = C_o.V_0.\frac{dV_o(t)}{dt}$$

In order to obtain a linear transfer function we suppose the variable $Y(t) = V_o^2(t)$. This leads to:

$$\frac{y(p)}{i(p)} = \frac{V_{sM}}{C_o p}$$

Fig. 6 shows the control closed loop schematic using an IP controller; the following second order system can be obtained:

$$\frac{y(p)}{y_{ref}(p)} = \frac{\omega_n^2}{\omega_n^2 + 2\xi\omega_n p + p^2}$$

by choosing $k_p = \frac{2.\xi.\omega_n.C_o}{V_{sM}}$ and $k_i = \frac{\omega_n}{2.\xi}$.

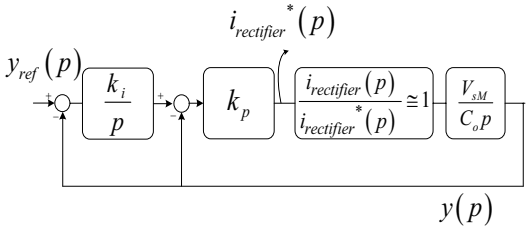

Fig. 6: the voltage IP controller

D. The current controller:

The studied controller is a non-linear hysteresis controller. The hysteresis control strategy aims to keep the controlled current inside a defined rejoin around the desired reference current, as in Fig. 7. The status of the switches is determined according to the error. When the current is increasing and the error exceeds a certain positive value, the status of the switches changes and the current begins to decrease until the error reaches a certain negative value, then the switches status changes again.

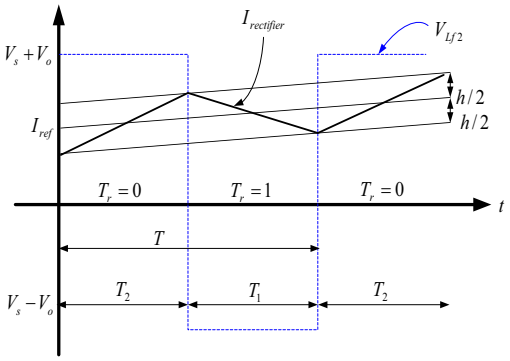

Fig. 7: The hysteresis method

It is very important to calculate the minimum and the maximum chopping frequencies to avoid the resonance explained before, and to limit the rectifier losses caused by the chopping. To do the calculation, a linear variation for the current reference during a chopping period is considered. From Fig. 7:

$$T_2 = \frac{h}{\frac{V_s + V_o}{L_{f2}} - \varepsilon}$$

and $$T_1 = \frac{h}{\varepsilon - \frac{V_s - V_o}{L_{f2}}}$$

where ε is the slope of the current reference. The expression of the chopping frequency is then:

$$f = \frac{1}{T_1 + T_2} = \frac{\left(V_o^2 - V_s^2\right) + 2\varepsilon V_s L_{f2} - \varepsilon^2 L_{f2}^2}{2V_o h L_{f2}}$$

The minimum and the maximum chopping frequencies expressions for a given slope ε are:

$$f_{\min} = \frac{\left(V_o^2 - V_{sM}^2\right) - 2|\varepsilon| V_{sM} L_{f2} - \varepsilon^2 L_{f2}^2}{2V_o h L_{f2}}$$

$$f_{\max} = \frac{V_o}{2hL_{f2}}$$

It is obvious that the maximum chopping frequency is independent of the slope ε.

Fig. 8 shows how the chopping frequency varies with time for several slope values.

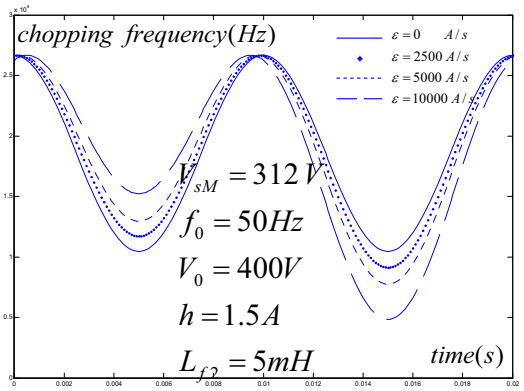

Fig. 8: Chopping frequency variations

For a known ε according to the load, and for desired f_{min} and f_{max}:

$$L_{f2} = \frac{V_o\sqrt{1 - \frac{f_{\min}}{f_{\max}}} - V_{sM}}{\varepsilon}$$

$$h = \frac{\varepsilon V_o}{2f_{\max}\left(V_o\sqrt{1 - \frac{f_{\min}}{f_{\max}}} - V_{sM}\right)}$$

III. Simulation Results

The purpose of the simulation is to validate the results of the theoretical study presented previously, and to explain the designing procedure for dimensioning the active power filter components. The simulation is done using OrCAD.

The simulation is done for mains maximum voltage V_{sM}=312(V), and a rectifier storage capacitor C_o=10(mF). The closed loop voltage reference is V_o=400(V).

The maximum linear variation of the controlled current is considered to be *30(A)* during *1(ms)*, this is equivalent to a slope of ε *=30,000(A/sec).*

The value of the inductor L_{f2} determines the active power filter reference current tracking capability. The faster the changes of the current to be compensated, the smaller the value of the inductance. The values of h and L_{f2} can be calculated from their expressions, for f_{min}*=15(KHz)* and f_{max}*=78(KHz)*:

L_{f2}*=1.6(mH),* and *h=1.6(A).*

From the expression of f_{c2}, the frequency value f_{c2}*=2.5(KHz)* is chosen to calculate C_f: C_f*=2.5(uF)*. Similarly, from the expression of f_{c1}, and by choosing f_{c1}*=7(KHz)*, we find L_{f1}*=0.2(mH)*. The resonance frequency is $f_{resonance}$*=7.4(KHz)* which is far from the minimum chopping frequency f_{min}.

For the voltage controller, the gains are calculated for ω_n*=10 (rad/sec)* and ξ=0.7: K_p*=4.5*$^{-4}$ and K_i*=7.14*.

A simulation is made using the previous calculated parameters. Fig. 9 shows the power network current and the network voltage. The currents of the non-linear load and of the active filter are shown in Fig. 10.

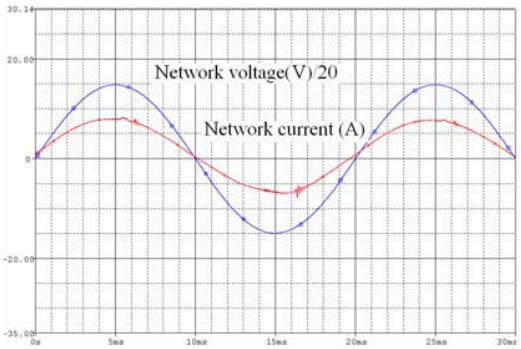

Fig. 9: Dynamic behavior of the active power filter

In order to verify the functionality of the passive filter, Fig. 11 shows the controlled current of L_{f2} and the filtered current of L_{f1}, which is the active power filter current.

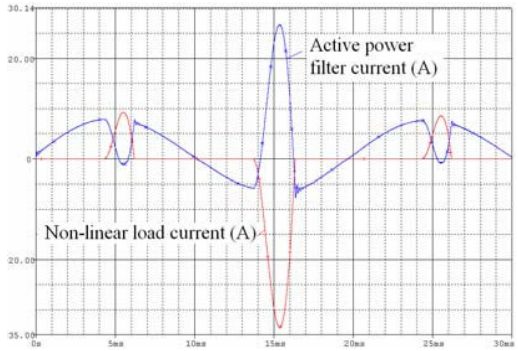

Fig. 10: Non-linear load current and active filter current

The ripples in the zoomed area happen when the frequency is near to f_{min}*=15(KHz)*. This can be explained from fig. 5. In fact, harmonics are more attenuated for high chopping frequencies.

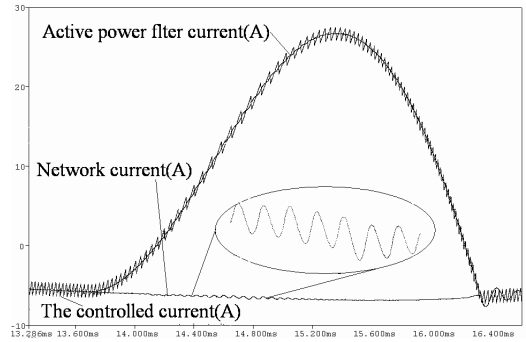

Fig. 11: The behavior of the passive filter

By doing a spectrum analysis of the controlled current signal (Fig. 12), the chopping frequency variations are found. In addition to the low order harmonics, it can be noticed that the chopping frequencies are in the desired range between f_{min} and f_{max}.

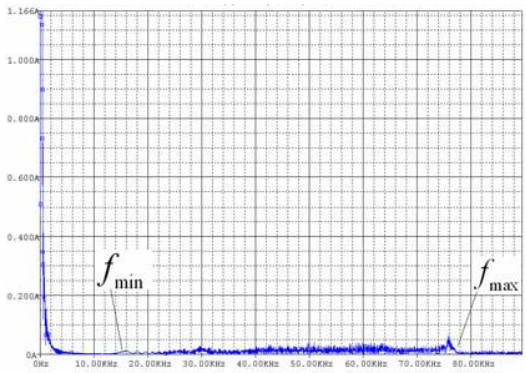

Fig. 12: Spectrum analysis of the controlled current

IV. Conclusion

This paper presented a full study of a mono-phase active power filter. A designing procedure to dimension all the components of the active filter was proposed. The theoretical part showed the chopping frequency borders for a hysteresis current controller. This helps to avoid resonance problems and high power losses in the rectifier. The simulation permitted to validate the theoretical study. It showed the good dynamic behavior of the active filter when respecting the presented designing procedure.

References

[1] J.Delaballe. EMC: electromagnetic compatibility. Cahier Technique no 149. December 2001.

[2] C.Collomet, J.M.Lupin, J.Sshonek. Harmonic disturbances in networks, and their treatment. Cahier Technique no 152. December 1999.

[3] R.M.Duke and S.D.Round. The steady-state performance of a controlled current active filter. IEEE Trans. Po r Electronics, Vol. 8, no 3, pp 140. April 1993.
[4] J.Nastran, R.Cajhen, M.Seliger, and P.Jereb. Active power filter for nonlinear ac loads. IEEE Trans. PE, Vol. 9, no 1, pp 92. January 1994.
[5] E.Bettega, J-N. Fiorina Active harmonic conditioners and unity power factor, Cahier Technique no 183. June 1999.E.Bettega, J-N. Fiorina Active harmonic conditioners and unity power factor, Cahier Technique no 183. June 1999.