A Beyond 100 Gbps Polymer Microwave Fiber Communication Link at D-band

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***Abstract*—A D-band (110-170 GHz) ultra high data rate link is presented and characterized. The circuits are realized in a commercial 130 nm silicon germanium (SiGe) BiCMOS process. The 3-dB bandwidth for both transmitter (Tx) and receiver (Rx) is between 125 - 165 GHz, resulting in a 40 GHz bandwidth. The communication link has demonstrated transmissions up to 102 Gbps using 8-phase shift keying (PSK) modulation over a one meter long foam-cladded polymer microwave fiber (PMF) with a bit error rate (BER) of 2.1×10^{-3}. Using direct quadrature phase shift keying (QPSK), 56 Gbps was reached with a BER $< 10^{-12}$. Total chip area for Tx and Rx combined, including pads, is 4.2 mm^2.**

***Index Terms*—D-band, High datarate, I/Q, PMF, Rx, SiGe, Tx**

I. Introduction

FOLLOWING the rapid development of new commercial semiconductor processes with a maximum frequency of oscillation well above 300 GHz [1], new applications at frequencies above 100 GHz are rapidly researched and developed. Such applications include wireless backhaul [2] [3] [4], wireless access [5], radar and radiometer sensors, wireless energy distribution and harvesting, IoT etc. Several of these applications require throughput in data rate well above 10 Gbps, even up to 100 Gbps. For high data rate, long range wired communication, optical fiber communication is the leading option, but for shorter ranges like chip-to-chip or module-to-module (up to 10 meters), sub-THz communication over a plastic fiber is an interesting alternative due to its potentially low cost. Other advantages are less sensitivity to temperature variations and better mechanical ruggedness. The polymer microwave fiber (PMF) is a good candidate to fill this need, due to its low cost, flexibility and robustness. Using PMFs in combination with millimeter wave chipsets allows for larger tolerance in alignment and temperature restrictions [6].

Frequencies above 100 GHz is preferred for the signal to stay confined to the fiber and not be sensitive to bends [7]. To further improve the confinement and decrease sensitivity, foam-cladding around the fiber core can be used, it also allows the fiber to be touched without affecting the signal [8]. Work has been presented at D-band (110 - 170 GHz), showing the potential of these short range high data rate links, with data rates up to 27 Gbps over a one meter long PMF [9] [10] [11]. Over a shorter distance (5 cm), 30 Gbps has been achieved [12]. At H-band (220 - 325 GHz) 35 Gbps was demonstrated over a 30 cm dielectric waveguide [13]. In [14] longer distances (three and four meters) were demonstrated using dual-band.

In this work, a commercial 130 nm SiGe BiCMOS process is used to create a competitive high data rate communication link at D-band. Previous work achieved data rates up to 40 Gbps using 16-quadrature amplitude modulation (QAM) [15]. Development towards a wider bandwidth, more importantly covering the upper side of D-band has been a priority in this work. The upper side of D-band was prioritized due to insights gained in [16]. A 3-dB bandwidth of 40 GHz was achieved in these designs, making it possible to transfer ultra high datarates at a low modulation order. In combination with a one meter long foam-cladded PMF, it forms a link that has demonstrated data rates above 100 Gbps using 8-phase shift keying (PSK).

The paper is structured as following: a brief description of the technology and topology of the design in Sec. II, followed by presentation of the measurement results both in frequency domain and time domain in Sec. III. In Sec. IV the limitations of the system is discussed. The performance is summarized and compared with previous published results in Sec. V.

II. Technology and Circuit Design

In this work, both the transmitter (Tx) and receiver (Rx) are designed and fabricated using a 130 nm SiGe BiCMOS process (B11HFC) developed by Infineon technologies. The process features high speed npn HBTs with maximum f_t/f_{max} of 250 GHz/370 GHz [17]. The process features six metal layers to route the RF signal and DC bias. The forth layer (m4) from the bottom is used as ground, with exception of the baluns, where the bottom layer is used (m1). The stack of the B11HFC process is displayed in Fig. 1.

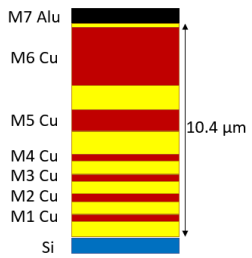

Fig. 1. The stack of the B11HFC process developed by Infineon technologies.

The block diagrams of the transmitter and receiver can be seen in Fig. 2, showing that the three main parts of the circuits are frequency multipliers, amplifiers and mixers.

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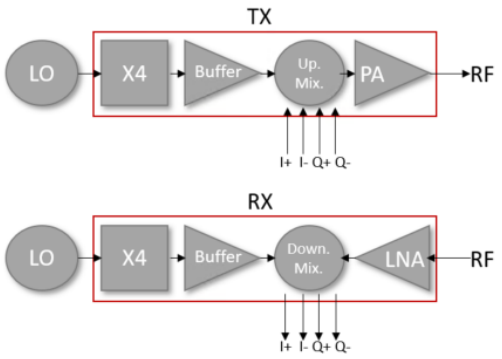

Fig. 2. Block diagram of the transmitter and receiver.

A. Wideband Amplifier Design

The power amplifiers (PA) and low noise amplifier (LNA) uses the same six-stage common emitter topology. The amplifier is designed to have a flat gain with a large bandwidth, covering the entire D-band. A simplified schematic can be seen in Fig. 3.

For the PA the transistor sizes are getting larger at each stage ranging between 4 μm and 10 μm. All transistors share the same collector supply, Vcc, which is of the order 1.8 V. The collector currents are set by a common current mirror base supply, Q4. The current consumption of the amplifier is typically between 20-40 mA depending on the required gain and output power. The amplifiers include interstage matching utilizing high-pass networks including shorted stubs (L5, L6, L8) and two capacitors (C4, C5) to get a flat gain across the entire bandwidth. For the input and output a matching, an L-type series-parallel transmission line match is used. The photo of the LNA is shown in Fig. 4. In Fig. 5, the measured S-parameters are plotted. The mid-band gain of the amplifier is 12.4 dB and the bandwidth is 125-179 GHz (54 GHz), the input/output reflection is less than -10 dB over the full band. The measured P_{sat} is 4.1 $\mathrm{dB_m}$ at 140 GHz in good agreement with the simulation when using the HICUM-model. The simulated noise figure of the amplifier is 11 dB in the mid of the D-band.

B. Frequency Multiplier Design

Both the Tx and Rx uses an off-chip local oscillator (LO) that is one forth of the carrier frequency, thus a frequency quadrupler is included in the chipsets. The quadrupler consists of two cascaded frequency doublers. In Fig. 6 the schematic of the E-band (60-90 GHz) doubler is plotted. Each doubler has an emitter coupled pair which is differentially fed. The differential signal is realized using a passive Marchand balun and the transistor pair is class-B biased. The combined waveform from the collectors is rich in the second harmonic, while the fundamental and uneven harmonics are ideally canceled out. The output from the combined collectors is fed to the emitter of a cascoded transistor to achieve a higher output power. Stub matching is implemented both at input and output.

The D-band doubler schematic is shown in Fig. 7. All transistors are internally biased through resistors and diod ladders.

The suppression of the uneven harmonics is dependent of the balun design. A conventional Marchand balun will give a good performance, but needs to be optimized to achieve full balance (phase, balance and input match). An offset of the transmission lines in the baluns were introduced to compensate the difference between in gain. The offset between the transmission lines can be seen in Fig. 8. The output branch that is bounded to the input first will get more power, which is why an offset (between the metals) is introduced. Using this method the phase offset can be preserved, while a better amplitude matching is achieved.

Simulated S21 for the baluns are plotted in Fig. 9 and Fig. 10. The baluns are designed to be as wideband as possible, to be able to cover a wide frequency range, thus enable wideband communication. The lower frequency band balun exhibit a higher insertion loss due to the difference in layout to also optimize for a smaller sized circuit. In Fig. 11 a photo of the frequency quadrupler is depicted.

The measured output power from the quadrupler is plotted in Fig. 12. The DC bias is 3 V and the current is 25 mA, giving a DC power consumption of 75 mW for the quadrupler. The input power is 3 $\mathrm{dB_m}$ to saturate the quadrupler.

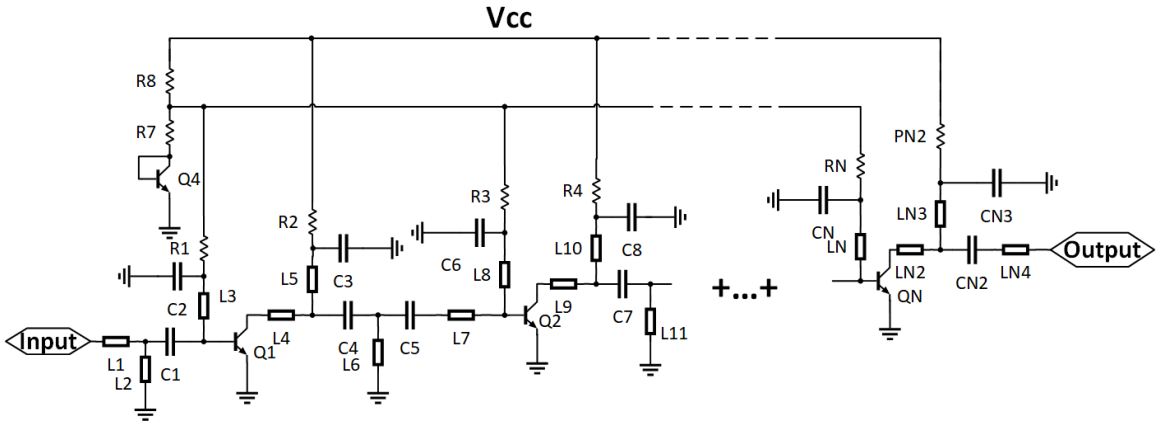

Fig. 3. Simplified schematic for the amplifiers.

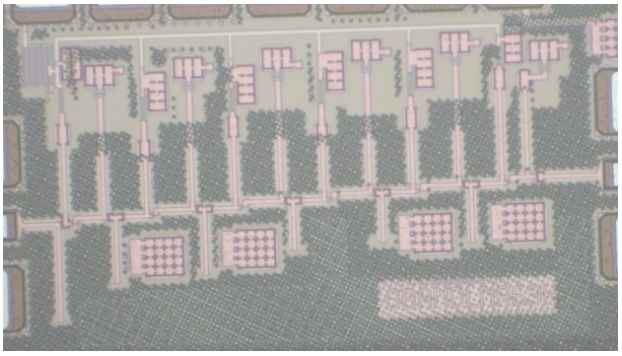

Fig. 4. A photo of the 6-stage amplifier.

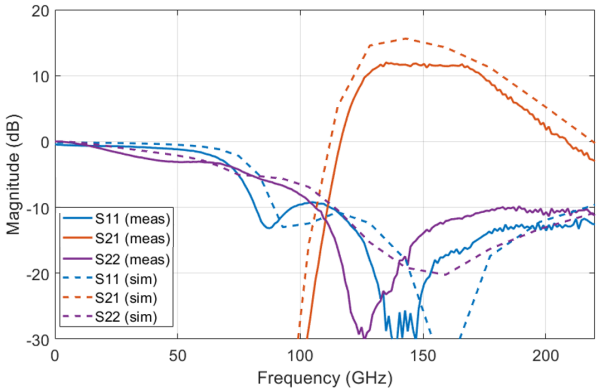

Fig. 5. Measured and simulated S-parameters.

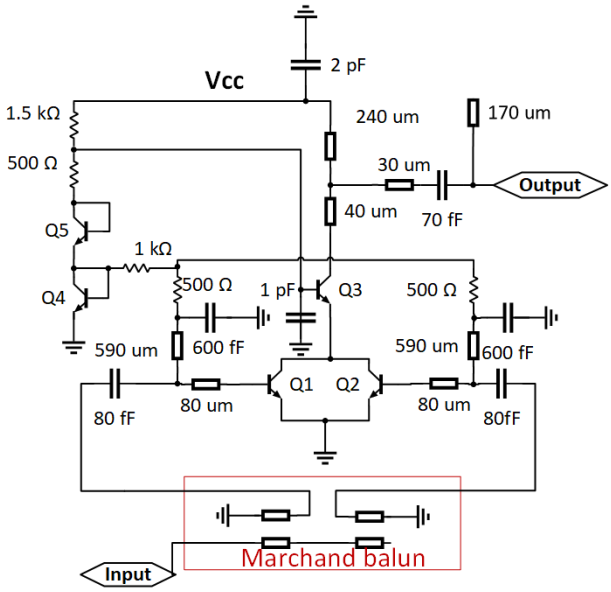

Fig. 6. Schematic of the E-band doubler. Transmission lines uses metal 6, with metal 4 as ground.

C. Mixer Design

Aiming for an IQ differential IF configuration, both the up-converter mixer and the down-converter mixer was realized with two identical double-balanced Gilbert cells.

Fig. 13 shows the schematic of the up-converter mixer. As can be seen in the Gilbert Cell 1, the differential IF input

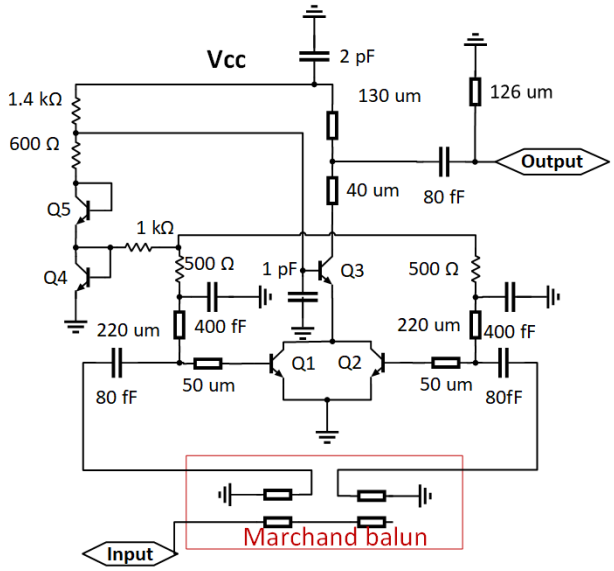

Fig. 7. Schematic of the D-band doubler. Transmission lines uses metal 6, with metal 4 as ground.

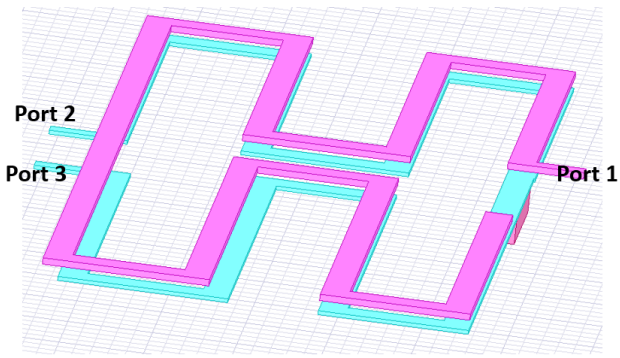

Fig. 8. The Marchand balun for the E-band doubler. The pink layer is the input layer (m6), and the turquoise layer is the output metal (m5).

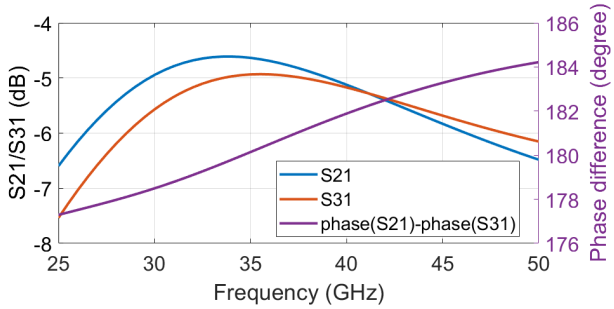

Fig. 9. Simulated S21 of the Marchand balun for the E-band doubler.

signals are fed into the bases of the lower level transistor pair Q1 and Q2 (size: 6 μm) through off-chip DC blocks, so as to operate at the frequency down to the baseband. At the LO port, the single-ended LO input signal is firstly converted into four quadrature phased signals through an on-chip Marchand balun in combined with two 90 degree 3-dB couplers, and one branch of differential LO signals are further applied to the bases of the upper level transistors Q2-Q6 (size: 2.5 μm).

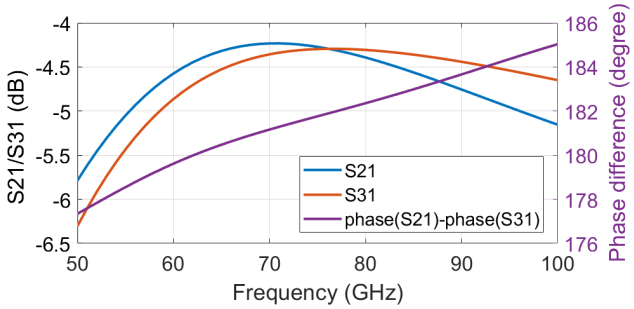

Fig. 10. Simulated S21 of the Marchand balun for the D-band doubler.

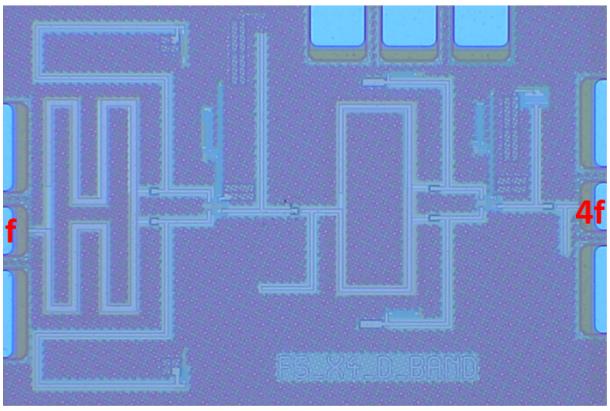

Fig. 11. A photo of the frequency quadrupler.

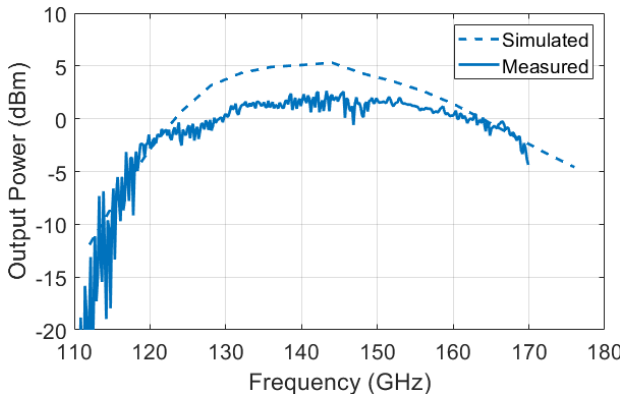

Fig. 12. Measured output power from the frequency quadrupler.

The transistor pair Q1 and Q2 work as the transconductance stages, which convert the input baseband signals at the bases into currents at the collectors. The upper level transistors Q3-Q6 operate as switches and generate mixing products of IF and LO at the collectors. The desired RF outputs will be added up through the Marchand balun, while the LO will be canceled. In order to simplify the biasing, the mixer is internally biased and controlled by the current mirror pair Q1 and Q2, while the bases of the transistors are voltage biased through the transistor diodes stack-up. The designed D-band IQ-differential up-converter mixer occupies an area of 700×650 μm^2, and the chip photo is shown in Fig. 14. With an IF input frequency of 2 GHz and an LO power of 5$\sim$7 dBm, a typical conversion gain of around -3 dB was measured for the entire D-band, as is shown in Fig. 15, while better than 20 dB side-band suppression was achieved.

The down-converter mixer shares a similar Gilbert mixer core cell as the up-converter mixer. The schematic is shown in Fig. 16. The single-ended RF input is differentially fed into the bases of the lower level transconductance stage through an on-chip Marchand balun. Considering the parasitic parameters at high frequency of RF and the linearity, an optimized transistor size of 0.22 μm$\times$4 μm is chosen for Q1 and Q2. The down-converted IF outputs are obtained through an emitter-follower stage and further optimized with the help of a series connected microstrip line TL1 and a small shunt capacitor C1. Similar like the up-converter mixer, the internal biasing network is applied to the down-converter mixer and only one external voltage bias of V_{C-MIX} is needed. The D-band IQ-differential down-converter mixer occupies an area of 700×700 μm^2, and the chip photo is shown in Fig. 17. With an LO power of 5$\sim$7 dBm, Fig. 18 shows the measured conversion gains of the LSB and USB. For the entire D-band, a typically conversion gain of 0 dB was obtained while the side-band suppression is around 15 dB.

D. Fully integrated Tx and Rx

The above presented frequency multiplier, mixers and amplifier were designed and optimized for 50 Ω port impedance to facilitate a simple matching between sub-circuits. The layout of the sub-circuits were designed to fit together, without using long transmission lines between to avoid unnecessary loss in the integrations.

The chip photo of the transmitter and receiver is shown in Fig. 19. The total chip area for Tx and Rx combined is 4.3 mm^2.

III. Measurement Results

Measurements were done both in frequency domain and in time domain as a link communication demonstration. Both were done on-wafer using Cascade probe stations and GGB picoprobes.

A. Frequency domain measurements

For the frequency domain measurements, a Keysight PNA-X (67 GHz N5247A) was used together with a VDI D-band extender WR 6.5 at the output of the Tx and as the input for the Rx. The LO was provided by a Keysight signal generator (Agilent 67 GHz PSG E8257D) which was synchronized to the PNA-X.

1) Evaluation of the Tx: The conversion gain for the transmitter was measured with an input IF power of -15 dB$_m$ and an LO power fed into the quadrupler of 4 dB$_m$. The IF was a fixed sinusoidal at 4 GHz and both the lower sideband (LSB) and the upper sideband (USB) was measured sweeping the RF frequency between 110 - 170 GHz. The single-ended IF input was split into the four channels using a commercial hybrid (Marki QH-0440)and two baluns (Marki BAL-0050). The quadrature-phase IF signals were further connected to the GSSGSSG probe through external DC blocks.

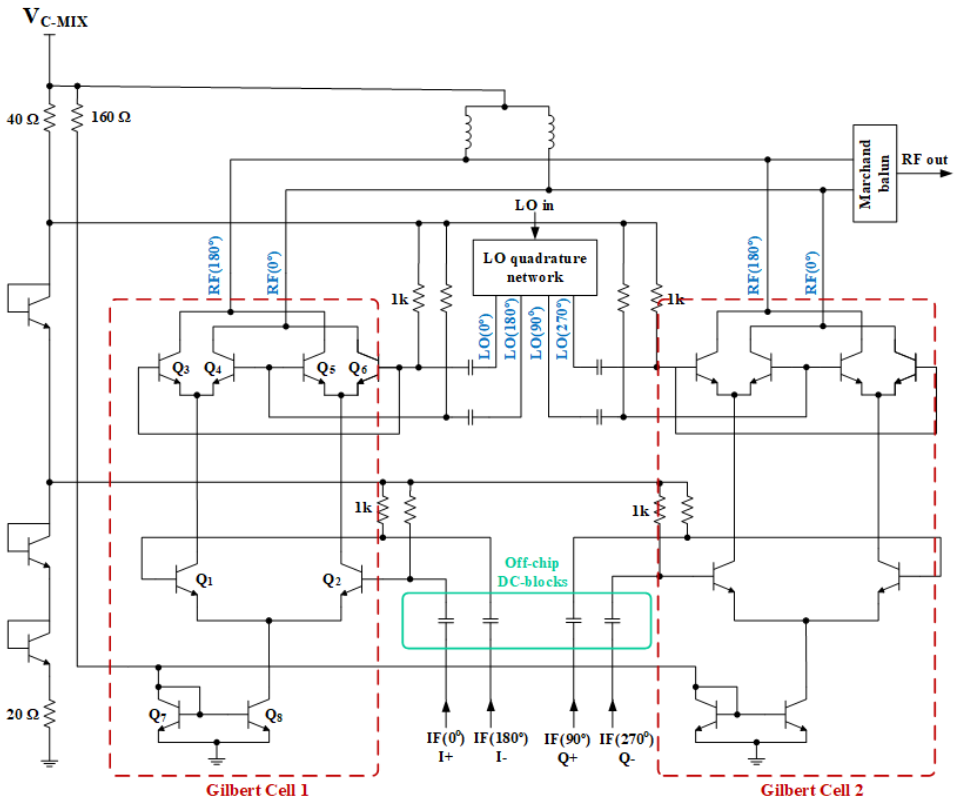

Fig. 13. Schematic of the up-converter mixer.

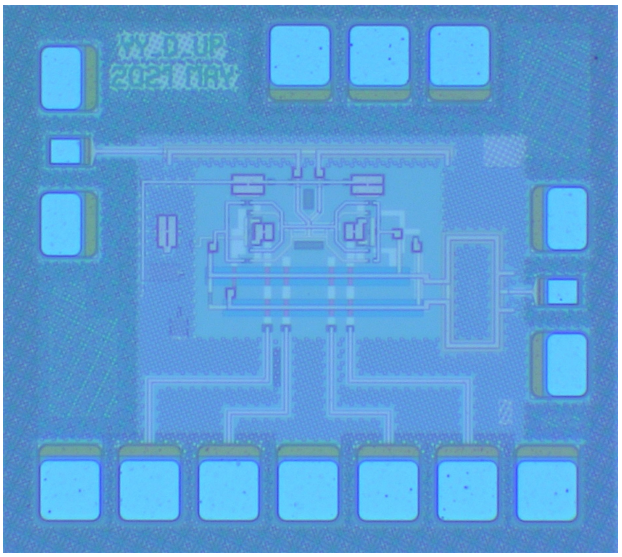

Fig. 14. Photo of the D-band up-converter mixer.

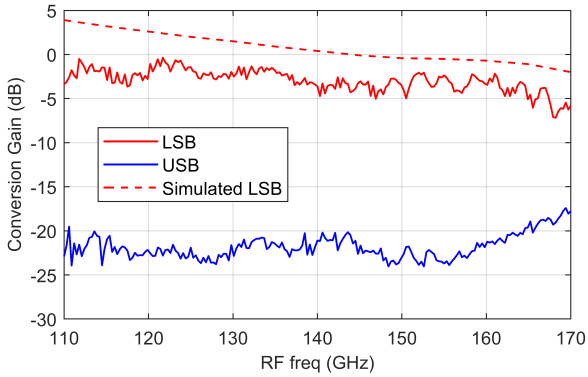

Fig. 15. Measured conversion gain of the LSB and USB versus RF frequency at fIF=2 GHz and PLO=5∼7 dBm.

As can be seen from the Fig. 20, a typical conversion gain of around 10 dB was measured between 125 - 165 GHz, which corresponds to an RF bandwidth of 40 GHz, and a sideband suppression of around 20 dB was achieved. The highest sideband suppression (25 dB) was around 152 GHz. During the link measurements direct I/Q modulation is used, but the sideband suppression is also a measure of I/Q (im-) balance. I/Q imbalance is a result of either an amplitude difference between I and Q, or a phase difference that is deviating from the ideal 90 degrees. The result is a distortion of the signal and can be measured in a signal-to-distortion ratio (SDR). SDR is given by;

$$\mathrm{SDR} = 10\log\left(\frac{1+\epsilon_R^2+\epsilon_R^2\tan^2(\Delta\phi_R)}{\epsilon_R^2+\tan^2(\Delta\phi_R)}\right) \quad (1)$$

where ϵ_R is the amplitude error and $\Delta\phi_R$ is the phase error. For an SDR above 20 dB the phase error has to be lower than 6 degrees or the amplitude error less than 10 % [18]. Known distortion can be dealt with, but it is increasingly difficult to

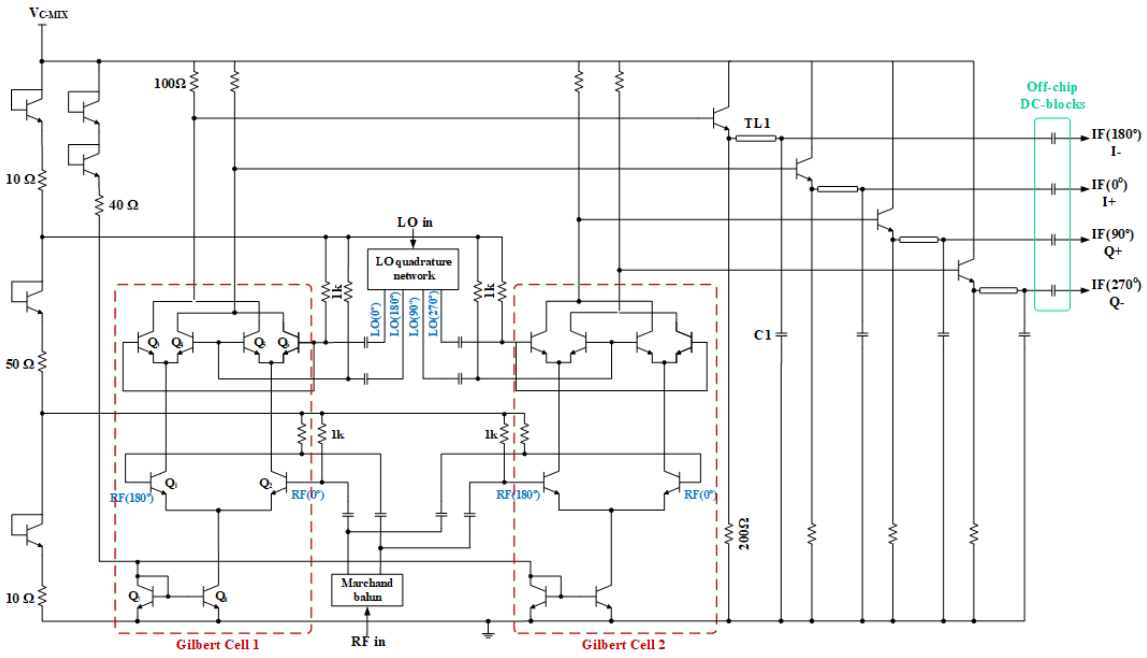

Fig. 16. Schematic of the down-converter mixer.

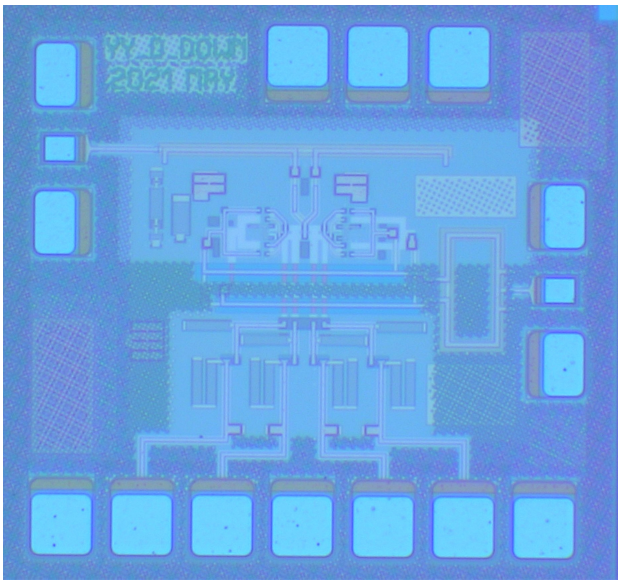

Fig. 17. Photo of the D-band down-converter mixer.

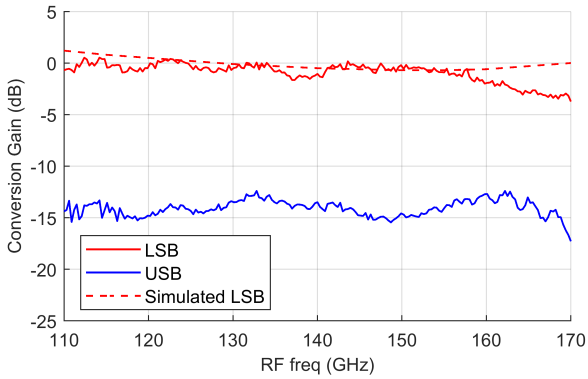

Fig. 18. Measured conversion gain of the LSB and USB versus RF frequency at fIF=2 GHz and PLO=5∼7 dBm.

implement at high data rates, in real-time, which is why it can be seen as noise in those cases.

In Fig. 21, the saturated output power of the Tx is measured using the LSB with a 4 GHz sinusoidal IF. The peak output power is 0 dB_m.

To investigate the IF bandwidth a sweep (4 GHz - 30 GHz) of the IF frequency was done for both LSB and USB, using -15 dB_m IF power and 4 dB_m LO input (to the quadrupler). The results can be found in Fig. 22. The difference in gain between 5 GHz and 20 GHz is only 4 dB, and some gain can still be seen at 30 GHz IF.

The input power at the IF port was swept using constant IF frequency (4 GHz) and RF (152 GHz). Conversion gain and RF output power is plotted in Fig. 23. To avoid compression, the input power at IF should be kept below -15 dB_m.

The output spectrum of a modulated 5 Gbd QPSK signal was captured by a Rohde & Schwarz Signal Source Analyzer (FSUP50) via an external signal analyzer mixer (SAM-170). The output spectrum is displayed in Fig. 24. The LO leakage can be seen at the center of the signal, which is a result of phase and/or amplitude mismatch when the RF output signal is combined.

2) Evaluation of the Rx: Similar measurements were done for the receiver, using two baluns and a hybrid to combine the four IF ports. With the IF frequency of 4 GHz and an input power of -20 dB_m, the measured conversion gain for both LSB and USB can be seen in Fig. 25. A conversion gain of more than 10 dB was obtained at the RF frequency range of 125-165 GHz, while the side-band suppression was typically 15

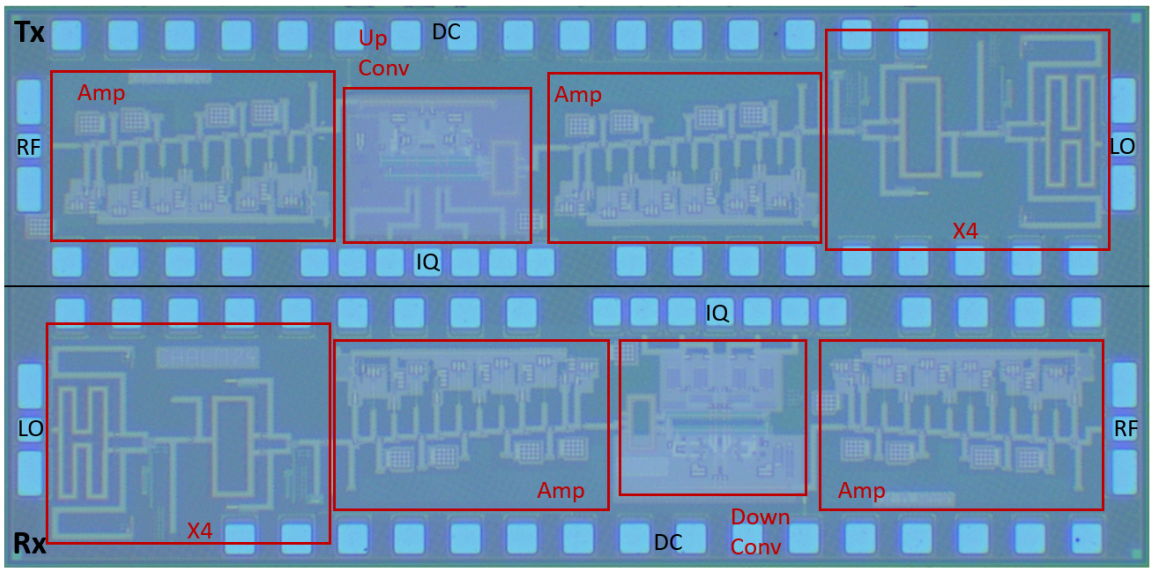

Fig. 19. Photo of the transmitter and receiver chipset. The total area for both circuits is 3 mm by 1.448 mm including the pads.

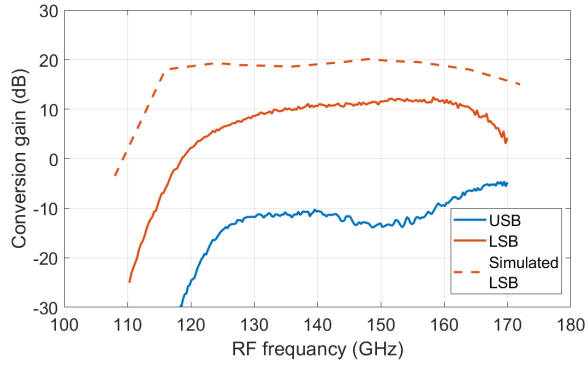

Fig. 20. Measured and simulated conversion gain for the Tx using a 4 GHz IF signal. The simulated value is about 10 dB higher than the measured value, which is in majority due to a lower conversion gain than expected in the up converter mixer.

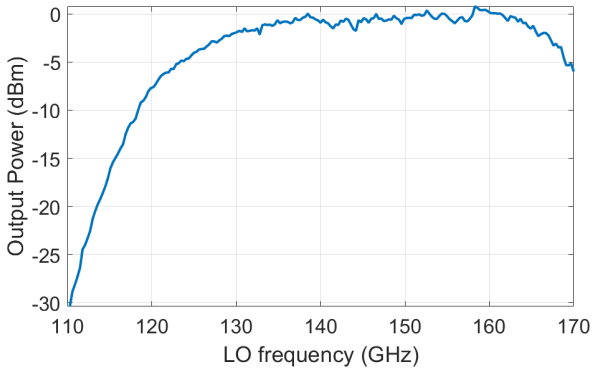

Fig. 21. Saturated output power for an RF sweep with a 4 GHz IF.

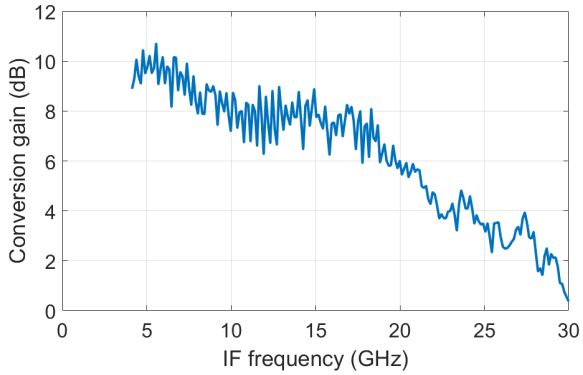

Fig. 22. IF sweep with a 152 GHz RF.

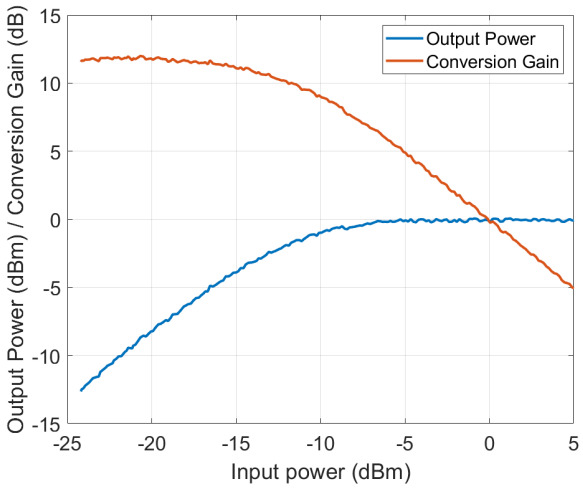

Fig. 23. IF power sweep with a 2 GHz IF at 152 GHz RF

dB, with 20 dB at most.

The IF bandwidth was measured with a fixed input RF frequency of 152 GHz. The result is plotted in Fig. 26. Compared to the Tx, the Rx has a higher gain but worse sideband suppression. It drops 10 dB in gain between 5 GHz

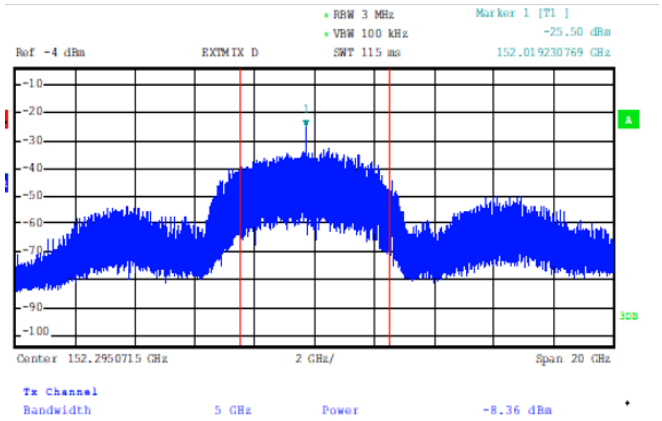

Fig. 24. Captured spectrum of the output signal from the Tx. The signal is modulated with a 5 GBd QPSK with an LO at 152 GHz.

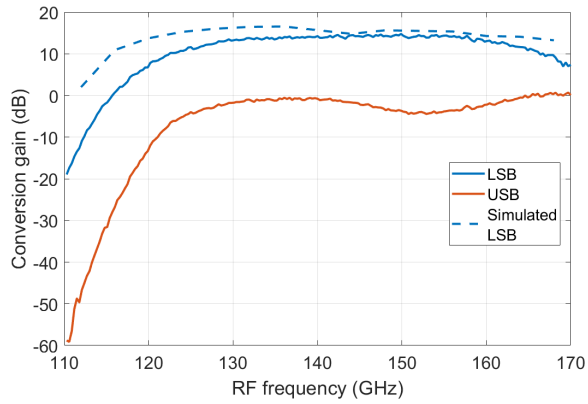

Fig. 25. Conversion gain for an RF sweep with a 4 GHz IF.

and 20 GHz, though the circuit still has some gain at 30 GHz IF.

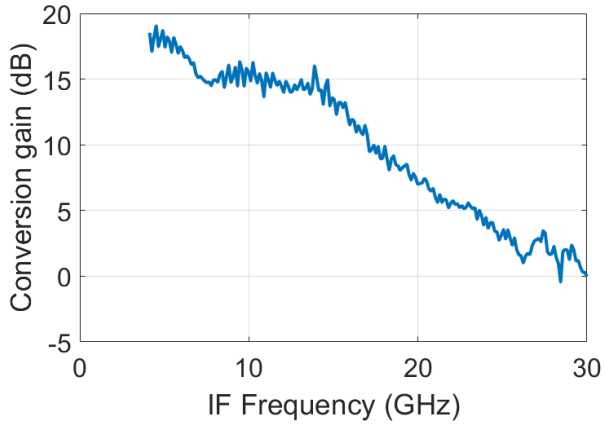

Fig. 26. IF sweep with a 152 GHz RF.

An input power sweep was done for the Rx, with a 152 GHz LO. In Fig. 27 both IF output power and conversion gain is plotted. Compression starts around -18 dB_m.

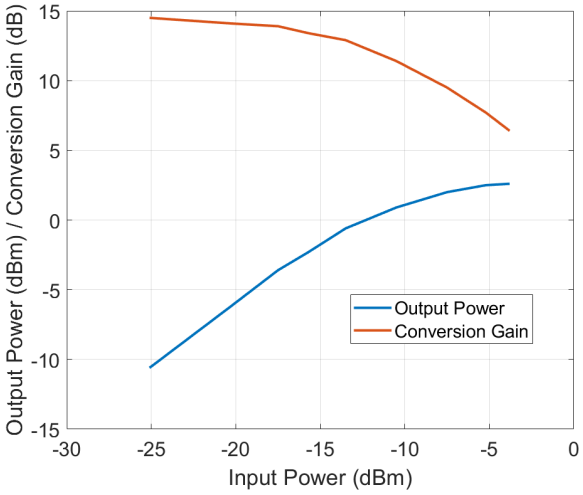

Fig. 27. RF power sweep with a 4 GHz IF at 152 GHz RF

B. Time domain measurements

The transmitter and receiver link was setup using a one meter PMF, to validate and measure the performance of the link. The PMF including transitions was provided by Huber+Suhner. The fiber has a rectangular polytetrafluoroethylene (PTFE) core with a cross section of 2.1 mm by 1.2 mm and a circular polyethylene (PE) foam cladding. The end of the fiber is cut like a taper and inserted in the waveguide adaptor.

The measured S-parameters and group delay of the fiber is plotted in Fig. 28 and Fig. 29. The measurements were done using a Keysight PNA-X (67 GHz N5247A) together with VDI extenders (WR-6.5) , and include the waveguide transitions to and from the fiber.

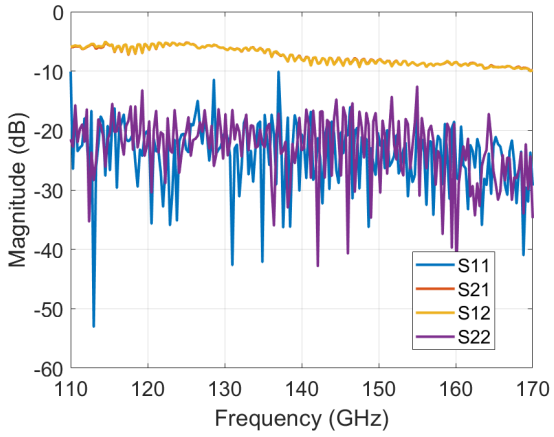

Fig. 28. Measured S-parameters of the one meter long PMF including the transitions from waveguide to fiber and fiber to waveguide.

The difference in group delay over the signal bandwidth has to be small in comparison to the symbol period in order to avoid symbol interference. Pulse shaping of the baseband signal on the transmitter side and equalization/filtering on the receiver side can be used in order to compensate for this.

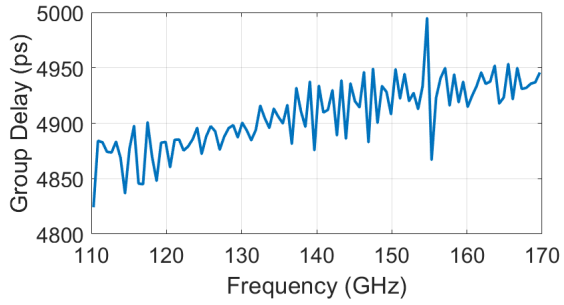

Fig. 29. Measured group delay for the fiber including waveguide transitions, for different frequencies at D-band.

Reflections and variations in Fig 28 and Fig. 29 could be due to the fact that the fiber is cut by hand.

The data input was provided by a Keysight M8195A arbitrary waveform generator (AWG), where a pseudorandom binary sequence (PRBS-10) was generated using root raised cosine pulse shaping with a roll off of 0.7. Direct I/Q modulation was used during the link measurements.

The LO was provided by a Keysight signal generator (Agilent 67 GHz PSG E8257D), which was shared by Tx and Rx using a power splitter. A Teledyne LeCroy LabMaster 10-100Zi was used to capture the output signal from the Rx. The bandwidth of the oscilloscope is 36 GHz which is smaller than the measured bandwidth of the transmitter and receiver and can be considered a limitation in this measurement setup. Fig. 30 is a block diagram of the setup.

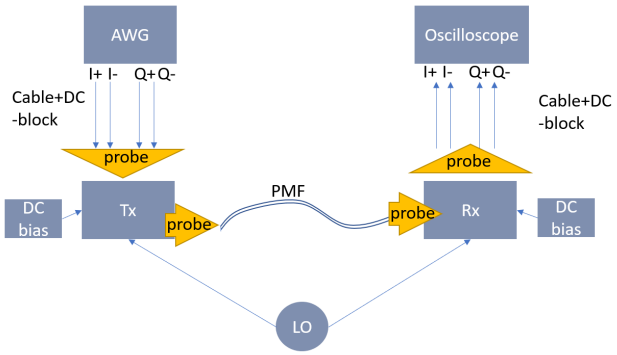

Fig. 30. A block diagram of the setup used during the link measurements.

The setup for the measurement is shown in Fig. 31. The Tx can be seen to the right which is connected to the Rx on the left. The output is then captured by the oscilloscope. Carrier frequencies between 151 GHz and 153 GHz were used during the link measurements. The DC power consumption for the Tx is 437 mW, and for the Rx it is 556 mW.

In Table I, an estimation of the power levels for the link is made. The noise floor of the 36 GHz bandwidth of the oscilloscope is approximately -68 dB_m.

Captured eye diagrams and IQ constellation for QPSK modulations can be seen in Fig. 32, 33 and 34 for data rates of 28 GBd, 34 Gbd and 40 GBd, corresponding to 56 Gbps, 68 Gbps and 80 Gbps.

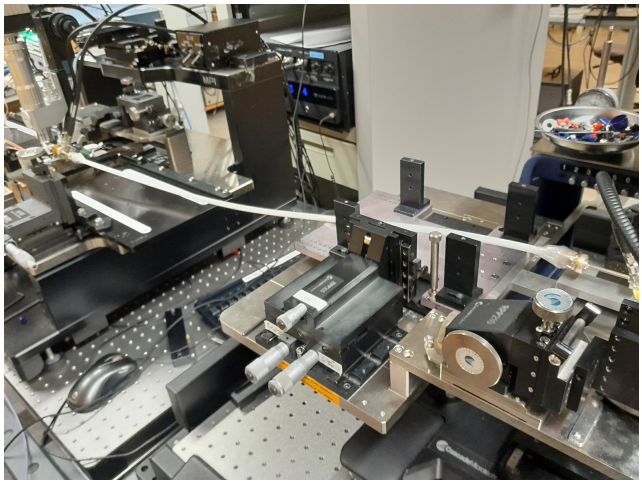

Fig. 31. Setup used during the PMF link measurements. The Tx is on the right probe station and the Rx is on the left probe station. The PMF can be seen connecting to output and input on each probe station.

TABLE I
LINK ESTIMATION

Item	Gain (dB)	Power (dB_m)	Note
AWG	-	7	I=4dbm (Vp=500mV) Q=4dBm (Vp=500mV)
Attenuator	-20	-13	SMA
Cable (including DC block)	-2	-15	Measured S-param.
Probe	-0.7	-15.7	picoprobe (40A)
Tx	+8	-7.7	Estimated from S-param.
Probe	-1.5	-9.2	picoprobe (170)
PMF (including transitions)	-7	-16.2	Measured S-param.
Probe	-1.5	-17.7	picoprobe (170)
Rx	+14	-3.7	Estimated from S-param.
Probe	-0.7	-4.4	picoprobe (40A)
Cable (including DC block)	-2	-6.4	Measured S-param.
Oscilloscope	-	-6.4	I=-9.4dbm (Vp=105mV) Q=-9.4dBm (Vp=105mV)

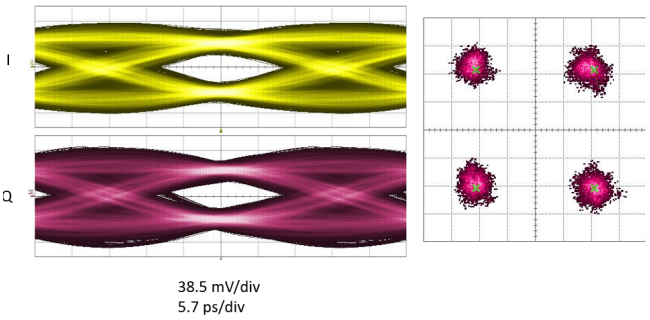

Fig. 32. 28 GBd QPSK with LO at 152 GHz and BER $< 10^{-12}$.

The measured bit error rate (BER) for different baudrates for QPSK modulation is depicted in Fig. 35.

The eye diagrams and IQ constellations for 8-PSK modulation can be seen in Fig. 36 and 37 for data rates of 26 GBd and 34 GBd, corresponding to 78 Gbps and 102 Gbps.

Transmissions with QAM-16 modulations were also tested.

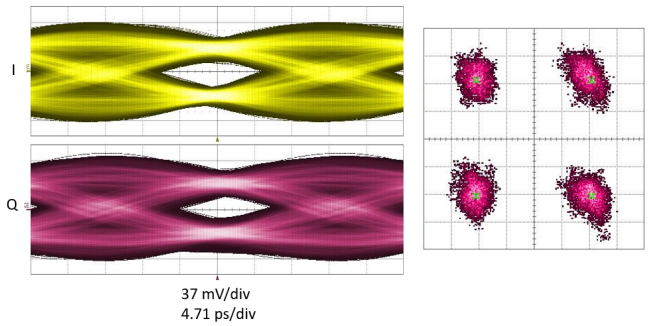

Fig. 33. 34 GBd QPSK with LO at 152 GHz and BER=2.0*10^{-8}.

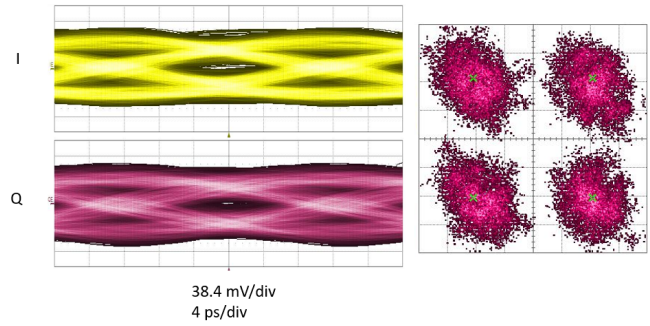

Fig. 34. 40 GBd QPSK with LO at 152 GHz and BER=9.5*10^{-4}.

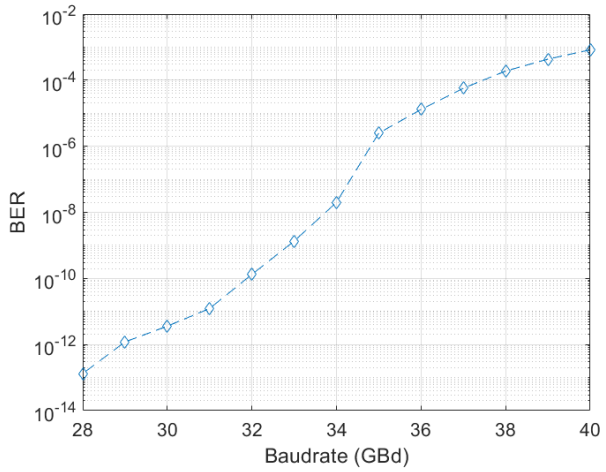

Fig. 35. BER for different baud rates for QPSK modulation.

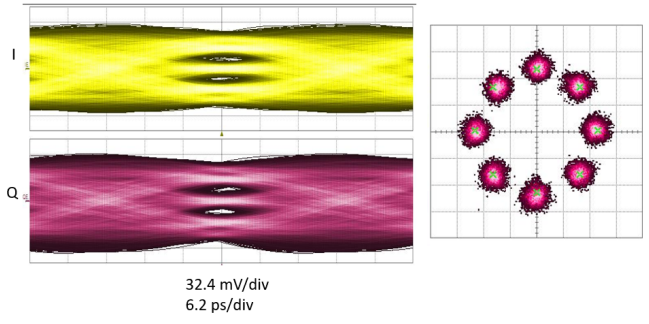

Fig. 36. 26 GBd 8-PSK with LO at 151 GHz and BER=2.9*10^{-4}.

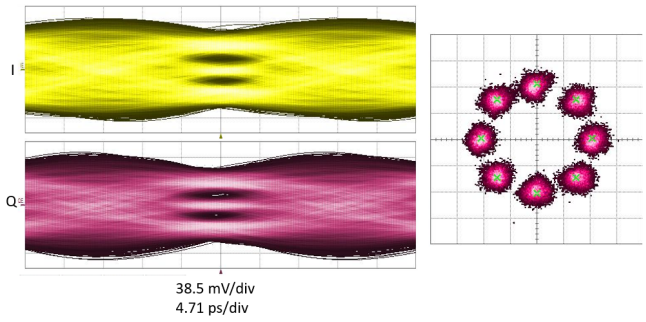

Fig. 37. 34 GBd 8-PSK with LO at 151 GHz and BER=2.1*10^{-3}.

In Fig. 38 10 GBd is transmitted corresponding to 40 Gbps.

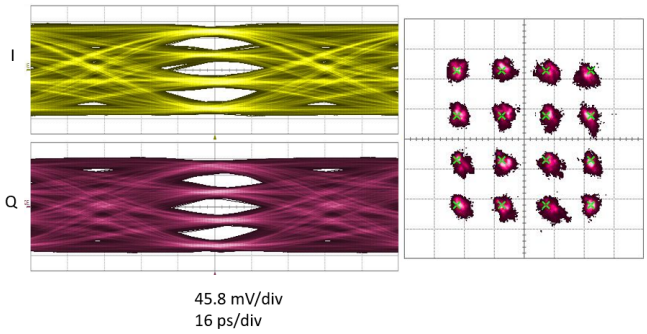

Fig. 38. 10 GBd QAM-16 with LO at 153 GHz and BER=2.4*10^{-8}.

The spectrum of the output signal from the Rx was captured by the oscilloscope. The signal was QPSK modulated with baudrates of 15, 25 and 30 Gbd. The spectras can be seen in Fig. 39. The bandwidth of the signal is less than the baudrate. The RRC pulse shaping of the signal done by the AWG is decreasing the signal bandwidth, which means the signal will be less sensitive to the dispersive effects of the PMF. It can also be seen that the noise floor is much lower than the signal power, meaning it should not impact the SNR.

Captured waveforms when only I or Q channel is used and both channels are used can be seen in Fig. 40. 10 Gbd QPSK modulated data was used and a carrier of 151 GHz. In the first case the input to the Q channel was turned off, second case I channel was turned off. It can be seen that a small part of the I channel is leaking to the Q channel and conversely. The quality of the signal is slightly degraded in both channels when they are used simultaneously.

IV. Discussion

The bandwidth of the measurement setup is a factor that cannot be neglected, but that is an ”outside the system” limitation. Thus, to increase the datarate even more in the future, a higher modulation order is the solution, which means a larger SNR is required.

The input power (≈ -17.7 dB_m) at the Rx is not enough to saturate the circuit according to Fig. 27, and verified using an attenuator after the PMF, before the Rx. The input power

to the oscilloscope is far from the noise floor (as seen in Fig. 39), eliminating that as a limitation.

In Fig. 24 some LO leakage can be noticed, which may limit the SNR, thus higher modulation orders. By adding a bias tee to the I+ and Q+ port a small voltage change (a few mV) could significantly improve the LO leakage. Fig. 41 shows the output spectrum of a 5 GHz continuous wave (CW), with 90 degree offset between channels to show sideband suppression as well, where the one on the left is without bias tee, and the one on the right is with bias tee.

Another limitation can be found in Fig. 40, where some crosstalk between the channels can be seen. This can be removed through signal processing, but it is challenging to do in real time at high datarates.

The potential of the link is clearly be seen in the large bandwidth, and further improvements can possible be made by focusing on minimizing the LO leakage and crosstalk between the channels.

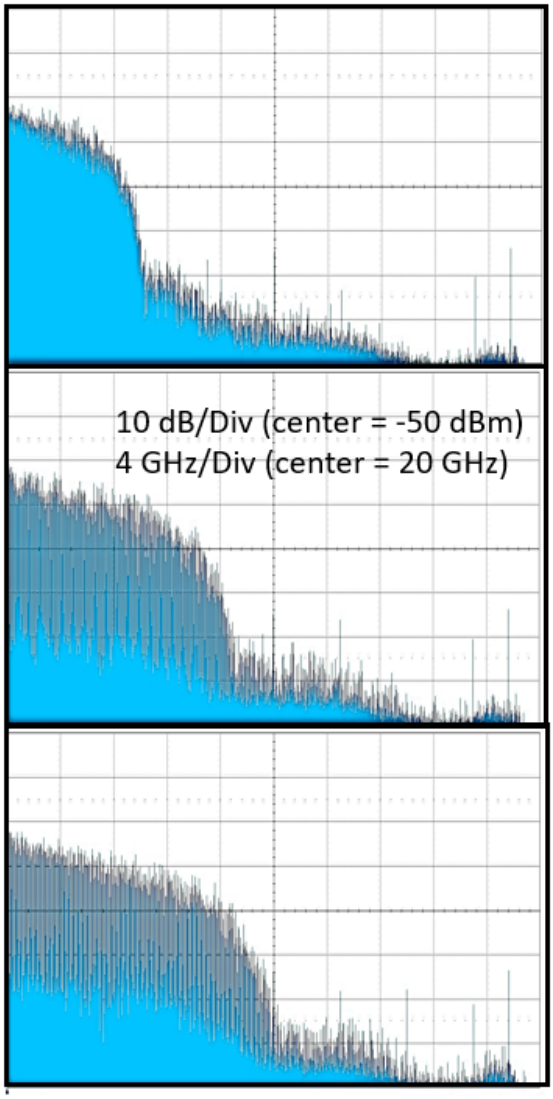

Fig. 39. Spectrum of a QPSK modulated signal received by the oscilloscope from the Rx. From the top 15 Gbd, center 25 Gbd and the bottom 30 Gbd. (LO = 151 GHz)

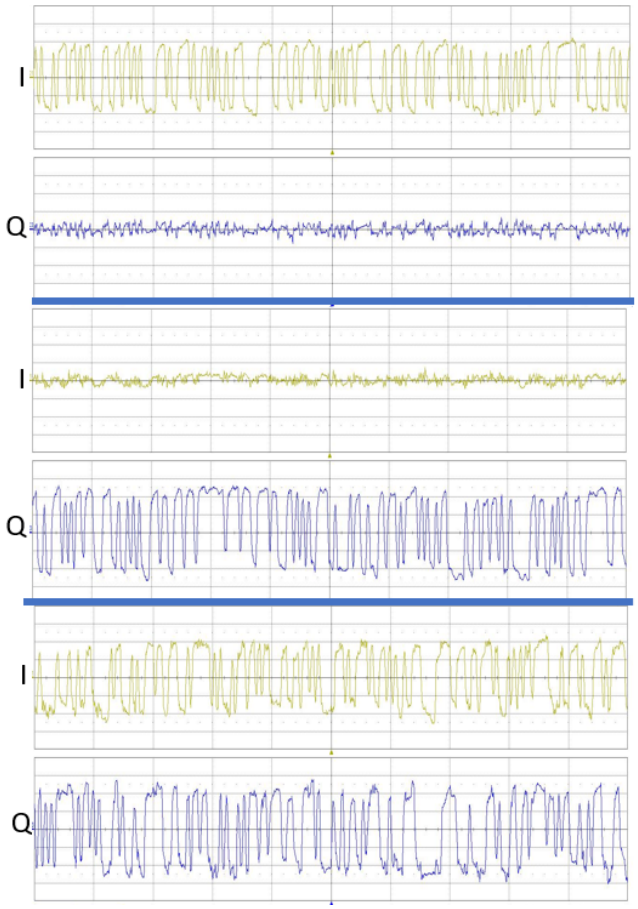

Fig. 40. Output waveform from the oscilloscope when data is only transmitted from one channel at the time in the first two cases. On top only the I channel is used, in the middle only Q channel is used, and at the bottom both channels are used. The symbolrate was 10 Gbd with a carrier of 151 GHz.

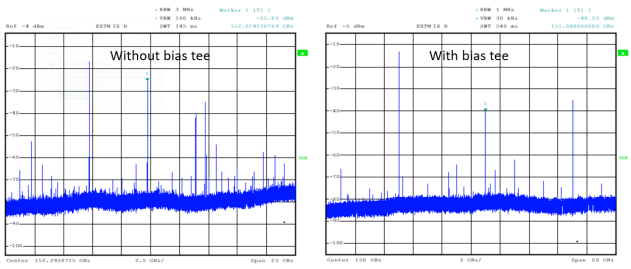

Fig. 41. 5 GHz CW with LO at 152 GHz with and without bias tee at the I+ and Q+ port.

V. Conclusion

In this work a high datarate, short range communication link has been designed in a commercial 130 nm SiGe BiCMOS process and evaluated. The link is measured to support data rates up to 102 Gbps with a BER=$2.1 * 10^{-3}$ using 8-PSK modulation and 56 Gbps with a BER$< 10^{-12}$ using QPSK modulation. The 3-dB bandwidth is 40 GHz, which is larger than the measurement setup equipment, which may add some limitations in the performance. The performance in comparison to other PMF links can be seen in Table II. It can be seen that this link has the highest datarate, more than

TABLE II
COMPARISON WITH OTHER D-BAND PMF LINKS, WITH BER $< 10^{-12}$

Reference	[9]	[10]	[11]	**[this work]**
Technology	40 nm CMOS	28 nm CMOS	28 nm CMOS	**130 nm BiCMOS**
Modulation	CP-FSK	CP-FSK	ASK	**QPSK**
Frequency (GHz)	120	140	135	**152**
Data Rate (Gbps)	17.7	12	27	**56**
Fiber Length (m)	1.0	1.0	1.0	**1.0**
Energy Eff. (pJ/bit)	4.0*	19.2	4.8	**17.7***
(*=no LO included)				
Total chip area (mm^2)	N/A	2.31	1.94	**4.2**
Peak output power (dB_m)	-1.9	6	-3	**0**

double, for these distances in this frequency range.

The chipset is designed for PMF communication, and is suitable for short distance, ultra high speed chip-to-chip or module-to-module communication, for example in-cabin vehicle communication for autonomous vehicles. It is potentially a low cost, robust solution using a commercial process.

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