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# AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

# DELIVERABLE REPORT

# MPW 28 NM

## DELIVERABLE: D11.1

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**Abstract:**

This deliverable report describes the ASICs that were fabricated in CMOS 28 nm for work package 11.2. Two prototypes containing several test circuits to explore key features of the technology were designed, fabricated and tested. A low-power ADC was studied in detail in simulation, and it should be submitted for fabrication within the 3rd quarter of 2024.

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## Delivery Slip

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## Executive summary

*Deliverable D11.1 reports the fabrication of test chips in 28 nm containing elementary test structures and fully-fledged building blocks essential for the design of detector front-end electronics. Two chips have been designed, fabricated and tested. The chips were internally reviewed before fabrication which constituted Milestone MS45.*

# 1. INTRODUCTION

There is a consensus in the detector community that 28 nm CMOS should be the reference technology node for the design of front-end electronics in coming years. This choice stems from several reasons. First, the 28 nm is the last node employing standard planar MOS devices, whereas more aggressively scaled technologies adopt FinFETs. The use of such devices entails an increased design complexity and significantly higher Non-Recurrent Engineering (NRE) costs. The 28 nm, on the other hand, is already dense enough to allow the deployment of very complex digital circuits, a fundamental aspect as the digital part is now predominant also in ASICs for detector readout. The transistor speed is fully adequate to allow the implementation of very fast transceivers, which will be a key component in future systems. The 28 nm is a mature one, which is an advantage as key aspects such as its response to the ionizing and not ionizing radiation that required extensive characterization are expected to remain stable over time. On the other hand, the use of the technology is more complex both for the analogue and the digital design. In analogue design, many new layout rules are introduced that reduce the flexibility the designers have in optimizing critical analogue circuits. In digital, the complexity of digital libraries and PDK require a longer training curve. The use of the technology in the AIDAInnova project is thus exploratory, with the aim of fostering its use in the community. As a first step, small ASICs have been designed and fabricated to address two major items: the effective design of key analogue blocks and the characterization of the technology radiation hardness. Whenever the application becomes relevant, such as in the design of front-end amplifiers, pixel detectors are targeted as hybrid pixel detectors with smaller feature size and better time resolution are expected to be critical for improving the performance of future particle detectors. Two chips containing different test structures have been designed and sent to fabrication in 2022. The tests are underway and discussed in the following.

## 2.1. 28 NM CHIP DESCRIPTION AND TEST RESULTS

### 2.1.1. Test chip designed by CPPM/IN2P3

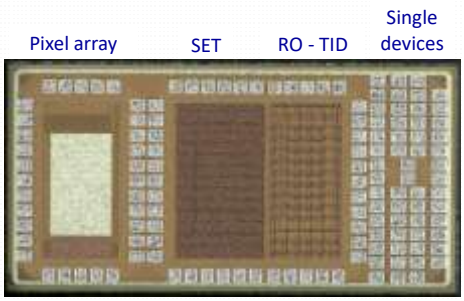


*Figure 1: ASIC protype developed by CPPM*

Figure 1 shows the prototype developed by the group of CPPM/IN2P3 in Marseille. The chip consists of four different sections that can be powered and tested independently. Three sections are intended to qualify the radiation hardness of the technology. The array of single devices (right part of the ASIC) allows to test the parameters change of single transistors under Total Ionizing Dose, (TID). The Ring Oscillator-Total Ionizing Dose (RO-TID) is a Ring Oscillator made with standard cells with the purpose of characterizing the radiation tolerance of the digital gates. The scope of the Single Event Transient (SET) test structure is to characterize the sensitivity of the technology to Single Event Transient. Briefly, charge particles can induce voltage spikes that can propagate through combinational logic and generate bit upsets in memories, FIFOs and state machines. The problem tends to worsen as the technology becomes faster, so a thorough study of the 28 nm case is necessary. Finally, the Pixel array contains a matrix of 36 x 12 front-end for hybrid pixels with binary readout and Time-over-Threshold capability, targeting very small pixel size (25 µm x 25 µm). Figure 2 shows the chip on the test Printed Circuit Board (PCB).

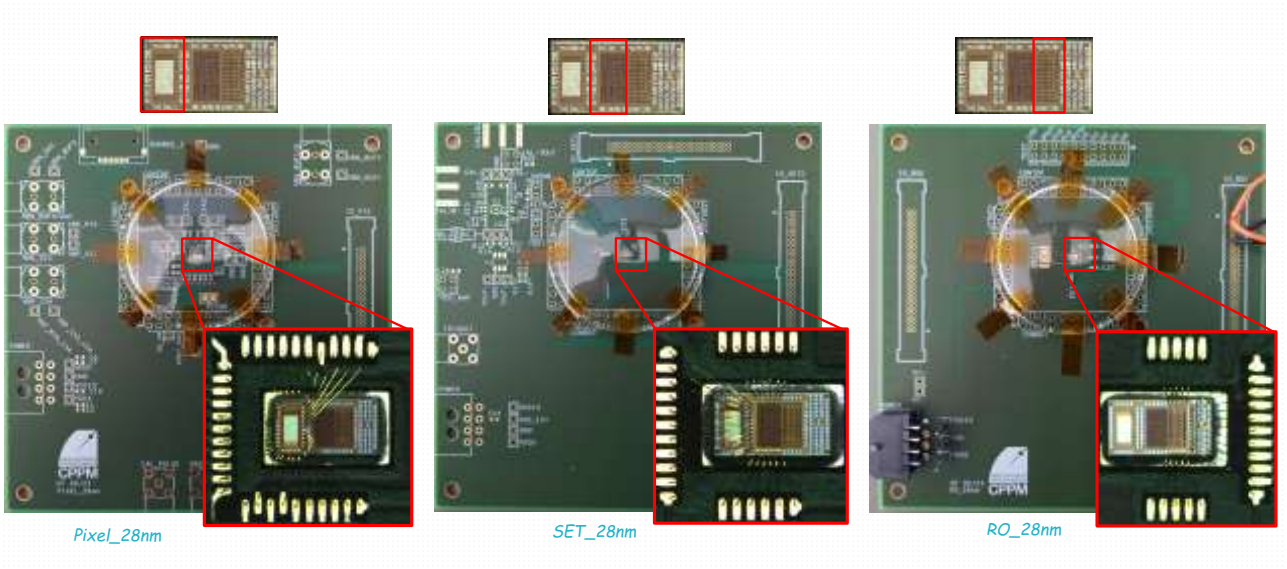


*Figure 2: ASIC protype developed by CPPM on the test board*

The same board tests the various parts by wire-bonding the appropriate one. Test measurements are underway. The test program started with the characterization of the pixel array, which is fully functional with results consistent with simulations (noise below 100 electrons for an input capacitance

of 100 fF and RMS jitter below 100 ps for signal charge above 4000 electrons). The radiation testing will take place in Q3 and Q4 of 2024.

### 2.1.2. Test chip designed by INFN-Pavia

The test chip designed by INFN-Pavia is shown in Fig. 3. The chip features single devices to test device characteristics before and after irradiation and a complete analogue pixel front-end. The chip has been fabricated and the tests are in progress. Several interesting results have emerged from the measurements. First, the 28 nm process has shown an increase of the gate leakage current compared to older technology nodes. This is not a showstopper for analogue circuit designs; however, additional attention should be paid when long shaping-time is needed or in sampling circuits that need to store an analogue voltage for long times. The technology, on the other hand, proves to be very robust against TID effects. Only marginal increases in noise and shifts in transistor threshold voltage were measured, confirming that, from this respect, the technology is fully adequate for the next generation of detector front-end. Figure 4 shows as an example a comparison between the noise of a NMOS transistor before and after irradiation. It is apparent from the figure that the noise increase is marginal. A front-end containing an innovative 2-bit flash ADC was also implemented and tested. The circuit contains innovative discriminators with auto-cancellation of the offset. The measurements of the front-end show that the technique works effectively, allowing to keep the threshold dispersion between the compactors around 25 electrons RMS without the need of dedicated digital-to-analogue converters for trimming.

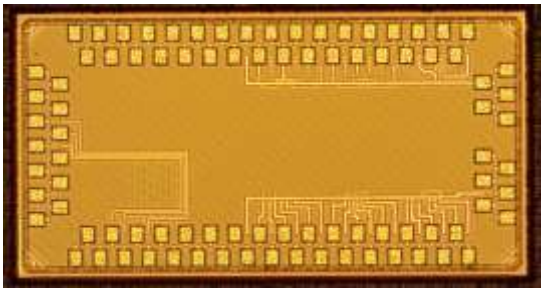

*Figure 3: ASIC protype developed by INFN-Pavia*

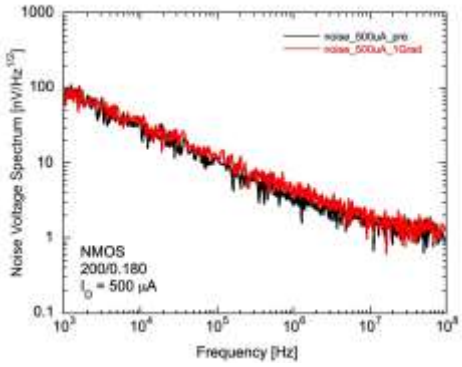


*Figure 4: Noise measured before and after irradiation to 1 Grad*

### 2.1.3. Other developments

Other developments are ongoing and well advanced but did not yet reach a maturity for a submission to the foundry. A very interesting design is a fast and low-power 10-bit ADC being developed by AGH in Krakow. The ADC cell has been designed and verified in post-layout simulations. The integration of the test chip is in progress and the submission to the foundry is expected to take place in Q3 2024. The simulation results are very promising, suggesting that a sampling frequency of 180 Ms/s and a power consumption of 150 µW could be achieved. The ADC occupies an area of 280 µm x 110 µm. This design will be an excellent test bench to cross-check the correlation between simulations and results in complex mixed-signal design. The development of complex parametrized

cells optimized for mixed-signal circuits is being pursued by University of Bonn, with the aim of accelerating the implementation of complex layouts.

## 3. FINAL REMARKS AND OUTLOOK

Work package 11.2 explores the use of 28 nm for future detector front-end. The technology is very complex and the PDKs required a long learning curve to be mastered. This delayed the submissions, and it was decided to accumulate enough measured data before producing a report. Interesting test chips have been however fabricated, and the tests are now well underway. The results so far are promising, showing that the technology is fully adequate for future front-end chips and providing valuable insights on the required design criteria. More tests are in progress and the submission of other test chips is expected within Q3 2024. It is therefore expected that by the end of the project task 11.1 will be fulfilled, by providing measured data and guidelines that will serve as valuable inputs for the design of more complex detector readout ICs in the future.

# ANNEX: GLOSSARY

| Acronym | Definition |
|---|---|
| ASIC | Application Specific Integrated Circuit |
| MPW | Multi-Project Wafer |
| IC | Integrated Circuits |
| ADC | Analogue-to-Digital Converters |