A Small-size Semi-lumped Three-port Tunable Power Divider

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***Abstract*— In this paper, a small-size semi-lumped three-port power divider with both power and frequency tune is designed and measured. The proposed topology uses complex impedance transformers in each output branch. A 3D CPW prototype is realized with varactor diodes. It exhibits a wide tunable power, from -1.3 dB to -21 dB, and a wide working frequency tune, from 0.8 GHz to 1.4 GHz. Measurements and simulations are in good agreement.**

***Index Terms*— Power divider, tunable device, tuner, varactors.**

I. INTRODUCTION

Tunable miniaturized devices constitute a great challenge in the field of modern RF/microwave telecommunications. In the near future, more and more applications will use multiple operating frequencies, with hard miniaturization constraints for MMIC applications. In this context, some researches are carried out to show the feasibility of various tunable devices that can be embedded in RF/microwave telecommunication systems like phase shifters, impedance transformers, filters, couplers, and power dividers. Several technologies can be used to achieve such tunable devices: ferroelectric and ferromagnetic materials, MEMS, piezoelectric devices, optical control and semiconductors.

The maturity of the power dividers goes back to the years 1960 when Wilkinson realized a N-way power divider [1]. Since, many researches were made in order to reduce the size of the devices [2], [3], [4], to increase their bandwidth [5], to eliminate the frequency harmonics [6] and for an unbalance distribution of the power in each output ports [7].

To our knowledge, few works proposed a tunable power distribution. In [8] a four-port divider with a tunable distribution of the power was presented. However no work was made on tunable three-port dividers.

In this paper, a three-port tunable power divider is presented. It can be tuned both in power distribution and in term of working frequency. As any power divider, our device is based on impedance transformation but it does not use quarter-wave transmission lines. Two semi-lumped complex impedance transformer, with a λ/10 length, constitute each output branch of our divider, leading to a miniaturized device. The paper is organized as follows: in section II, the principle of the power divider is described. In section III, the design of a prototype based on a 3D CPW (three dimensions coplanar waveguide) technology is described. Measurements are shown in section IVand some perspectives are discussed in section V.

II. PRINCIPLE

A three-port tunable power divider is used to split a power P_1 at the input port throughout the two output ports, with powers P_2 and P_3, respectively. In our design, this power distribution is tunable from balanced (P_2=P_3) to maximum unbalanced distribution (P_2>>P_3 or P_3>>P_2).

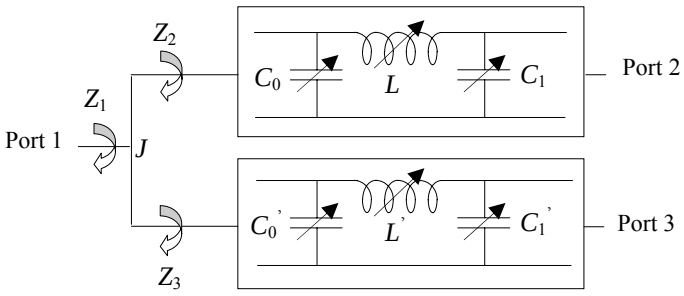

Fig. 1 Principle of the proposed tunable three-port power divider.

The principle of the three-port power divider is described in Fig. 1. A CLC tunable impedance transformer constitutes each output branch of the divider. Let call Z_2 and Z_3 the input impedances of the two output branches.

The available power at the input port 1 can be written as:

$P_1 = \frac{V^2}{Z_1}$ where V is the voltage at the junction point J.

In the same manner: $P_i = \frac{V^2}{Z_i}$ with i=2 or 3 for the output branches.

So $\frac{P_i}{P_1} = \frac{Z_1}{Z_i}$ (1).

If losses are neglected, then: P_1=P_2+P_3, leading to:

$\frac{1}{Z_1} = \frac{1}{Z_2} + \frac{1}{Z_3}$ (2) or $Y_1 = Y_2 + Y_3$ (3), where $Y_i = \frac{1}{Z_i}$ is the input admittance of branch *i*.

The input port is matched when Z_1 is equal to the conjugate of the reference impedance, ie 50 Ω in the general case that will be considered in this paper. Next, the power distribution is realized by tuning Z_2 and Z_3 input impedances.

When $Z_2 = Z_3 = 2Z_1$, the input power is equally distributed throughout ports 2 and 3. We speak of a balanced distribution

of the power. The divider works in a balanced mode.

When Z_2 (resp. Z_3) = Z_1 and Z_3 (resp. Z_2) >> Z_1, there is an unbalanced distribution of the input power. Port 3 (resp. port 2) is considered as open. In this case, all the power is sent into port 2 (resp. port 3). The divider works in an unbalanced mode.

For a typical case, the evolution of Z_2 and Z_3 from balanced to unbalanced mode is simulated for all ports loaded by 50 Ω, and for an input matching $|S_{11}| < -20\,\text{dB}$. Simulations results are shown in Fig. 2 Smith chart at a fixed frequency. In the balanced mode, $Z_2 = Z_3 \approx 100\Omega$ and $P_2 = P_3$. For the maximum unbalanced mode, $Z_2 \approx 50\ \Omega$ and $Z_3 \approx \infty$, leading to $P_2 \approx P_1$ and $P_3 \approx 0$. Between these two extreme cases, Z_2 and Z_3 are complex, they are linked by relation (2).

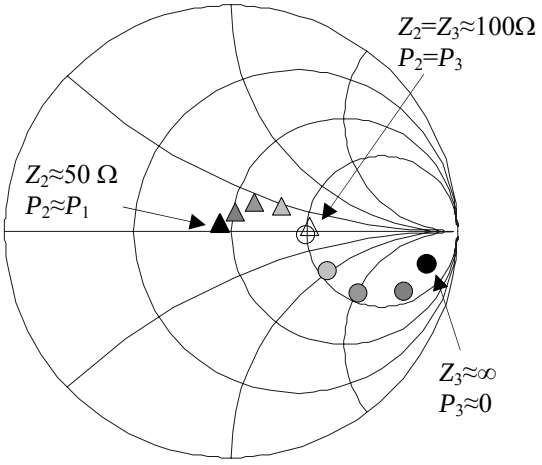

Fig. 2 Input impedance Z_2 (▲) and Z_3 (●) of branches 2 and 3 for a balanced mode (white) to a maximum unbalanced mode (black), with intermediate points (Grey).

Z_2 and Z_3 are realized by CLC tunable impedance transformers. These Π transformers with three tunable elements allow a large complex impedance coverage on the Smith chart. Fig. 3 gives the realization principle of the impedance transformers. The variable capacitors are realized by varactor diodes and the tunable inductance is realized by a varactor in series with an inductor [9].

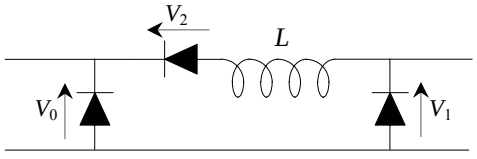

Fig. 3 The impedance transformer realization principle.

III. CONCEPTION

The power divider is constituted by two impedance transformers as shown in Fig. 4. A pair of capacitors C is necessary to separate the diode's bias voltages of the two impedance transformers while maintaining the divider symmetry.

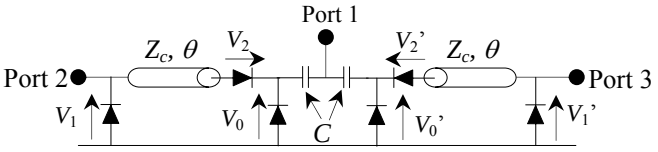

Fig. 4 The tunable power divider.

For the realized prototype, Macom™ MA4ST-1240 varactor diodes are used. The equivalent electrical circuit of these diodes (Fig. 5) is constituted by a series inductor (L_S=1.8nH), a series resistance (R_s=1.6Ω), a case capacitance (C_c=0.11pF) and a tunable capacitance ($C(V)$) varying from 1.5 to 8.6 pF with a bias voltage V varying from 12 V to 0 V.

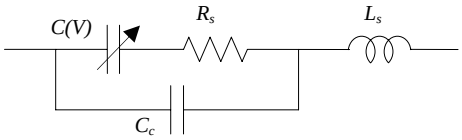

Fig. 5. Macom MA4ST-1240 Varactor equivalent electrical circuit.

In order to minimize losses, the inductor L is realized by a section of transmission line of characteristic impedance Z_c and electrical length θ, leading to a semi-lumped device. We chose a CPW technology to achieve an easier soldering of the varactor diodes.

The power divider was designed on a Rogers™ RO4003 substrate (relative permittivity $\varepsilon_r = 3.38$, dielectric loss $\tan(\delta) = 0.0035$, substrate thickness $h = 0.813$ mm, and copper thickness $t = 35$ µm). The inductance is realized by a transmission line with a 250 µm central conductor width, a 2.8 mm gap width and a 15.7 mm length leading to a characteristic impedance $Z_c = 200\Omega$ and an electrical length $\theta = 27.5°$ at the working frequency of 1.1 GHz (ie less than λ/10) instead of λ/4 for classical Wilkinson power dividers.

The realized prototype of power divider is shown in Fig. 6. The gaps in the ground planes permit to separate diodes biases. SMC (Surface Mounted Component) capacitors maintain the ground continuity in high frequency.

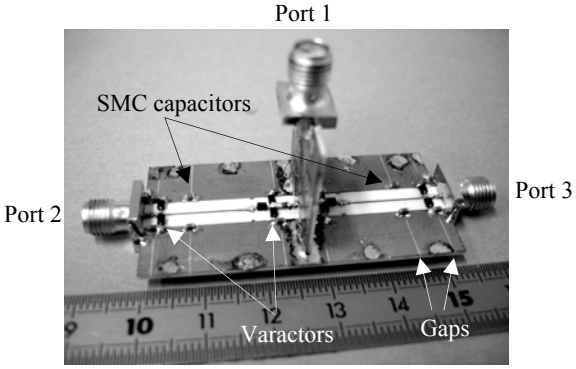

Fig. 6 Photography of the power divider.

The used of a 3D junction leads to an easy connection between the three branches of the divider. Note that a

microstrip technology could also be used, with via holes for the connection of the shunt varactor diodes.

IV. RESULTS

First the tunable distribution of the power is shown at a fixed frequency. Secondly the tuning of the working frequency for a balanced and for a maximum unbalanced distribution of the power is presented.

A. Tunable power distribution for a fixed working frequency.

At a fixed working frequency, the divider permits a tunable distribution of the power from a balanced mode when $Z_2 = Z_3 = 2Z_1$ to a maximum unbalanced mode when $Z_3 >> Z_2$ and $Z_2 = Z_1$, as previously shown in Fig. 2. This tunable distribution of the power is obtained by varying the different diode's biases. Fig. 7 (a) shows measurement results of S_{21} and S_{31} magnitude for the balanced and the maximum unbalanced modes, and for intermediate mode. As expected in the balanced mode, the input power is equally distributed to the two output ports. The same bias voltages are applied to the diodes of the two transformers: V_0=V_0', V_1=V_1' and V_2=V_2'. We measured $|S_{21}| = |S_{31}| = -3.8\,\text{dB}$ at 1.1 GHz. So insertion loss is 0.8 dB.

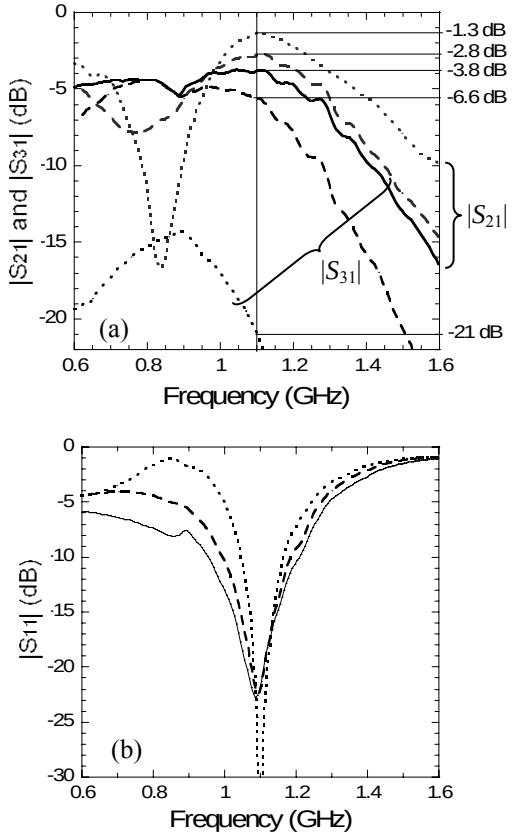

Fig. 7 $|S_{11}|$, $|S_{21}|$ et $|S_{31}|$ measured at 1.1 GHz for a balanced mode (—), medium unbalanced mode (– –) and for a maximum unbalanced mode (····).

To achieve an unbalanced power distribution through the output ports, the varactor diodes of the two impedance transformers are differently biased. In Fig. 7, medium and maximum unbalanced distributions of the power have been represented. In the maximum unbalanced mode, we obtain $|S_{21}| = -1.3\,\text{dB}$ and $|S_{31}| = -21\,\text{dB}$ at 1.1 GHz, leading to about 1 dB insertion loss.

Note that the power divider is always matched at the input port with $|S_{11}| < -20\,\text{dB}$ (Fig. 7 (b)).

B. Tunable working frequency for balanced and maximum unbalanced modes.

First, the working frequency tunability considering the balanced mode is addressed. Simulation and measurement results are given in Fig. 8 for $|S_{11}|$ and $|S_{21}|$. $|S_{21}| = |S_{31}|$ for the balanced mode. Results are given for only three different frequencies, 0.8 GHz, 1.1 GHz and 1.4 GHz, but the tuning is continuous from a minimum working frequency f_{min} equal to 0.8 GHz to a maximum working frequency f_{max} equal to 1.48 GHz in simulations and from 0.8 GHz to 1.58 GHz in measurements. Dot points represent results of $|S_{21}|$ for working frequencies from f_{min} to f_{max}. The agreement between simulation (Fig. 8 (a)) and measurement (Fig. 8 (b)) results is very good. For an input matching $|S_{11}| < -20\,\text{dB}$, $|S_{21}|$ is better than -4.8 dB from 0.8 GHz to 1.58 GHz, leading to a ± 33 % tunable working frequency around 1.2 GHz.

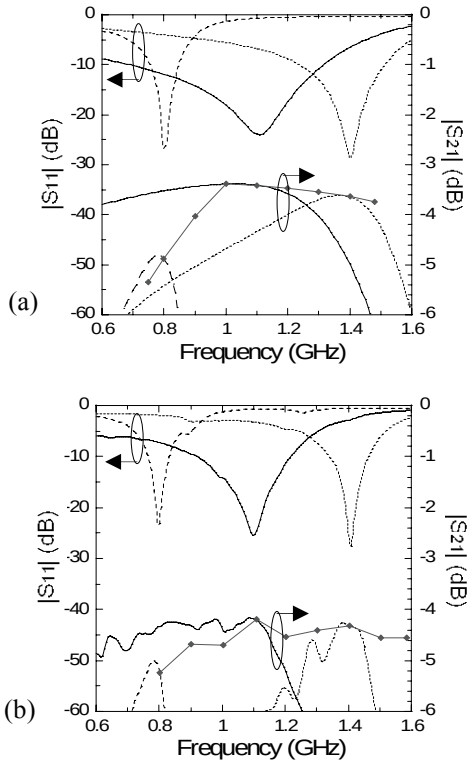

Fig. 8 (a) simulations and (b) measurements of the power divider in balanced mode. $|S_{11}|$, $|S_{21}|$ and $|S_{31}|$ at 0.8 GHz (– –), 1.1 GHz (—) and 1.4 GHz (····).

The differences between simulations and measurements can be attributed to the varactor diodes parasitic elements inaccuracies and the 3D junction that has been considered as ideal in the simulations.

The same study of the working frequency tunability was realized considering the maximum unbalanced mode. Measurement results of $|S_{21}|$ and $|S_{21}|$ are given in Fig. 9. From 0.8 GHz to 1.4 GHz, it can be considered that the unbalanced mode is possible, with $|S_{21}| > -1.4\,\text{dB}$, $|S_{31}| > -17\,\text{dB}$ and $|S_{11}| < -20\,\text{dB}$. So, in the unbalanced mode, a ± 29 % tunable working frequency around 1.1 GHz is achieved.

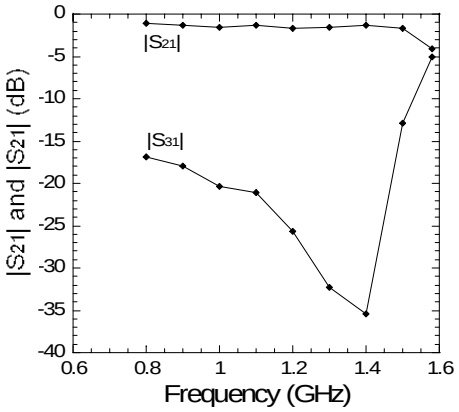

Fig. 9 $|S_{21}|$ and $|S_{31}|$ for the maximum unbalanced mode.

V. Discussion.

The realized prototype has shown the validity of the proposed tunable power divider topology. To go further, it could be interesting to realize the power divider in a microstrip technology, in order to obtain a 2D planar device and a much simpler *J* junction.

It is also interesting to point out the origin of insertion loss.

Frequency (GHz)	$R_s = 1.6\,\Omega$	$R_s = 0.4\,\Omega$
0.8	-4.8 dB	-3.4 dB
1.1	-3.4 dB	-3.1 dB
1.4	-3.7 dB	-3.2 dB

Table 1 Simulation of $|S_{21}|$ for two different series resistances of the diodes in the balanced mode.

Table 1 shows simulation results of the insertion loss obtained in the balanced mode. Simulations have been carried out for two different values of the diode's series resistance R_s, ie 1.6 Ω (actual case) and 0.4 Ω. For $R_s = 0.4\,\Omega$, insertion loss are smaller than 0.4 dB for the whole tuning frequency band, from 0.8 GHz to 1.4 GHz. For $R_s = 1.6\,\Omega$, insertion loss are equal to 0.4 dB, compared to the 1.2 dB measured insertion loss (see Fig. 8(b): $|S_{21}| \approx -4.2\,\text{dB}$). The difference between simulation and measurement results are probably due to the 3D *J* junction that was not at all optimized.

These simulation results show that the use of a MEMS technology to realize tunable power dividers for working frequencies around 20 GHz could lead to very interesting results in term of power tuning and insertion loss.

VI. Conclusion

A new topology of a power divider with both power and working frequency tune has been proposed. A prototype has been realized in a 3D CPW technology. The output power can be tuned between -1.3 dB to -17 dB over a wide working frequency range, from 0.8 GHz to 1.4 GHz. The semi-lumped approach used for the design leads to a small-sized device with less than λ/10 output branches.

Insertion loss is lower than 1.8 dB. It is due to the CPW 3D junction and the varactor diode's parasitic series resistance. The insertion loss could be reduced to less than 0.4 dB if the junction was correctly optimized and diodes with a better quality factor were used. Finally, a MEMS power divider based upon the proposed technology could be designed with interesting expected characteristics in term of power and working frequency tuning range.

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