

DATA ACQUISITION SYSTEM FOR A TIME PROJECTION CHAMBER

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A data acquisition system has been designed to digitize the trajectory information of muon decay every eight milliseconds. A time projection chamber is used which operates in a solenoidal magnetic field. It has 315 sense wires which induce signals on 5355 pads and thus create approximately 402,000 bits of data for each event or 55 megabits per second. Most of the data are zeros which are handled using a hardware-aided compaction scheme. The meaningful data are extracted by a modular system consisting of three basic building blocks. These are flash encoders with associated storage, wire hit memory boards, and bit-slice data preprocessors described herein.

Introduction

A Time Projection Chamber (TPC)^{1,2} is a three dimensional charged particle detector. In a TPC the ionization electrons produced by the particle within the chamber are forced by a uniform electric field to drift towards a readout plane. At the readout plane, the ionization electrons initiate an avalanche on the sense wires. An induced charge from the avalanche appears on cathode segments, called pads, located under the sense wires, as shown schematically in Fig. 1. The location of the pads which have an induced charge and the wires which were hit by ionization electrons give the x,y coordinates. The time from the event trigger to the detection of charge on the pads gives the z dimension. It is possible to reconstruct a three-dimensional picture of the particle track in the chamber from these coordinates.

System Considerations

Each pad has its own charge-to-voltage converting amplifier whose signals are multiplexed to reduce the number of transient recorders (high-speed digital-to-analog converters with associated random access memory) needed to digitize the data. The multiplexing scheme attempts to minimize the ambiguities in the data by multiplexing those pads which are unlikely to have charge induced on them by the same particle track at nearly the same time. Thirty-five pad amplifier signals are connected to each multiplexer circuit. This reduces the number of transient recorders from 5355 to 153. Figure 2 is a schematic diagram of a transient recorder. There are eight transient recorders on a

board. The boards are large double-sided printed circuit boards approximately 16 inches wide by 18 inches long. The use of large boards reduces the number of interconnections within the system, makes it more compact, and therefore increases its reliability. Furthermore the reduced size of the overall system makes it possible to put the entire system in one forced-air-cooled relay chassis.

The output of the multiplexer circuit is a 200-nanosecond-wide pulse. A transient recorder amplifier serves as an impedance matching device with a gain of 2. A 25-MHz clock rate was chosen to take five samples (time buckets) of each pulse. This is more than the TRW 1007J Flash Encoder³ (a high-speed digital-to-analog converter) worse case specification of 20 megasamples per second. The output of the Flash Encoder is stored sequentially in eight Intel 2125H-3⁴ integrated circuits so the addresses correspond to the timing information. These chips are 1 bit wide by 1024 bits deep, and are capable of 35-MHz operation. They have tri-state outputs, and are static, random access devices. All these features are important to the system design.

The wire hit information from each of the 315 wires in the TPC is recorded as one binary bit per wire for each time bucket in the wire hit storage boards. Figure 3 is a schematic diagram of one of these boards. The output of the wire amplifier/discriminators is an ECL logic signal which is converted to TTL logic on the wire hit boards by the 10125⁵ receivers. The storage section is 64 bits wide by 1024 words deep and also uses the 2125H-3 integrated circuits. At 40 nanoseconds per time bucket, the memory will hold 40 microseconds worth of data. This is more than sufficient for the drift time of the TPC (20 μ sec). When data are recorded the clocks for both the wire hit storage boards and the transient recorders are synchronized. The rest of the circuitry on the wire hit memory board is used during data compaction and will be described later.

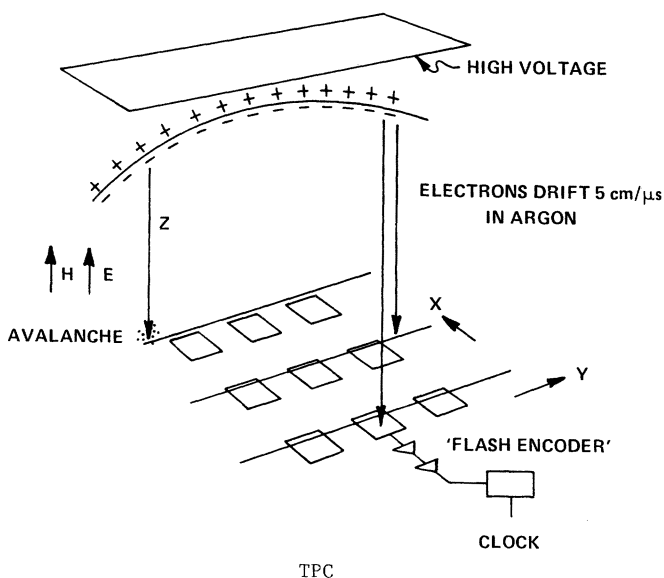


Figure 1.

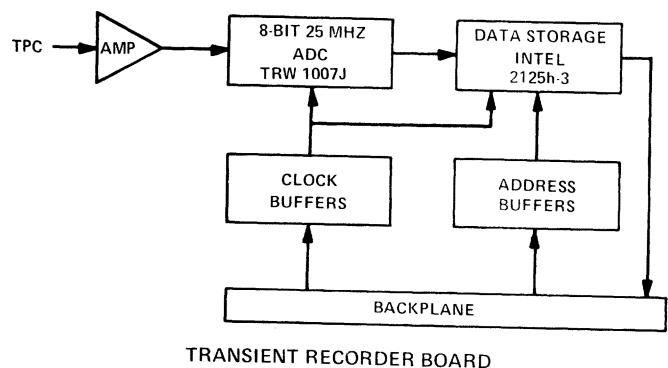


Figure 2.

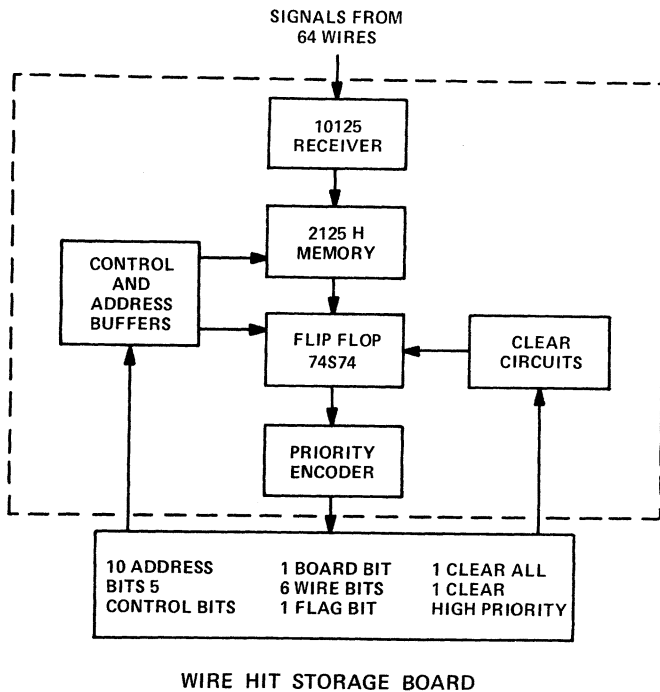


Figure 3

Typical drift velocities in the TPC are on the order of 5 cm/ μ sec; therefore, all the data produced by one event can be recorded as x,y (pad and wire), z (time or sequential memory address) coordinates in 20 μ sec. Each event produces $\pm 53 \times (8 \text{ bits/word} \times 500 \text{ words}) + (315 \text{ bits/word} \times 500 \text{ words}) = 402,000$ bits of data. The event rate is 120 per second. Therefore, The TPC is producing 55 megabits of data per second. Most of the data recorded during an event are the baseline values (zero) of the transient recorders. How much significant data will exist is still open to question, but the best calculation is that around 250 pads will have charge induced on them by a typical event.

Data Compaction

The system design handles this large sparse array of data in the following manner. First the chamber is divided into three independent partitions. Each partition has 105 wire amplifier/discriminators and 51 pad amplifier multiplexer signals. The chamber partitions were chosen in a manner which equalizes the work load for the data preprocessors. Figure 4 is a schematic diagram of TPC digitizer and preprocessor system. Each partition requires 7 transient recorder boards to digitize the signals from the 51 pad amplifier multiplexers, two wire hit storage boards to record the data from the 105 wires assigned to the partition, and one preprocessor to do the sparse data scan for the partition. Notice there are three back-plane busses shown, one for each partition. This eliminates back-plane contention problems between the three data preprocessors. Each back-plane bus has 200 signal lines. Two of the back planes have 10 slots, the third has 17 to accommodate the rest of the system elements, such as the magnetic tape data formatting preprocessor and the main computer interface.

The data preprocessors, which are identical, are designed utilizing bipolar bit slice logic and have an 88-bit wide microword to insure highly parallel operation. Many operations can be performed in a single 200 nanosecond cycle time. Figure 5 is a schematic diagram of the data preprocessor. This

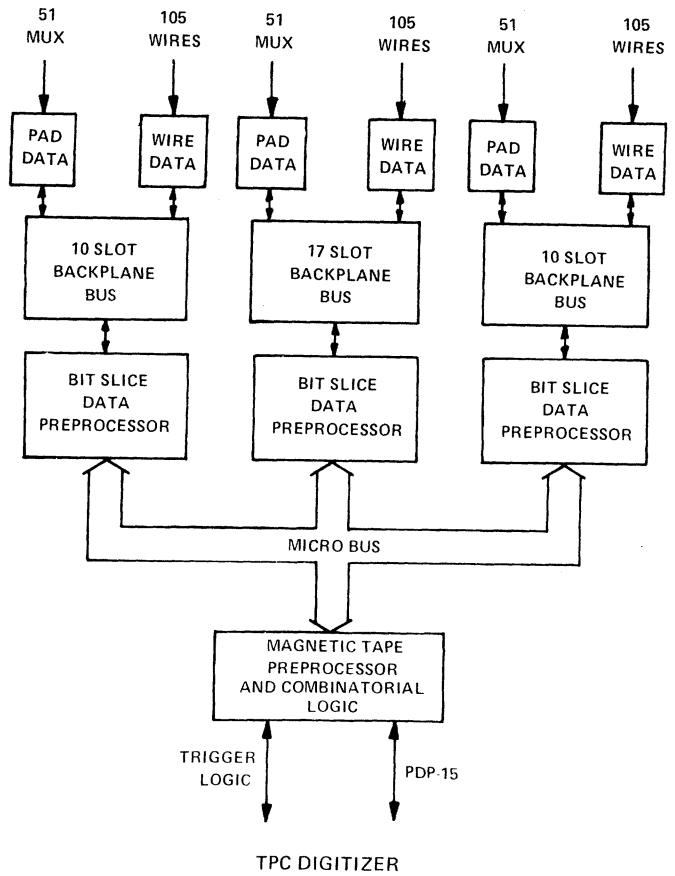


Figure 4

design takes advantage of the register expansion capability of the AMD⁶ 2903 bit slice integrated circuit by making the special purpose registers which control the operation of the transient recorders, and wire bit modules appear as internal registers to the data preprocessor. This arrangement eliminates the need for input-output operations. A fast multiplier chip and a pipeline register are utilized to increase the speed of the data reduction algorithm. The N counter, N register, and N comparator are part of the digitizer control. Their purpose is to allow pre-trigger recording of the data in the TPC. These registers are also internal registers to the preprocessor.

The search for non-zero data is done very rapidly by scanning the data in the wire hit memory modules. This scan is done by priority encoder circuitry on the wire hit memory module that allows the preprocessor to search all wire hit memories for data in parallel at the rate of one cycle per empty time bucket. When hit data is found, a flag notifies the preprocessor and the output of the priority encoder is used as a vector for a lookup table which contains the address of the pertinent transient recorder. The 74S74 Flip-Flop register in conjunction with the clear circuitry allows each high priority bit to be cleared without changing the bits which have lower priority within the time bucket being examined. Therefore, no wire hit data will be missed. The address counter for the transient recorders is independent of the one used for the wire hit modules during data compaction so that it may be varied without changing the time-bucket information. This feature saves the time that would be needed to save and restore the time-bucket information. The compacted data are then stored in the preprocessor's dual-ported memory.

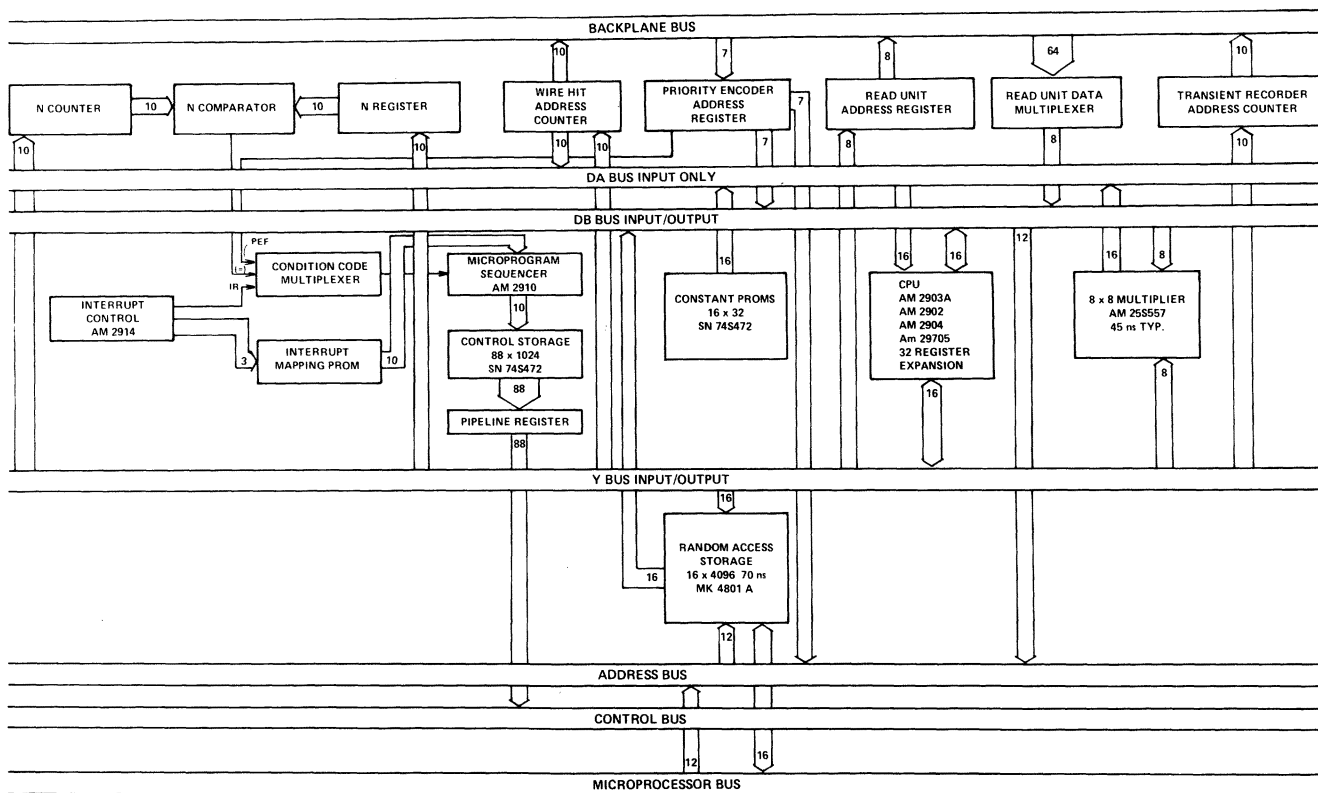


Figure 5.

A fourth preprocessor, which has access to the compacted data through the second port, gathers the data from the three data preprocessors. It then formats and ships the data to the main computer system where it is written onto magnetic tape. The main computer samples events to determine that the experiment is functioning properly. The main analysis is done off-line.

Conclusion

A modular system has been designed which can be easily modified to meet the needs of both the current and future uses of the TPC.

Acknowledgments

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