IEEE Transactions on Nuclear Science, Vol.NS-25, No.6, December 1978

ULTRA-HIGH UPSET, MEGARAD-HARD SI-GATE CMOS/SOS CODE GENERATOR*

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Abstract

A high-speed, radiation-hard code generator LSI array has been developed and fabricated. A unique design approach combined with hard silicon-gate CMOS/ SOS processing has resulted in an ultra-high transient-upset threshold ($\sim10^{11}$ rads/s for 50 ns pulse width) and megarad total-dose hardness. This paper describes the design as well as characterizes the electrical, radiation and temperature capabilities of this device. Even with modified design and the radiation-hard process, the code generator achieves better than 20 megabit per second operation. The measured 25°C and 125°C clock-to-output propagation delays are 46 and 52 ns respectively prior to radiation exposure. The measured clock-to-output propagation delay after 10^6 rads (si) is 55 ns. These results demonstrate Si-gate CMOS/SOS as a successful radiation-hard LSI technology.

Introduction

The benefits of low-power, high speed and radiation-hardness required for space applications can be realized using Si-gate CMOS/SOS technology in LSI-arrays. Typical LSI candidates requiring these benefits are sequence generators frequently used in spacecraft components for security, jam-resistant, and time keeping applications. As an example, the baseband subsystem from a navigation satellite application is shown in block diagram form in Figure 1. This subsystem produces a 10.23 megabit per second precision (P) navigation code using an atomic frequency standard with the appropriate accuracy. The PX1 and PX2 code generators each produce a one and one-half second long pseudorandom sequence which are then combined, with appropriate relative delay, to form the seven-day long P code. The tap register varies the delay of the X2 sequence enabling one of thirty-two unique sequences to be formed. The Z counter is advanced every 1.5 seconds with a count of 403,200 required for a complete week. Monitoring, control and initialization of the sequence is provided through the phase adjustment logic subject to externally provided control signals. This paper discusses a mask programmable radiation-hard code generator, designated the TCS102, that generates the pseudorandom sequences in the precision navigation baseband subsystem.

Array Description

There are three basic functional elements on the TCS102 array. The first two elements, designated the X_A and X_B code generators, are twelve-stage pseudorandom sequence generators. Each sequence generator consists of twelve master-slave register stages with the output of the final stage being fed back to exclusive-OR gates located between selected successive register stages. The specific sequence generated is selected by using a metal mask option to locate the feedback taps. The third element of the array is a twelve-stage synchronous counter. In addition, control and clock logic associated with each of these elements is included on the array. The TCS102 is 5.13 by 4.80 mm (202 mil x 189 mil) in size and contains a total of 2660 transistors. A photomicrograph of the TCS102B (the specific metal mask option described in this paper) is shown in Figure 2. Test devices designed to aid device characterization and lot-sampling tests are included along the chip periphery.

Figure 1. A block diagram of a precision navigation baseband subsystem.

The X_A code generator portion of the TCS102 array consists of a twelve-stage pseudorandom sequence generator, a twelve-stage serial shift register, state-decode logic and clock-control logic (Figure 2). The pseudorandom sequence produced by the programmable sequence generator is clocked through the twelve-stage serial register. Buffered array outputs are taken at twelve successive stages of the sequence generator and serial register as well as at the final register output to provide sequence outputs shifted in time. The state-decode logic gives an epoch output whenever the sequence generator reaches a preprogrammed state. The clock-control logic is used to halt or resume X_A sequence generation depending on control inputs to the array. The X_A sequence can be externally initialized by the SET input pulse. Specifically, the X_A code for the TCS102B is generated by the polynomial $X^{12} + X^{11} + X^{10} + X^9 + X^8 + X^7 + X^5 + X^4 + X^3 + X + 1$. The sequence length is shortened to 4092 bits from the natural 4095 bits by resetting the sequence generator with the epoch signal. The generation of the X_B code is similar to that of the X_A code.

The synchronous counter on the TCS102 generates 1.5 second timing pulse (if operated at a 10.23 MHz clock rate) by counting the epoch pulses of the X_A code generator. Unlike a ripple counter where the carry propagates from the last to most significant stage when clocked, all stages of the TCS102 counter will change state simultaneously when clocked. In this manner, a valid count is maintained at all times in a synchronous system operating in the 10-20 MHz range. Although designed to count the epoch pulses generated by the X_A code generator, the connection of the X_A epoch to the counter input is external to the chip. This allows independent operation of the X_A code generator and the counter and facilitates testing of the array.

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*Work was supported by DNA under Subtask TD033.

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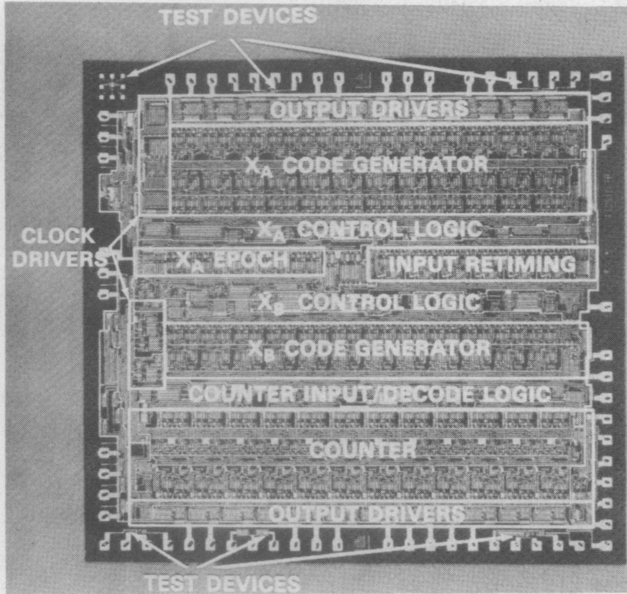


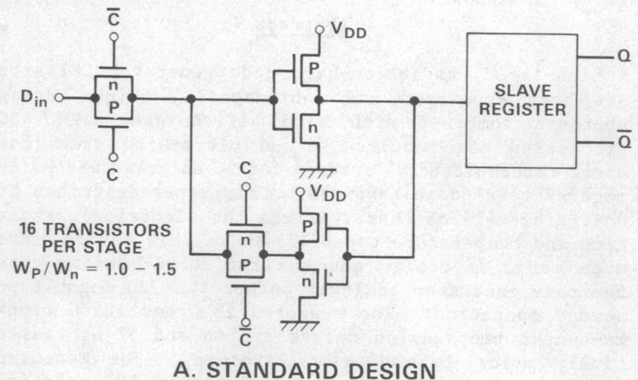
Figure 2. Photomicrograph of TCS102B code generator showing the functional elements of the custom array.

Array Design and Simulation

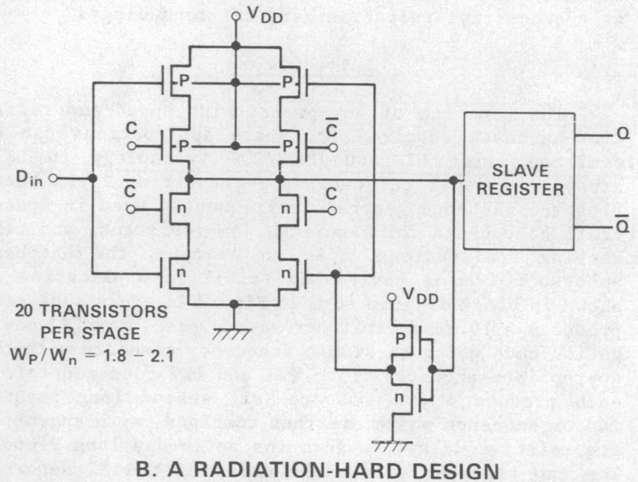
A handcrafted-custom approach rather than the standard-cell approach[1] was used to design the TCS102 array because the logic in the array is inherently repetitive rather than random, and because a mask programmable feature was desired. In addition, the custom approach allows the most freedom to optimize both electrical performance and radiation hardness. The design procedure that was followed entailed optimizing logic and circuit design to assure a high level of tolerance to transient-radiation induced circuit upset, while minimizing the effect on circuit performance of the expected total-dose induced parameter changes.[2] Consideration was given to total-dose induced threshold voltage changes (including transient annealing effects), mobility degradation, increases in subthreshold leakage of n-channel transistors and minimizing the irradiation-bias dependence of transistor parameter changes. For LSI arrays, it is most important to minimize this irradiation-bias dependence to make meaningful irradiation testing and simulations possible. Reasonable simulation and experiments, to data, make predictions of the worst-case bias condition virtually impossible.

Specific design rules included (1) elimination of circuit options that were more sensitive to upset than a 3-input NAND, (2) the bodies of stacked p-channel transistors were clamped to the positive power supply, (3) transmission gates were not used, (4) stacked transistors of the same polarity were limited to three and (5) the p-channel transistor widths in inverters were increased from a typical W_p/W_n ratio of 1.5 to about 2.0.

As an example, a standard-design master-slave static register stage, shown in Figure 3A, is contrasted with a radiation-hard register stage, Figure 3B, where some of the above rules were incorporated. The standard-design register is sensitive to radiation induced n-channel currents in the transmission gate, TG, (next to the D_{in} terminal) when this TG is in the OFF state. If D_{in} is changed to a logic "1" after a logic "0" is entered into the master, leakage through the transmission gate will tend to cause D_{in} to fall below the logic "1" level and the signal on the master inverter to rise above the logic "0" level. This effect, when coupled with the reduced noise immunity from radiation-induced parameter shifts, can eventually lead to failure in either the register or the D_{in} driving source. In contrast, the radiation-hard register stage uses no transmission gates and provides isolation between the D_{in} signal and the stored data.



A. STANDARD DESIGN



B. A RADIATION-HARD DESIGN

Figure 3. A comparison between the standard and a modified design for the register stages.

Extensive transient analysis using the R-CAP[3] computer simulation program was utilized to obtain an optimum design. These simulations were used to evaluate array speed capability, temperature performance and radiation sensitivity. Both total-dose and transient radiation performance was investigated. Model parameters utilized in the simulations are listed in Table I.

TABLE I

Transistor Parameters Used in Simulations

Parameter	N 0V Bias	N +10V Bias	P 0V Bias	P -10V Bias
V_T (pre) [V]	1.5		-1.5	
K' (pre) [$\mu A/V^2$]	5.0		3.35	
V_T (10^6rad) [V]	2.5	0.5	-3.5	-2.5
K'/K'_0 (10^6rad)	0.95	0.70	0.85	0.92

To study the effect on circuit performance of the bias conditions during irradiation, the propagation delay of the register stage followed by an output driver was determined by computer simulations using each of the sets of post-irradiation parameters given in Table I. The results showed a signal propagation delay of 54-57 ns when the output makes a positive going transition and 40-43 ns for a negative going transition. These results indicate the insensitivity of this design to irradiation-bias effects, at least for the speed parameter.

The simulated internal delays for the important elements of the TCS102 are listed in Table II for typical, worst-case temperature (125°C) and total-dose irradiation cases. An examination of these data show that 125°C temperature and irradiation have about the same effect on circuit performance. The simulated values also indicate a significant design margin from the maximum 100 ns delay allowable at 10 MHz operation. The predictions of maximum code generator speed using worst-case parameters are 18 MHz at 25°C, 13 MHz at 125°C and 13 MHz after a total-dose of 10^6 rad (Si) at 25°C.

Table II

Summary of the Simulated Internal Delays of TCS102 Sub-circuits

Sub-circuit	Pre-irrad. 25°C	Pre-irrad. 125°C	After 10^6 rad(Si)
Code Generator	17 ns	25 ns	26 ns
Clock Driver	13 ns	17 ns	16 ns
Clock Control	25 ns	35 ns	34 ns
Counter Logic	49 ns	67 ns	61 ns
Counter Output Register	17 ns	24 ns	23 ns
Out Drivers (Double inverter)	17 ns	24 ns	22 ns

Critical circuits such as the register stage were analyzed to study their transient-upset behavior. Sapphire photoconduction was assumed to dominate the transient response and a conductivity factor of 1×10^{-15} mho (mil-rad/s) based on test device performance[4] was assumed. A typical simulation result from the transient-upset analysis is shown in Figure 4. These data show that proper circuit operation is maintained at the simulation level with about a 25 percent degradation in the output level during the irradiation pulse. The simulations predicted 5- and 7-volt logic levels at 10^{11} rad/s indicating the proximity to upset. Although the exact upset levels are not necessarily predicted due to uncertainties in input parameters, these results are useful in uncovering circuits particularly susceptible to upset.

Array Processing

The circuits were processed using a radiation-hard, self-aligned, Si-gate CMOS/SOS process.[5] The n- and p-transistor islands were separately ion implanted, i.e., a single-epitaxial, full enhancement process. The gate oxide was a 925°C pyrogenic oxide that was annealed in oxygen and nitrogen at the same temperature. The gate-oxide thicknesses ranged from 700 to 850 Å. The P^+ polysilicon gates are boron doped during deposition. The sources and drains are separately ion-implanted (an addition mask is used to shield P^+ areas during phosphorous implantation) and the dopants are activated at 850°C. RF heated Al metalization is used. A low-temperature glassivation overcoat completes the passivation.

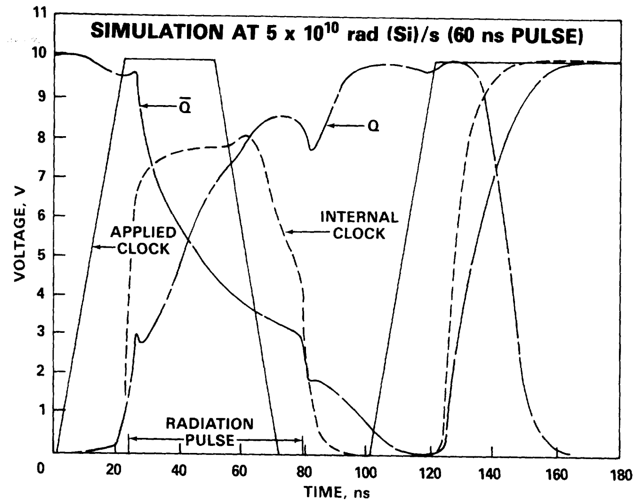


Figure 4. Simulated performance of the register circuit to a transient radiation pulse.

The array design rules allowed 0.25 mil polysilicon gate lengths and 0.4 mil minimum metal linewidth with 0.3 mil minimum spacing. Other design and layout rules are outlined in reference 6. Array input protection is provided by a closed-geometry gated diode, resistor and arc-gap that is compatible with the radiation-hard process.[7]

TABLE III

Transistor Parameters Measured on TCS102B Test Devices

	N OV Bias	N +10V Bias	P OV Bias	P -10V Bias	P +10V Bias
V_T (pre), [V]	2.0			-1.0	
K' (pre), [$\mu A/V^2$]	6.0			3.7	
V_T (10^6rad), [V]	2.0	0.0	-2.5	-2.2	-6.5
K'/K'_0	0.95	0.65	0.90	0.95	0.70

Test transistors on the TCS102 array were used to evaluate the performance of the radiation-hard process. These devices were exposed to cobalt 60 irradiation at various bias conditions. The transistor parameters before and after 10^6 rad (Si) are listed in Table III. These measured parameters are similar to the parameters used in the simulations except perhaps a slightly larger threshold voltage shift for the n-channel transistors. The large change in the p-transistor threshold observed under positive bias indicates the need for substrate clamps. Radiation-induced back-channel leakage of about 1 μA/mil was observed on some wafers and less than 0.01 μA/mil was observed on other wafers. All n-transistors exhibited some degree of edge-transistor leakage that was especially pronounced during positive irradiation bias.

Electrical Evaluation

TCS102 arrays were evaluated from both radiation-hard process and conventional process lots. Functional performance for the arrays was obtained from 3.5 to 10 volts for the hard process and 2.5 to 10 volts for the standard process. Higher voltage operation is possible but was not attempted. Measurements

of maximum array speed were performed by monitoring the X_A and X_B code outputs as the frequency was increased. Maximum frequency of operation as a function of operating voltage is shown in Figure 5 for typical arrays. For the radiation-hard process, the maximum operating frequency ranged from 18-26 MHz and 8-12 MHz for 10 and 5 volt operation, respectively. For the standard process, the maximum frequency range was 27 to 28 MHz at 10 volt operation. These data indicate that a modest (10 to 20%) performance reduction can be expected between the standard and radiation-hard processes. Note that the maximum operating frequency is an internal parameter and hence is independent of output loading. The simulations predicted a maximum operating frequency that was lower than generally observed (Figure 5). These results are expected, since the simulations used worst-case assumptions. In addition, the transistor mobilities assumed in the simulations were generally lower than experimentally observed.

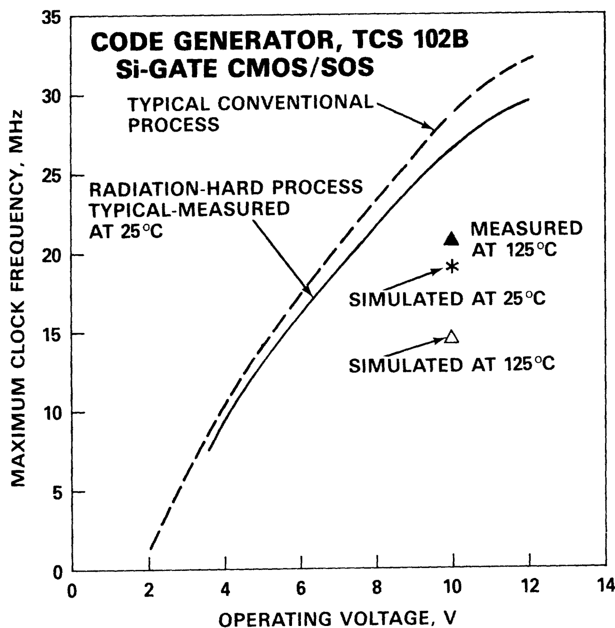


Figure 5. Performance of the code generator array as a function of operating voltage.

Measured signal propagation delays ranged between 45 and 50 ns (at 10V) for the clock input to code output path. Again, these values were slightly lower than the simulated values. The devices fabricated by the standard process had clock-to-output delays ranging from 37 to 43 ns. Propagation delays of 56 to 77 ns were measured for these arrays at 5 volts. Measurements made on the input clock requirements indicated considerable tolerance of the array to variations in clock duty cycle. Measurement of propagation delays as a function of output loading were made. The slope of this characteristic was measured as 0.2 ns per pF up to 60 pF.

Standby or leakage currents for the arrays were found to vary from array to array. The distribution of maximum leakage currents peaked near 200 μA (10 volt) for the devices fabricated by the radiation-hard process. The lot produced by the conventional process had lower (∿ 80 μA) average leakage. The 10 volt dynamic power was found to depend linearly on frequency at 22 mW/MHz.

Measurement of array performance over temperature showed that the maximum speed of the arrays was reduced by about 15-20 percent from the room temperature speed at 125°C. The simulation predicted a larger decrease in speed (about 30 percent) than the decrease experimentally observed (see Figure 5). Standby current increased by a factor of 100 over the room temperature values at 125°C. The dynamic power of the arrays increased to 250 mW (10 V and 10 MHz) at 125°C as compared with 220 mW at room temperature.

Total-Dose Effects

Ionizing total-dose effects on the code generator were evaluated by exposing the devices at the NRL cobalt 60 facility at a dose rate of 10^6 rad (Si) per hour. Since in the actual applications the code is continually generated without interruption, the arrays were clocked at 100 KHz during radiation exposure. A portable measurement box was used so that a limited functional test, the maximum frequency of operation and the standby current could be measured immediately after the removal of the devices from the irradiation source. The NRL-EH-4500 computer-controlled test system was then utilized to completely characterize the arrays including a full functional test and measurement of propagation delays at all outputs. In all cases, the arrays were completely characterized within 30 minutes after irradiation. Correlations between the EH 4500 tester and the portable test box indicated negligible annealing in all parameters except the array leakage. Typically, about 20 percent annealing in the standby current was observed during the measurement intervals.

The effect of total-dose irradiation on the TCS-102 array is primarily a reduction in the maximum frequency of operation and an increase in the standby current. The reduction in array performance as a function of irradiation dose is shown in Figure 6. The decrease in maximum operating frequency and increase in propagation delay was about 15 percent after 10^6 rad (Si). The simulated results, similar to those obtained for the temperature sensitivity, predicted more degradation than was observed. These data show that significant margin is available at 10 MHz at 10^6 rad (Si). Initial failures in some arrays were observed at $2x10^6$ rad (Si). Some arrays were functional after an irradiation dose of $3x10^6$ rad (Si). The leakage current increased from 100-500 μA before irradiation to about 1 mA at 10^6 rad (Si) as shown in Figure 7. The increase in leakage resulted primarily from island-edge-effects and to a lesser extent to back-channel leakage because similar increases in radiation-induced leakage current were observed for arrays taken from wafers where the test transistors showed no back-channel leakage.

Transient-Radiation Upset

The transient upset threshold for the array was measured using the 40 MeV LINAC with 50 ns to 1 μs electron pulses. Dosimetry was performed for each pulse by 4-1/8 inch TLD dosimeters. The electron pulse shape of the LINAC was monitored using a PIN diode. The array was operated at the nominal 10 MHz clock rate with the radiation pulse synchronized to the SET pulse (start of code generators). The delay between the irradiation pulse and the SET pulse was usually adjusted to about 1 μs. Several counter outputs were monitored during and after the irradiation pulse on dual-beam oscilloscopes. Since the SET pulse started the array in a known state, observation of the code generator outputs for only a limited number (about 25) of clock cycles was needed to determine if an upset in any internal register occurred.

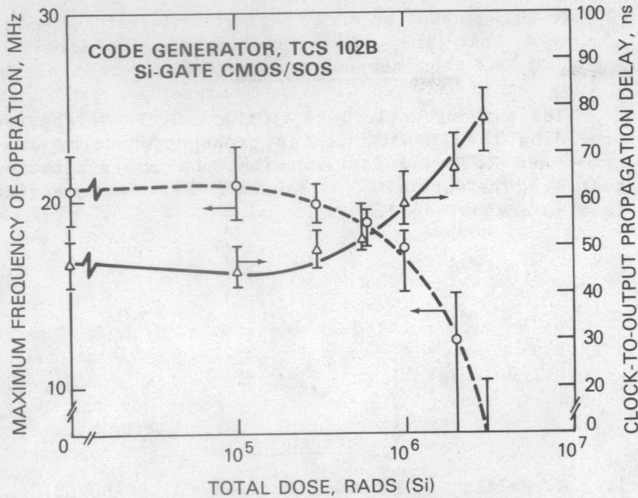


Figure 6. Performance curves for the code generator. The irradiations were conducted in a cobalt 60 source at a dose rate of 10^6 rad (Si) per hour. The effect of total dose on maximum frequency is given by the dashed curve while the solid line shows the total dose effects on the propagation delay. Output loading for both propagation delay and maximum frequency measurements was between 20-25 pF.

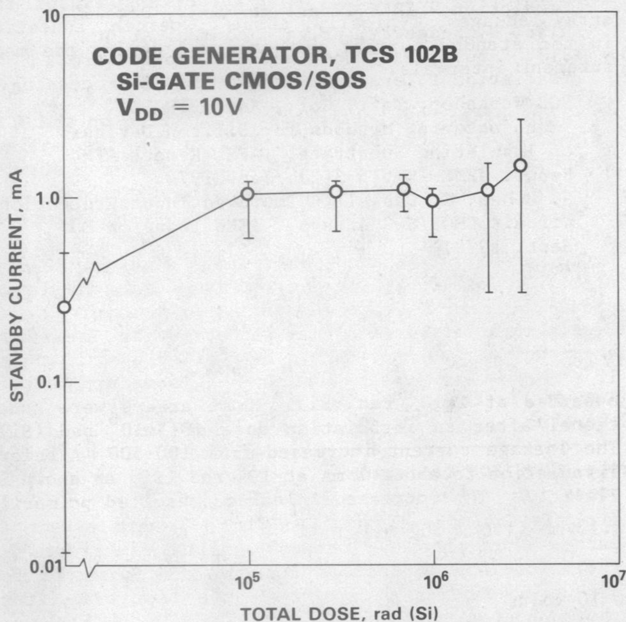


Figure 7. The irradiation induced leakage current as a function of the irradiation dose. The error bars indicate both the variation with the condition of measurement and variability among the devices tested.

To illustrate the transient behavior of the code generator, actual output data near the upset threshold is shown in Figure 8. The center trace shows the proper X_A-code output after the application of the set pulse. The top trace shows the X_A output during and after a 1 μs irradiation pulse. By comparing the top and center traces, it is clear that the proper X_A code is maintained during and after the irradiation pulse. The modification to the logic levels during the radiation pulse is in agreement with the simulations. It should be noted that the proper code output was maintained during irradiation even though the array power supply current increased to 200 mA (10 times the

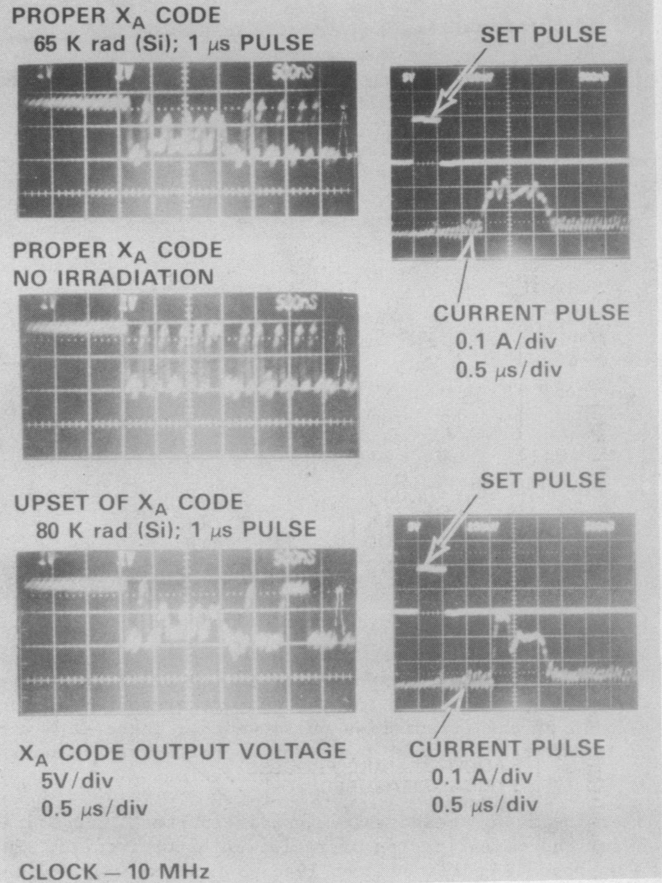


Figure 8. Response of the X_A output of the code generator when irradiated with 1 s LINAC pulses.

normal dynamic current). As is noted on the lower trace, the improper X_A code is generated after the irradiation pulse indicating that in this case an internal register changed state during the irradiation.

The transient error threshold was experimentally determined for the array as a function of irradiation-pulse width. These data are given in Figure 9. The array exhibited a transient-upset threshold near 10^{11} rads (Si)/s for 50 ns pulses. The error bars indicate the spread of four different samples tested. A slight decrease in upset threshold for longer pulses was observed due to the variation of dynamic noise immunity with pulse width.[2] Proper circuit operation was verified in these tests by irradiating the device with different input commands to verify that proper logic operation was maintained. No upset was observed from large threshold shifts (maximum dose 8×10^4 rads in 1 μs).

Conclusions

It has been demonstrated that the Si-gate CMOS/SOS technology can be used to fabricate high-performance radiation-hard large-scale integrated circuits. The performance achieved by the TCS102 code generator is summarized in Table IV. These results were achieved by combining modified designs and processes. It was demonstrated that to achieve the full potential of the radiation-hard CMOS/SOS process, care must be exercised in the design not to compromise either the transient or total dose hardness. In addition, the design procedures outlined also eliminate significant irradiation-bias dependent differences in the radiation response. The approach is, therefore, useful in

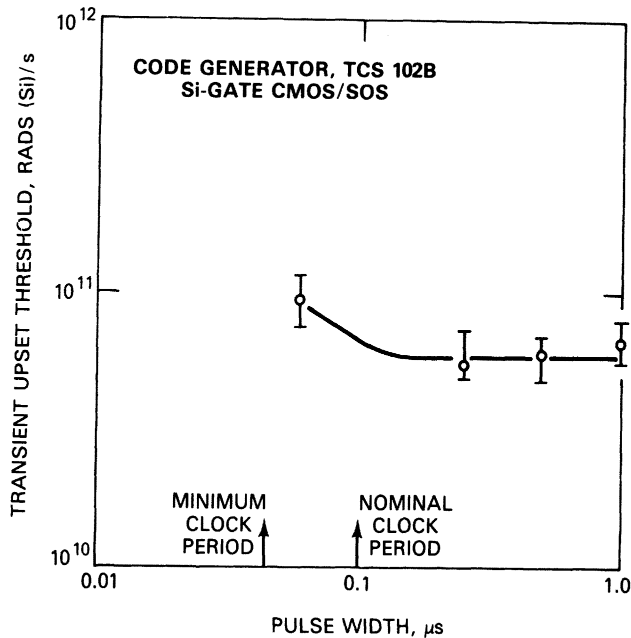


Figure 9. The threshold between acceptable operation and transient upset for the code generator as a function of the irradiation pulse width. These data were taken with the code generator operating at the nominal (10 MHz) clock rate during irradiation.

establishing reasonable irradiation-test procedures for the qualification of radiation-hard circuits. The approaches outlined can lead to custom LSI devices with near nominal performance after 10^6 rad(Si) and achieve error-free operation in excess of 5×10^{10} rad (Si)/s. These arrays can be fabricated without significant compromise to both circuit density and performance.

Acknowledgements

The authors would like to thank G. P. Nelson for providing the EH-4500 tester propagation-delay program, and R. Hevey for contributions to irradiation testing. The work of J. J. Fabula in device processing is also acknowledged.

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TABLE IV

Summary of Typical Characteristics of the Code Generator

Technology	P^+ Si-gate, CMOS/SOS radiation-hard process
Die size	4.83 x 5.13 mm (190 x 202 mils)
Devices	2660
Maximum clock rate	25 MHz @ 10 volts
Active current	20 mA @ 10 MHz
Standby current	0.3 mA @ 10 volts
Radiation parameters transient upset	$0.8\text{-}1.0 \times 10^{11}$ Rad (Si)/s (50 ns) $6\text{-}8 \times 10^{10}$ Rad (Si)/s (1 μs)
Total dose	10^6 Rad (Si)