

# An Automatic Test Set for the Dynamic Characterization of A/D Converters

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**Abstract**—An automatic test set is described for measuring the dynamic characteristics of A/D converters having up to 16 bits of resolution. The test converter is exercised with stepped input changes typical of the conditions of actual use. All dynamic test parameters are under program control, making it possible to separate and measure dynamic errors of various sources. Typical test results are included.

## INTRODUCTION

OVER THE PAST several years, the need for appropriate calibration support for A/D converters has become rather widely recognized. This is demonstrated by the increasing number and sophistication of articles on converter testing appearing in the trade literature, and by the advent of several commercial test systems capable of characterizing A/D converters of low to moderate resolution ( $\leq 12$  bits). Nevertheless, the emphasis to date has been on methods of static characterization, while relatively few dynamic test techniques have been developed, particularly for converters having resolution greater than 8 or 10 bits. And yet, the majority of A/D converters are called upon to process dynamic signals, generated either by multiplexing quasi-static signals or from externally sampled, dynamic stimuli. To address this need for dynamic test methods, a technique was recently proposed by one of the authors for obtaining the dynamic characteristics of high-resolution ( $>12$  bits) A/D converters [1]. This technique has now been incorporated into an automatic test set, the design, performance, and application of which is the subject of this paper.

Dynamic errors in A/D converters can be defined as any deviations from the static transfer characteristic resulting from prior exercise, i.e., previous changes in input. Typical error sources include input buffer settling limitations, the transient response of the internal analog comparators, dielectric absorption, and errors related to thermal effects in critical resistors, input buffers, or comparators. With the measurement technique employed in this test set, dynamic errors are measured in terms of the changes in the test converter's code transition levels resulting from prior exercise. This exercise is provided by means of accurately known, fast-settling input voltage steps. Since all but the slowest integrating-type A/D

converters are usually preceded by either a multiplexer or an S/H amplifier, this stepped input gives a good representation of the dynamic input conditions characteristic of actual use. In the automatic test set, any pair of levels within the dynamic range of the test converter can be selected under program control to define the voltage steps, as well as the code transition levels under test. In addition, the duration of each level is programmable, as is the recovery time allocated for the test converter to respond and settle.

This flexibility makes it possible to develop test programs which are capable of separating and measuring various static and dynamic errors, and their dependence on a number of test parameters. For example, dynamic errors can be tested for their dependence on the pulse level of prior exercise, reference codewords, or pulse duty cycle. Errors can furthermore be measured as a function of recovery time permitted for the test unit. Also, error sources can be separated, for example, according to their associated time constants, making it possible to isolate errors induced by thermal transients from errors due to other dynamic behavior having shorter time constants.

## BASIC PRINCIPLES

As described in [1], the operation of the dynamic test set is based on an extension of the basic principles used by the authors, and others, in characterizing the static performance of A/D converters [2]–[4]. This static method is illustrated in Fig. 1. The test converter is characterized by placing it within a feedback loop which locks the input voltage to a code-transition level defined by the reference codeword to the digital comparator. Input voltages thus developed are measured automatically at a number of input codewords to determine the converter's transfer characteristics.

For a dynamic test, it is desired to measure changes in these code-transition levels resulting from prior exercise. This process is accomplished by switching the converter's input to a programmable (pulse) level different from the designated transition level and back again, as illustrated in Fig. 2. While the unit under test converts when the input is both at the pulsed level as well as the transition level, the feedback samples are latched only following conversions made at the transition level. If the pulse voltage is switched off prior to the next feedback sample, locking at the reference level can be maintained. Referring to the timing diagram of Fig. 3, note that the feedback voltage represented by dashed lines changes only slowly during open-loop periods due to the long time constant of integration.

Manuscript received August 23, 1982. This work was partially funded by the Calibration Coordination Group of the U.S. Department of Defense.

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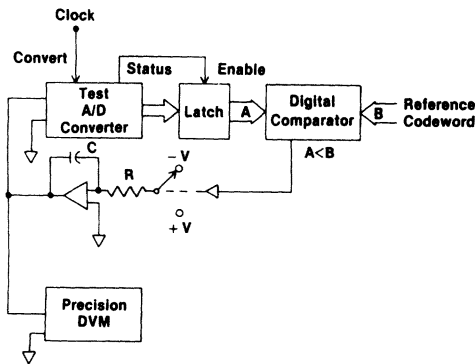


Fig. 1. Transition-locking feedback loop employed in static A/D converter testing.

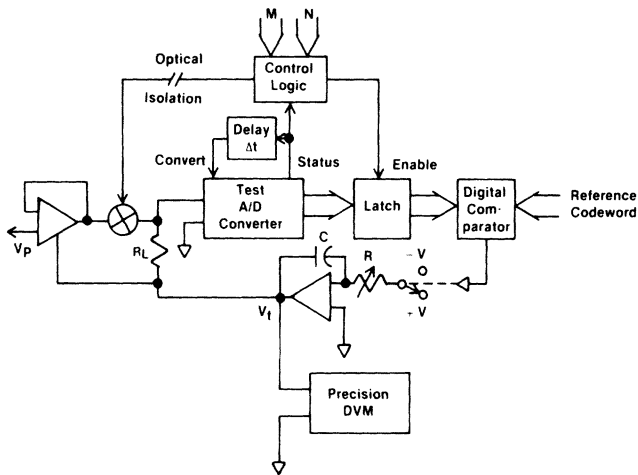


Fig. 2. Circuit for dynamic A/D converter testing: transition-locking feedback loop in conjunction with dynamic step generator.

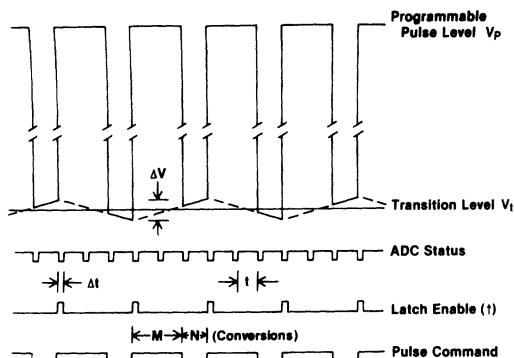


Fig. 3. Timing diagrams showing timing relationships between control signals and input voltage to test converter.

This change is given by

$$\Delta V = (V/RC)(M + N)(t + \Delta t)$$

where

- $V$  input voltage to integrator,
- $M$  number of conversions made with input at pulse level,
- $N$  number of conversions made with input at transition level,

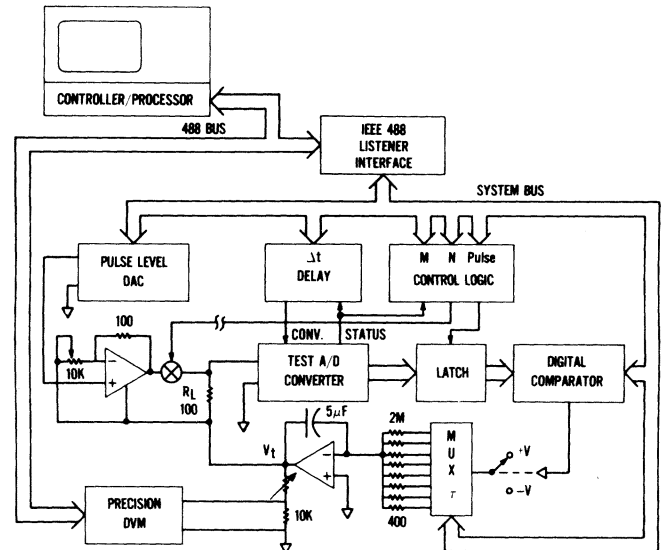


Fig. 4. Complete block diagram of dynamic test set.

- $t$  conversion duration of test unit,
- $\Delta t$  time delay to allow for pulse to return to zero and test unit to respond,
- $RC$  time constant ( $\tau$ ) of integrator.

Any dynamic response error due to this step change will be manifested as a change in the code-transition level maintained by the feedback loop, and can thus be measured by the DVM.

## DESIGN CONSIDERATIONS

A block diagram of the complete test set is given in Fig. 4. Overall control is provided via the IEEE-488 bus, for which an internal hard-wired listener interface has been provided. This bus interface, in turn, drives a system bus to distribute data for controlling all important operating parameters, including reference codeword, pulse level, delay time, pulse control and duty cycle parameters  $M$  and  $N$ , and integration time constant  $\tau$ . The actual measurements of transition voltage are made with a 6  $\frac{1}{2}$ -digit DVM which transmits data directly to the controller/processor via the 488 bus.

### Pulse Circuit

As Figs. 2 and 4 illustrate, the voltage steps are produced by summing the integrator's output voltage with a voltage pulse developed across a series resistor  $R_L$ . These pulses, turned on and off by a switch controlling current flow through the resistor, settle quickly to zero when the switch is turned off, since active components are isolated from the circuit at that time. During this switching, the transition voltage  $V_t$  maintained by the integrator will remain constant, provided only that the integrating amplifier has a low dynamic output impedance. Therefore, a voltage step having fast, accurate settling from the pulse level to the transition level is produced which settles to within 2 ppm of the static value in 2  $\mu$ s. The pulse circuit is shown in more detail in Fig. 5. Switching is accomplished with a junction FET having  $\leq 2\text{-}\Omega$  ON resistance and greater than

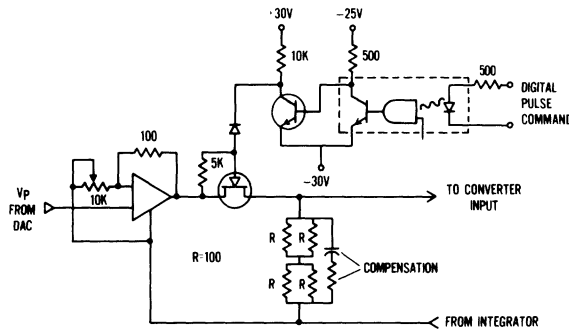


Fig. 5. Detailed diagram of pulse circuit.

30-V breakdown voltage, controlled by a bipolar transistor stage. This circuitry is optically isolated from the test set logic to facilitate the necessary level shifting and to eliminate ground loops. To minimize errors resulting from the FET switch feedthrough, the follower amplifier supplying the pulse voltage was selected for high speed and fast settling. In addition, this amplifier must be capable of supplying output current up to 200 mA to produce a full-scale voltage drop of 20 V across a 100- $\Omega$  load resistor. The follower-with-gain configuration of this amplifier is used to correct for the 2-percent pulse voltage errors which result from the finite ( $\sim 2\text{-}\Omega$ ) ON resistance of the switch, in series with the 100- $\Omega$  load resistor. This correction technique is limited by a variability in the ON resistance of  $\sim 5$  percent, so that the remaining error in the corrected pulse voltage is  $\sim 0.1$  percent. The entire pulse circuitry is powered from a  $\pm 30\text{-V}$  supply whose common terminal is driven by the output of the operational integrator. The 600 pF of capacitance to ground of this supply causes no stability problems in the integrator since it is in series with the distributed impedance of the power supply transformer windings.

The 100- $\Omega$  value for load resistor  $R_L$  was chosen to minimize the settling time while keeping the current and power at manageable levels. Even so, the maximum power to be dissipated in  $R_L$  is 4 W, and this amount necessitated using four low-temperature coefficient wire-wound resistor cards to dissipate the power without incurring significant errors due to resistance change. The maximum tolerable change in resistance is determined by the input impedance of the test converter to which this resistance is added, and by the maximum allowable uncertainty in the measurement. Taking the maximum allowable uncertainty to be  $1/16$  LSB, the maximum permissible resistance change is given by

$$\epsilon = \Delta R_L / R_L = 2^{-(n+4)} (R_{in} / 100 \Omega)$$

where  $n$  is the converter resolution in bits and  $R_{in}$  is the input impedance. For a maximum load of 1 W/resistor,  $\epsilon$  gives the maximum tolerable load coefficient, expressed in proportional parts per watt. The worst case design conditions were considered to be  $N = 16$  (for which  $1/16$  LSB = 1 ppm) and  $R_{in} = 5 \text{ k}\Omega$ , giving  $\epsilon = 50 \text{ ppm/W}$ . These conditions were met with the low-temperature coefficient wire-wound cards. However, while the power dissipation problem was solved using wire-wound resistors, their use increased the settling time somewhat because of series inductance. This effect was largely overcome by a parallel RC compensating network, as shown in Fig. 5.

### Timing Circuits for $M$ , $N$ , and $\Delta t$

The timing for the test set is orchestrated by the blocks in Fig. 4 labeled "DELAY" and "CONTROL LOGIC." These blocks, upon receiving the test parameters  $M$ ,  $N$ , and  $\Delta t$ , establish the timing relationships shown in Fig. 3. Thus input-voltage steps are always made immediately following the end of a conversion, as indicated by the test converter's "status" line. The delay  $\Delta t$  then immediately follows before the next conversion is initiated, providing a programmable duration for the input step to settle and the test converter to respond. With the input at the pulse level  $V_P$ , the converter makes  $M$  conversions, after which the input is switched to return to the transition level  $V_I$ , at which  $N$  conversions are made. The data from the last ( $N$ th) conversion at the transition level are then latched at the digital comparator's input to provide the feedback for controlling the transition voltage. For static tests, a pulse command from the controller inhibits the switch control, so that all  $M + N$  conversions are made at the transition level.

The circuits in both the "DELAY" and "CONTROL LOGIC" blocks are implemented with presetable counters. The  $\Delta t$  counters are driven with a 10-MHz clock so that the delay can be programmed with 100-ns resolution. The "status" level from the test converter provides the clock input for counters controlling  $M$  and  $N$ .

### Integration Time Constant $\tau$

It is desirable that the rate of change of  $V_I$  be matched to the specific test converter and operating conditions, so that the transition voltage does not change significantly ( $\Delta V \leq 1/16 \text{ LSB}$ ) during one feedback interval. Yet  $V_I$  must also be permitted to change fast enough to respond quickly to transition level shifts caused by dynamic exercise. While the rate of change of  $V_I$  could be controlled by varying either the integrator's input voltage or the integration time constant, the latter approach was taken to minimize the effects of offset voltage which could cause significant errors when small values of  $V$  would be required. The time constant is programmed by selecting one of eight input resistors, using an integrated circuit analog multiplexer, as shown in Fig. 4. The resulting eight values of  $\tau$  are adequate for all anticipated test conditions.

This time constant circuit, in addition, provides a fast search capability which is desirable when locking onto a transition level far removed from the previous one. To minimize the time required for  $V_I$  to ramp to the new level, the time constant is programmed initially for a faster rate of change and then to return to the slower rate after the new level has been reached. The maximum time required to acquire a new level in this manner is 2 s.

### Controls

The ranges of automatic control for the various test parameters are as follows:

$M$ :	1–99 conversions
$N$ :	1–9 conversions
$\Delta t$ :	0.1–99.9 $\mu\text{s}$
$V_P$ :	–10.0 to 9.92 V (8-bit resolution)



Fig. 6. Photograph of dynamic test set with test converter in place. Precision DVM used to measure transition voltage is below the test set.

Codeword: up to 16 bits  
 $\tau$ : 2 ms to 10 s in 8 steps  
 Pulse: OFF-ON.

The span of values for  $M$  and  $N$  permits the pulse level duty cycle to range from 10 to 99 percent.

Additional manual controls are provided to accommodate different coding and control formats for the test unit, and to correct for a systematic error which is proportional to input impedance. This impedance-dependent error arises because the voltage drop across the load resistor  $R_L$ , when the switch is off, causes the voltage  $V_i$  to deviate from the actual transition voltage at the converter's input. The resulting error is a simple function of input impedance, and is easily corrected by providing the necessary attenuation of  $V_i$  at the input to the DVM.

The complete test set is shown in Fig. 6.<sup>1</sup> A test converter is in place on the table provided at the front and the precision DVM is under the test set. Displays on the top panel indicate the operating parameters, including the reference codeword, the pulse voltage  $V_p$ , and the values of  $M$ ,  $N$ , and  $\Delta t$ . Not shown is the graphic display terminal which serves as the controller/processor.

#### SOURCES OF ERROR

A number of potential error sources affect the performance of the test set. Perhaps the most obvious one is the measurement uncertainty associated with the DVM which measures the transition levels. However, since the test set is primarily intended to measure only relatively small changes in transition levels resulting from dynamic exercise, absolute accuracy and

integral linearity are not critical specifications for this purpose. Consequently, several commercial DVM's are capable of making the required difference measurements with uncertainties no greater than 2–3 ppm, provided that averages of several readings are used to improve the precision.

The most critical elements of the test set itself are the circuits supplying the input signals to the test converter, including the pulse circuit and the operational integrator. Possible error sources in these elements include voltage step settling limitations, finite dynamic output impedance and thermal changes in the integrator, errors in the pulse level, and leakage current in the junction FET switch.

The settling time of the pulse returning to the transition level has been measured at the test converter's input using the second circuit described in [5]. The pulse was found to return to within 2 ppm (of full-scale range) of the transition level in under 2  $\mu$ s following a step change of 20 V. The limiting factor for the settling time is thought to be feedthrough of the gating signal through the 60 pF of FET gate-drain capacitance. Additional observations at the integrator's output during pulse switching revealed that the switching transients have an area of less than  $10^{-9}$  V  $\cdot$  s, and level changes are less than  $\frac{1}{2}$  ppm. Thus the average value (to which the DVM responds) will normally change by no more than 1 ppm. This test checks the effects of both output impedance and thermal changes.

Errors due to switch leakage current are minimized by maintaining adequate gate pinchoff voltage for all test conditions. For this reason, the gate is driven to 30 V below  $V_t$  for turn-off, to allow a pinchoff voltage of  $-10$  V under the most extreme condition at which  $V_t = +10$  V, and  $V_p = -10$  V. This design limits the leakage current to less than  $10^{-7}$  A, producing an error voltage across  $R_L$  of less than 10  $\mu$ V.

Finally, as was discussed previously, the pulse voltage has a maximum uncertainty of about 0.1 percent. In the tests made to date on specimen converters, there has been no indication that greater pulse level accuracy is required. This seems reasonable, since the pulse serves only to provide exercise, while the critical measurements are made at the well-defined transition levels. If further experiments indicate greater pulse level accuracy would be useful, a reasonable approach would be to establish the pulse level in terms of a second code-transition level, using a second feedback loop whose feedback samples are taken at the pulse level and alternate with those of the first loop. With this implementation, both levels,  $V_p$  and  $V_t$ , would then be precisely defined in terms of code-transition levels.

#### TEST PROGRAMS AND PROCEDURES

To fully characterize an  $n$ -bit A/D converter on a static basis requires  $2^n - 1$  measurements, a job which is manageable in a reasonable time only for  $n \leq 12$ . For dynamic testing, the number of measurements required to characterize the response to every possible step change is the square of this number, which is about 17 million for  $n = 12$ , and over 4 billion for  $n = 16$ . And even if all of these measurements were made, the effects of pairs of steps, taken in succession, would not have been determined; and so on, *ad infinitum*. Clearly, a highly simplified menu of test conditions is required for dynamic

<sup>1</sup> Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

testing. With this in mind, the operating programs for the test set were developed to isolate and measure errors of several generic types thought to be the most common and prominent; others will likely be discovered as experience accrues.

Thus, for example, it was felt that some dynamic errors would have relatively short time constants, i.e.,  $\leq$  one conversion period while others, perhaps caused by thermal or dielectric absorption problems, might have substantially longer time constants. These latter effects would likely be dependent on the time spent at a previous level. In addition to the duration and sequence of input steps, errors would also be expected to be dependent on the actual levels of the present and previous steps. The approach used to separate and measure the various error types follows.

Error sources having long and short time constants can be separated by changing  $N$ , the number of conversions made at the transition level, from one to two or greater. Errors of short time constant will disappear after the second try ( $N > 1$ ), while errors of longer time constant will remain. Errors with very long time constants ( $> 1$  s) due, for example, to thermal effects in discrete components, will show up as drift in subsequent DVM readings. To detect and separate these errors 1) a static test is first made at the reference transition level with the pulse turned off. Next, to accentuate thermal stress or other integrating effects, 2) the pulse duty cycle is programmed to 90 percent by setting  $M$  (the number of conversions made at the pulse level) to nine, and  $N$  to one, and a second measurement is made. Another dynamic measurement 3), is then made at the same duty cycle but with  $M = 18$  and  $N = 2$ . By subtracting the result of 1) from that of 2), the net dynamic error is obtained. On the other hand, subtracting 1) from 3) will give only those errors having long time constants. Finally, assuming the errors add linearly, subtracting 3) from 2) will remove the long-time constant errors, leaving only those of short-time constant. For these three steps, the time delay  $\Delta t$  is usually set to a value just long enough to assure that the voltage step has settled within the required error bounds. On the other hand, a fourth measurement, made with  $M = 9$ ,  $N = 1$ , and  $\Delta t$  increased by one conversion period, has been found to elucidate another important type of error. It might have reasonably been expected that this set of conditions would give the same values as does 3) above, since the time periods are identical. Nevertheless, striking differences can occur. In successive approximation converters these differences apparently result from the internal DAC remaining in the state determined by the last encoding. In case 4), following the return to the transition level, the converter remains idle for one conversion period before making a conversion, while in case 3), a first conversion is made (but ignored) during this interval. By subtracting 3) from 4) then, errors related to the previous digital state are uncovered. This last effect has been found to be very common, existing to a significant degree in almost all converters tested, regardless of resolution.

Two BASIC language programs to implement these tests have been developed thus far; one in which the pulse level is fixed and errors are measured and plotted as a function of the codeword, i.e., transition level, and another in which the codeword is specified, and errors are plotted against pulse level. For either program, errors are measured at all four test conditions described above for each new codeword or pulse level.

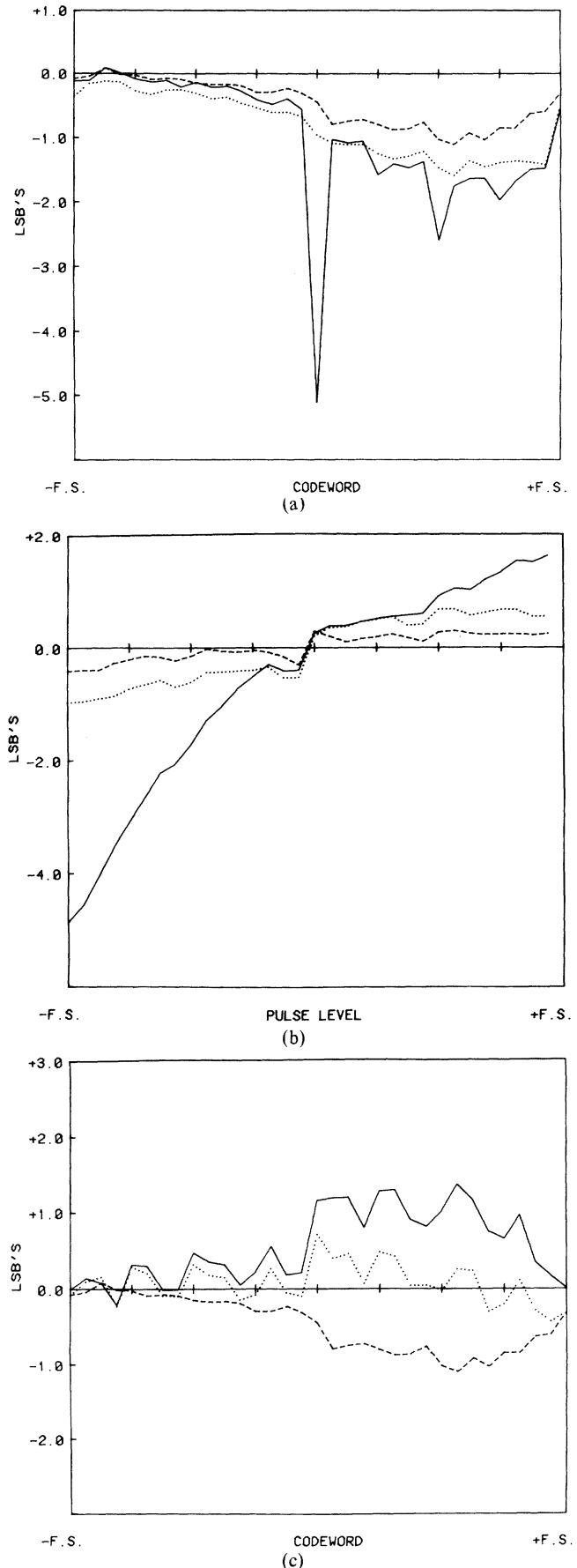


Fig. 7. Dynamic errors for a 16-bit, 30- $\mu$ s converter. (a) Errors versus reference codeword, with pulse level = -10 V: Solid— $M = 9$ ,  $N = 1$ ,  $\Delta t = 5 \mu$ s. Dashed— $M = 18$ ,  $N = 2$ ,  $\Delta t = 5 \mu$ s. Dotted— $M = 9$ ,  $N = 1$ ,  $\Delta t = 35 \mu$ s. (b) Errors versus pulse level with reference codeword = 1000. Curves same as in (a). (c) Errors versus codeword, with pulse level = -10 V: Solid—static errors. Dashed— $M = 18$ ,  $N = 2$ ,  $\Delta t = 5 \mu$ s. Dotted—solid plus dashed, i.e., static plus dynamic errors.

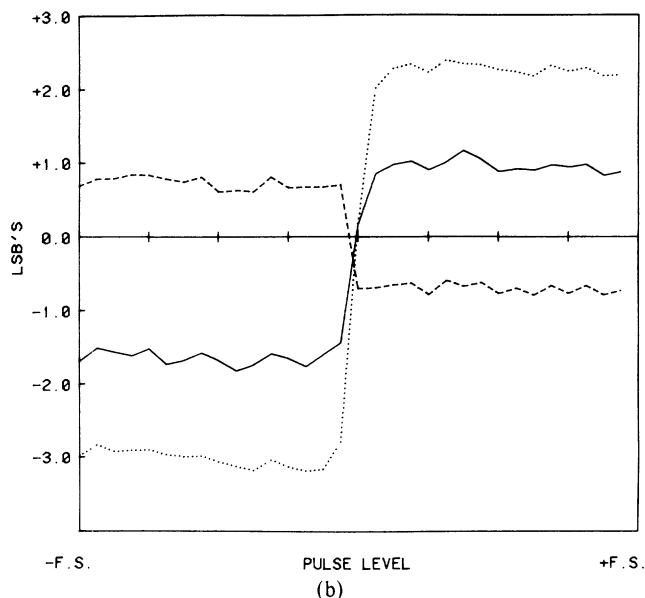
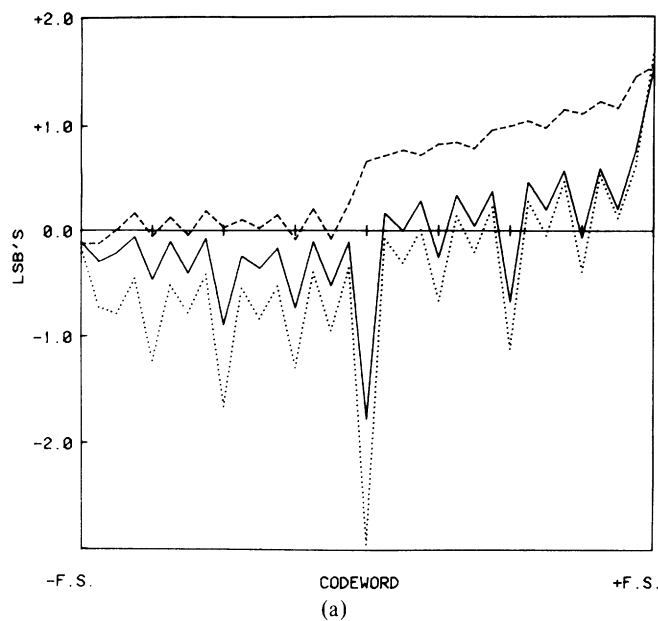


Fig. 8. Dynamic errors of 16-bit, 50- $\mu$ s converter from different manufacturer. (a) Dynamic errors versus reference codeword, with pulse level = -10 V: Solid— $M = 9$ ,  $N = 1$ ,  $\Delta t = 5.0 \mu$ s. Dashed— $M = 18$ ,  $N = 2$ ,  $\Delta t = 5.0 \mu$ s. Dotted— $M = 9$ ,  $N = 1$ ,  $\Delta t = 55.0 \mu$ s. (b) Dynamic errors versus pulse level, with codeword = 1000... Curves same conditions as in (a).

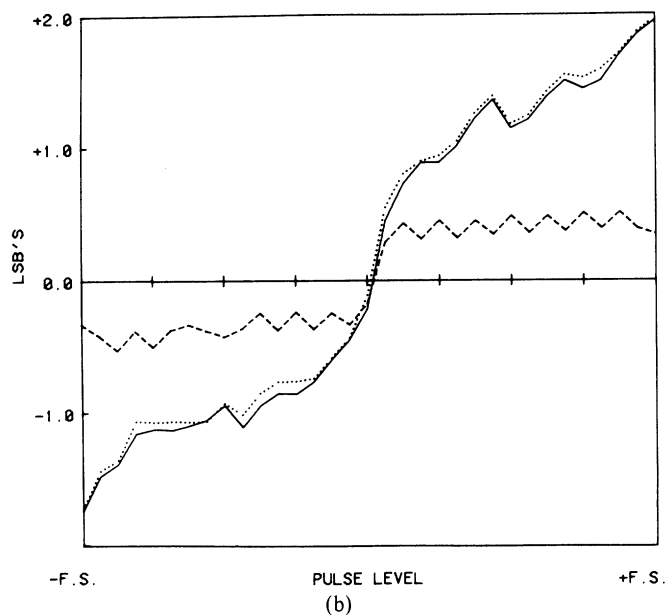
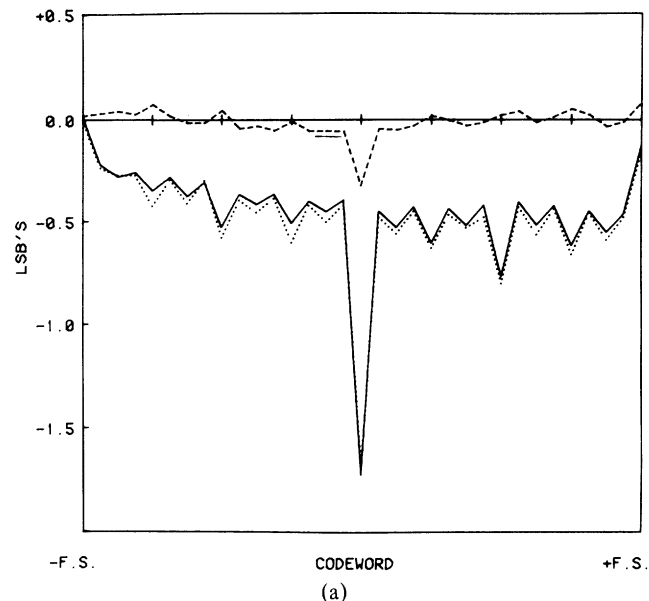


Fig. 9. Dynamic errors of 12-bit, 4- $\mu$ s converter. (a) Dynamic errors versus reference codeword, with pulse level = -10 V: Solid— $M = 9$ ,  $N = 1$ ,  $\Delta t = 3.0 \mu$ s. Dashed— $M = 18$ ,  $N = 2$ ,  $\Delta t = 3.0 \mu$ s. Dotted— $M = 9$ ,  $N = 1$ ,  $\Delta t = 7.0 \mu$ s. (b) Dynamic errors versus pulse level, with codeword = 1000... Curves—same conditions as in (a).

The independent variable normally ranges over 33 values, evenly spaced from minus full-scale to plus full-scale. Thus for either program, measurements are made under 132 ( $33 \times 4$ ) different test conditions. The test time is limited primarily by the time required for the test unit to reach thermal equilibrium after each new test condition, and by the conversion rate of the DVM as well as the number of samples required for averaging. A full test will usually require from 5 to 15 min to complete, depending on the type and resolution of the test unit.

#### TYPICAL TEST RESULTS

Typical test results, obtained from one 12-bit and two 16-bit A/D converters, are plotted in Figs. 7-9. Note that all errors are expressed in LSB's of the test converter, with one LSB equalling 244 ppm for a 12-bit, and 15 ppm for a 16-bit converter. Fig. 7(a) and (b) represents the dynamic errors of a 16-bit converter having a 30- $\mu$ s conversion time, plotted first

as a function of codeword with the pulse level fixed at -10 V, and then as a function of pulse level with the codeword fixed at the major transition (1000...). In both figures, the solid, dashed, and dotted curves, respectively, represent conditions 2)-1), 3)-1), and 4)-1), as discussed in the previous section. (Conditions 2)-3) and 4)-3), also referred to in that section, are seen to be the differences between these curves, i.e., (solid) - (dashed), and (dotted) - (dashed).) Thus the solid curve represents errors measured with  $M = 9$ ,  $N = 1$ , and  $\Delta t = 5.0 \mu$ s, the dashed curve gives errors with  $M = 18$ ,  $N = 2$ ,  $\Delta t = 5.0 \mu$ s, and the dotted curve represents errors measured at  $M = 9$ ,  $N = 1$ , and  $\Delta t = 35.0 \mu$ s. Note that the large peaks which are present in the solid curve disappear in the dotted curve, after a recovery of one conversion period is permitted. This result indicated a short time constant settling time problem, and the cause was traced to settling limitations of an input buffer amplifier. Additional improvement was seen in the



dashed curve, for which a second conversion was made in place of the added delay. In this case, the resetting of the internal DAC to correspond to the new input conditions seems to be responsible for the improvement. The remaining errors shown in this plot apparently comprise, at least in part, thermally induced errors having a time constant substantially longer than two conversion periods. In fact, in Fig. 7(c) the dashed curve is replotted from Fig. 7(a) along with a plot (solid) of the static errors of the converter. The sum of the two—static plus dynamic—is represented by the dotted curve. Note that the curve of the combined characteristics gives the total errors under the specified dynamic conditions. The fact that the errors are smaller in this particular case than under static conditions indicates that the thermally induced errors only occur when the test unit “soaks” at each measured level, as happens in a static test. Fig. 7(b) shows the input buffer settling limitations as a function of pulse level. The settling problem is most pronounced at the major transition because, at that input level, the first decision in the chain of successive approximation is the most critical. Therefore, to incur no error, the input voltage must completely settle before this first decision is made.

Dynamic errors of another 16-bit converter from a different manufacturer are plotted in Fig. 8(a) and (b). The test conditions for the three curves of each figure are the same as in the previous examples. In the plot of errors versus pulse level (Fig. 8(b)), in which the reference codeword has been fixed at midscale, note the threshold characteristic as the pulse level crosses midscale voltage. This behavior suggests a recovery problem in an internal comparator whose input is diode bounded. Note also that, contrary to what might be expected, the errors actually become larger when a longer recovery time

is permitted, as is seen in the difference between the solid and dotted curves.

Finally, in Fig. 9(a) and (b) are plotted the errors of a 12-bit, 4- $\mu$ s converter. From the figure it can be seen that providing the additional recovery time again has little effect, while permitting a second try at the new level substantially reduces the dynamic errors. Therefore, while similar in appearance to the error plot for the 16-bit converter of Fig. 7(a), the large error at midscale in this case is due not to a settling time problem, but more likely to an overload recovery problem.

It can be seen from these plots that the test set is capable of measuring dynamic errors with high precision, while at the same time being able to discriminate between various types of errors. With this capability the test set could prove useful in the design of high-resolution converters, as well as in acceptance testing. It is also evident from the data in these plots that dynamic as well as static tests are required to adequately characterize the performance of A/D converters under actual operating conditions.

#### REFERENCES

- [1] T. M. Souders, “A dynamic test method for high-resolution A/D converters,” *IEEE Trans. Instrum. Meas.*, vol. IM-31, no. 1, pp. 3–5, Mar. 1982.
- [2] T. M. Souders and D. R. Flach, “An automated test set for high resolution analog-to-digital and digital-to-analog converters,” *IEEE Trans. Instrum. Meas.*, vol. IM-28, no. 4, pp. 239–244, Dec. 1979.
- [3] T. M. Souders, D. R. Flach, and B. A. Bell, “A calibration service for analog-to-digital and digital-to-analog converters,” Nat. Bur. Stand. (U.S.), NBS Tech. Note 1145, July 1981.
- [4] J. J. Corcoran, T. Hornak, and P. B. Skov, “A high-resolution error plotter for analog-to-digital converters,” *IEEE Trans. Instrum. Meas.*, vol. IM-24, no. 4, pp. 370–374, Dec. 1975.
- [5] H. K. Schoenwetter, “High-accuracy settling time measurements,” this issue, pp. 22–27.