

# Multidimensional Turbo Product and Generalized LDPC Codes with Component RS Codes Suitable for use in Beyond 100 Gb/s Optical Transmission

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**Abstract** — We present two hard-decision decoding schemes suitable for use in beyond 100 Gb/s optical transmission. The first scheme is based on multidimensional turbo product codes (MTPCs) with component Reed-Solomon (RS) codes. The second scheme is based on generalized low-density parity-check (GLDPC) codes with component RS codes. The proposed schemes perform comparable to recent concatenation of RS and LDPC codes proposal, and solve the problem of nonexistence of A/D converters operating above 100 Gb/s.

**Keywords** — 100 Gb/s Ethernet, forward error correction (FEC), Reed-Solomon (RS) codes, multidimensional turbo product codes (MTPCs), generalized LDPC (GLDPC) codes

## I. INTRODUCTION

The network providers already consider the 100 Gb/s per dense wavelength-division multiplexing (DWDM) channel transmission for future optical networks. The bit-error ratio (BER) performance of such systems is degraded significantly due to intrachannel fiber nonlinearities, polarization mode dispersion (PMD), and chromatic dispersion. In order to overcome those challenges, novel advanced techniques and devices in modulation, detection, coding and signal processing are required. The development of a novel powerful forward error correction (FEC) scheme suitable for beyond 100 Gb/s transmission and 100Gb/s Ethernet is of high importance [1],[2].

The soft iteratively decodable codes [1]-[7], turbo-product codes (TPCs) and LDPC codes, are excellent candidates for use in high-speed optical communications. Although those schemes provide excellent performance improvement, they require soft bit reliabilities, and as such are still not implementable at data rates above 100 Gb/s. Given the lack of A/D converters operating at data rates  $\geq 100$  Gb/s, we propose two FEC schemes: (i) the FEC scheme based on multidimensional TPCs (MTPCs) with component Reed-Solomon (RS) codes [8], and (ii) the generalized LDPC (GLDPC) codes with component codes being either MTPCs or RS codes. These schemes operate on hard decisions only,

and provide competitive coding gains compared to a soft decision scheme, based on concatenation of an LDPC code and a RS code, proposed in [2] as possible candidate for 100Gb/s transmission. We further study the BER performance of the proposed schemes when used in combination with multilevel modulation schemes, such as  $M$ -ary QAM. The three-dimensional (3D)-TPC of rate 0.8, based on (255,237) RS code as a component code, provides the net effective coding gain of 9.3 dB at BER of  $10^{-15}$ . This scheme outperforms standard RS(255,239) code by 2.1 dB at BER of  $10^{-10}$ . On the other hand, the GLDPC code of rate 0.82, based on (255,239) and (255,223) RS codes as component codes, provides the net effective coding gain of 9.6 dB at BER of  $10^{-15}$ , and outperforms standard RS(255,239) code by 2.5 dB at BER of  $10^{-10}$ .

## II. MULTIDIMENSIONAL TPCs AND GLDPC CODES WITH COMPONENT RS CODES

The multidimensional turbo-product codes, proposed here, are generalization of turbo-product codes proposed by Elias [9]. The  $D$ -dimensional turbo product code is an  $(n_1 n_2 \dots n_D, k_1 k_2 \dots k_D, d_1 d_2 \dots d_D)$  code in which code words form an  $n_1 \times n_2 \times \dots \times n_D$  array such that  $i$ th dimension code word is obtained from an  $(n_i, k_i, d_i)$  code  $C_i$ . With  $n_i$ ,  $k_i$  and  $d_i$  ( $i=1, 2, \dots, D$ ) we denoted the codeword length, dimension and minimum distance, respectively, of  $i$ th component code. An example of 3-dimensional TPC, with RS component codes, is shown in Fig. 1.

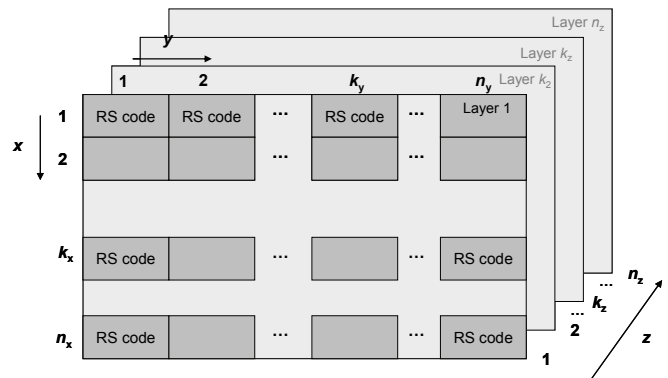


Fig. 1. A multidimensional TPC codeword example

The different options to perform encoding/decoding can be classified as: (i) serial, (ii) parallel, and (iii) partially parallel.

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In serial version, only three different encoders/decoders are needed, each performing encoding/decoding in corresponding dimension. If the component RS codes are identical, only one RS encoder/decoder is needed. The encoding/decoding latency of this scheme is high, but the complexity is low. In parallel implementation, we need  $n_y n_z$  encoders/decoders performing the encoding/decoding in x-direction,  $n_x n_z$  encoders/decoders performing the encoding/decoding in y-direction; and  $n_x n_y$  encoders/decoders performing the encoding/decoding in z-direction. The encoding/decoding latency of this scheme is low, while the encoding/decoding complexity is high. As the compromise between those two schemes we propose to implement the partially parallel scheme. One possible version is described next. It requires  $n_y$  encoders/decoders performing encoding/decoding in x-direction,  $n_x$  encoder/decoders performing encoding/decoding in y-direction, and  $n_z$  encoders/decoders performing encoding/decoding in z-direction. Particularly simple is the partially parallel scheme for which  $n_x = n_y = n_z = n$  employing identical RS( $n, k$ ) codes operating in parallel, whose BER performance is described in next Section. Next we describe the encoding/decoding process for the partially parallel scheme described above with the different RS encoders being of the same length but of different rates; namely  $R_x = k_x/n$ ,  $R_y = k_y/n$ , and  $R_z = k_z/n$ . The information sequence of bits is converted into bytes of length  $m$  bits. The information sequence of bytes fills the memory locations of layer  $i$  ( $i=1,2,\dots,n_z$ ), organized in a fashion similar to that from Fig. 1.  $k_y$  systematic encoders operate in parallel and generate corresponding code words of length  $n$ . In the second phase,  $n_x$  encoders operate in parallel on  $k_y$  memory locations per rows and generate corresponding code words. This procedure is repeated for different layers by employing the same sequence of encoders. Once the encoding performed per z-layers is over, we perform the encoding in similar fashion per y-layers. Transmission can further be done layer by layers (say in z-direction), by transmitting the code words in column-wise fashion, after appropriate mapping shown in Fig. 2. Before going to the description of transmitter and receiver architectures, let us briefly discuss the error correction capability of this scheme. If identical RS( $n, k$ ) codes of minimum distance  $d$  are used, the minimum distance would be  $d^N$ , where  $N > 2$  is dimensionality of MTPC, which would result in much more powerful scheme than TPC whose minimum distance grows as  $d^2$ . For example, 3D-TPC scheme with RS(255,237) code has the code rate 0.8 and the minimum distance  $9^3=729$  bytes. This scheme is also very efficient in dealing burst of errors due to intrachannel nonlinearities. If  $b_x$  is the burst error capability along x-direction,  $b_y$  along y-direction,  $b_z$  along z-direction; the 3D-TPC would be able to correct the burst error of length  $b = \max(n_y n_z b_x, n_x n_z b_y, n_x n_y b_z)$  bytes. The code rate of an MTPC is determined by

$$R = \prod_{i=1}^N R_i \quad (1)$$

where  $R_i = k_i/n_i$  is the code rate of  $i$ th component code.

The proposed MTPC can be used as constituent code to build the more powerful GLDPC codes with component

MTPCs. The parity-check matrix  $H$  of a Boutros-like [7] nonbinary GLDPC codes can be partitioned into  $W$  sub-matrices  $H_1, \dots, H_W$ .  $H_1$  is a block-diagonal matrix generated from an identity matrix by replacing the ones by the parity-check matrices  $H_i^{\text{MTPC}}$  of the constituent MTPCs of codeword-length  $N$  and dimension  $K_i$ ,  $i=1,2,\dots,N_t/N$ . With  $N_t$  we denoted the code word length of GLDPC code. Each sub-matrix  $H_j$  is derived from  $H_1$  by random permutations  $\pi_{j-1}$  as given below

$$H = \begin{bmatrix} H_1^T & \dots & H_W^T \end{bmatrix}^T, \quad (2)$$

$$H_1 = \begin{bmatrix} H_1^{\text{MTPC}} & 0 & 0 & \dots & 0 & 0 \\ & H_2^{\text{MTPC}} & 0 & \dots & 0 & 0 \\ \dots & & & & & \\ 0 & 0 & 0 & 0 & H_{N_t/N}^{\text{MTPC}} \end{bmatrix}$$

$$H_j = \pi_{j-1}(H_1), \quad j=2,\dots,W$$

For example, let the 3D-MTPC code based on RS(255,247) code be used as constituent code. The corresponding GLDPC code, when  $W=2$ , would be of rate 0.818. The code rate of a GLDPC code is lower bounded by

$$R \geq 1 - W \left( 1 - \frac{\sum_{i=1}^{N_t/N} K_i}{N_t} \right). \quad (3)$$

(The parameters in (3) were introduced earlier.) To reduce the complexity of GLDPC codes someone may use the RS codes as component codes instead of MTPCs.

The transmitter and receiver architectures for RS-based MTPC-coded  $M$ -ary QAM transmission is shown in Fig. 2. The bit streams originating from  $L$  different information sources are converted into bytes and encoded using different  $(N, K_i)$  MTPCs of code rate  $R_i = K_i/N$ .  $K_i$  denotes the number of information bytes of  $i$ th ( $i=1,2,\dots,L$ ) component MTPC, and  $N$  denotes the codeword length, which is the same for all MTPCs. The use of different MTPCs allows us optimally to allocate the code rates. The outputs of  $L$  MTPC encoders are written row-wise into a block-interleaver block. The mapper accepts  $l = \log_2 L$  bytes at time instance  $j$  from the  $(mxn)$  interleaver column-wise, performs nonbinary to binary conversion, and based on  $l$  bits determines the corresponding  $M$ -ary ( $M=2^l$ ) signal constellation point  $s_i = (\phi_{i,i}, \phi_{i,i}) = |s_i| \exp(j\phi_i)$ . The coordinates in  $s_j$  correspond to in-phase and quadrature components of  $M$ -ary QAM constellation. The data phasor  $\phi_i \in \{0, 2\pi/M, \dots, 2\pi(M-1)/M\}$  is sent at each  $i^{\text{th}}$  transmission interval. The outputs at I- and Q-branches at the receiver side, are sampled at the symbol rate, while the symbol log-likelihood ratios (LLRs) are calculated in a *a posteriori* probability (APP) demapper block as follows

$$\lambda(s) = \log \frac{P(s = s_0 | r)}{P(s \neq s_0 | r)}, \quad (4)$$

where  $P(s|r)$  is determined by using Bayes' rule

$$P(s | r) = \frac{P(r | s) P(s)}{\sum_{s'} P(r | s') P(s')}. \quad (5)$$

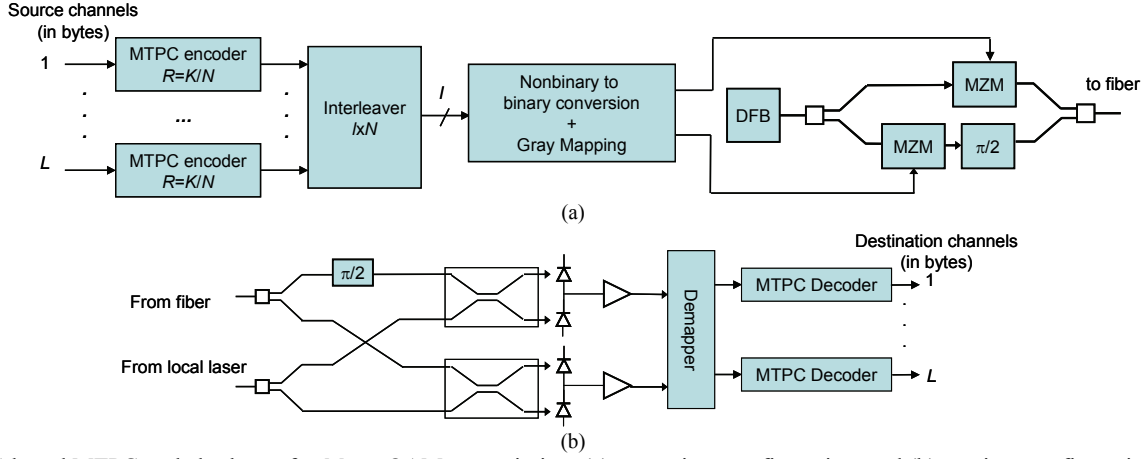


Fig. 2. RS-based MTPC-coded scheme for  $M$ -ary QAM transmission: (a) transmitter configuration, and (b) receiver configuration. MTPC: multidimensional turbo-product code, DFB: distributed feedback laser, MZM: Mach-Zehnder modulator,  $l = \log_2 L$

The symbol  $s = (I_i, Q_i)$  represents the transmitted signal constellation point at time instance  $i$ , while  $r = (r_I, r_Q)$ ,  $r_I = v_I(t = iT_s)$ , and  $r_Q = v_Q(t = iT_s)$  are the samples of I- and Q-detection branches from Fig. 2.  $P(r|s)$  from Eq. (5) is estimated by training based channel estimation. With  $P(s)$  we denoted the *a priori* probability of symbol  $s$ , while  $s_0$  is a referent symbol. The decision symbol is obtained by maximizing the symbol LLRs in (4). Such obtained symbol sequence is converted into binary sequence.

The use of Equations (4)-(5) are suitable for use at lower speeds, such as 10 Giga symbols/s and 40 Giga symbols/s. Due to nonexistence of A/D converters operating above 100 Gb/s, we have to split the constellation diagram into decision regions (see [10] for more details), and perform demapping by means of threshold circuits and logic gates instead. Another option would be to implement the calculations described by equations (4)-(5) in analog domain, using the Hagenauer's approach [11]. With this approach we have to perform the LLR-to-probabilistic domain conversion, conduct calculations in analog domain, and perform probabilistic-to-LLR conversion.

Before decoding starts, we have to convert the bit sequence obtained after detection, into sequence of  $N$  symbols to be used in MTPC decoding. Decoding procedure can be explained as follows.  $n_y$  systematic decoders operate in parallel and generate decoded code words of length  $n$ . In the second phase,  $n_x$  decoders operate in parallel on  $n_y$  memory locations per rows and generate corresponding decoded code words. This procedure is repeated for different layers by employing the same sequence of decoders. Once the decoding performed per  $z$ -layers is over, we perform the decoding in a similar fashion per  $y$ -layers.

### III. EVALUATION OF PROPOSED FEC SCHEMES

We turn our attention to the evaluation of proposed FEC schemes. The results of simulations, assuming a linear channel model, are shown in Figs. 3 and 4 for two different modulation formats, namely  $M$ -ary PSK and  $M$ -ary QAM,

with  $M=2, 4$ , and 16, when the Gray mapping rule is applied. The symbol rate was set to 100 Giga symbols/s. The cases with  $M=2$  and  $M=4$  (with Gray mapping) perform comparable. The first scheme (for  $M=2$ ), based on 3D-TPC code of rate 0.8, based on (255,237) RS code as a component code, provides the net effective coding gain of 9.3 dB at BER of  $10^{-15}$ , and outperforms standard RS(255,239) code by 2.1 dB at BER around  $10^{-10}$ . The second scheme (for  $M=2$ ) provides 2.5 dB improvement over RS(255,239) at BER of  $10^{-10}$ . Given the slope of GLDPC and RS curves we expect larger improvement at lower BERs. GLDPC-coded 16-QAM outperforms GLDPC-coded 16-PSK by about 3.6 dB, and performs 3.7 dB worse than GLDPC-coded QPSK, but carries 4 bits/symbol. The expected net effective coding gain at BER of  $10^{-15}$  is 9.6 dB, which is about 1.5 dB away from the soft-decoding BCH(128,113)xBCH(256,239) TPC code (also shown in Figs. 3 and 4).

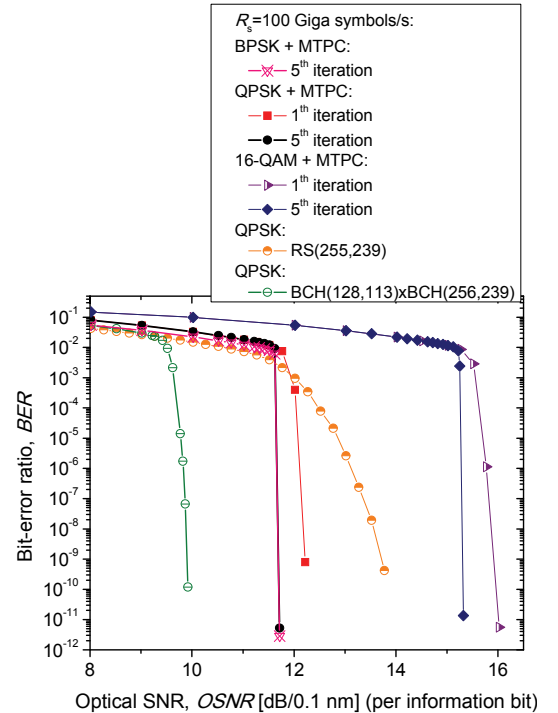


Fig. 3. BER performance of three-dimensional TPC of rate 0.803 with RS(255,237) component code

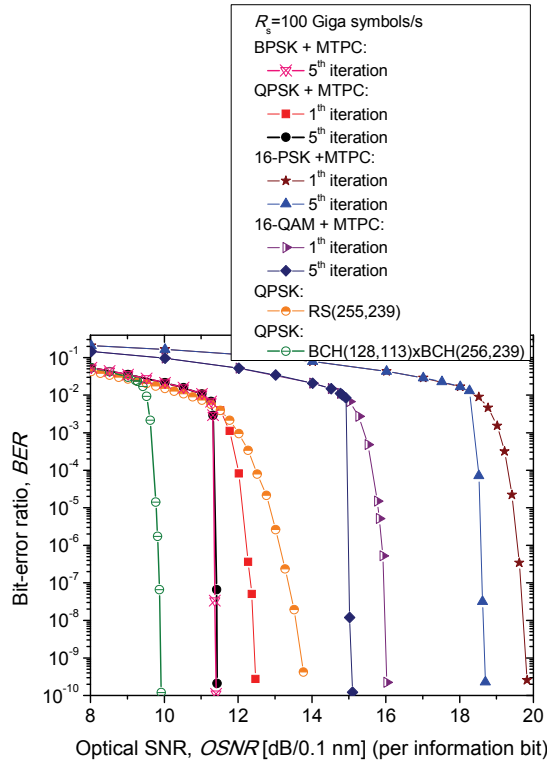


Fig. 4. BER performance of two-dimensional GLDPC of rate 0.82 with RS(255,239) and RS(255,223) component codes

#### IV. CONCLUSION

This paper presents two hard-decision decoding FEC schemes: (i) the first scheme is based on multilevel TPCs with component RS codes, and (ii) the GLDPC codes with component codes being either MTPCs or RS codes. We explain how these schemes can be used in combination with multilevel modulation formats, such as  $M$ -ary QAM. We show that GLDPC-coded 16-QAM outperforms the corresponding 16-PSK scheme by about 3.6 dB. By using the RS-based MTPC in combination with 16-QAM and coherent detection someone may achieve the aggregate rate of 400 Gb/s per wavelength channel, by using the transmission equipment operating at 100 Giga symbols/s. Notice that monolithic silicon coherent receiver operating at 112 Gb/s in aggregate rate has recently been reported in [12], confirming that proposed FEC approach is timely. Through the use of

polarization division multiplexing and selecting the symbol rate 125 Giga symbols/s, the aggregate rate can be further increased to 1 Tb/s per wavelength channel, the option that might be of interest for future 1 Tb/s Ethernet.

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