

# A 112-134 GHz SiGe Amplifier with Peak Output Power of 120 mW

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**Abstract** — A fully-integrated 8-way power combining amplifier for 120 GHz application in an advanced 90 nm SiGe HBT technology is presented. The single-ended PA breakout has a small-signal gain of 20 dB and  $P_{sat}$  of 12.5-13.8 dBm at 114 to 130 GHz. The 8-way power combining PA achieves a small-signal gain of 15 dB and peak  $P_{sat}$  of 20-20.8 dBm at 114-126 GHz with a PAE of 7.6-6.3 %. To our knowledge, this is the highest power silicon-based D-band amplifier to-date.

**Index Terms** — Power amplifier (PA), millimeter-wave (mmW) integrated circuits, silicon germanium (SiGe) HBT, D-band.

## I. INTRODUCTION

Recent work in SiGe technology have demonstrated the capability of generating significant millimeter-wave power at F-band (90 to 140 GHz) and D-band (110 to 170 GHz) with reasonable efficiencies [1]–[4]. Fully-integrated power amplifiers (PAs) at D-band are essential components for frequency multipliers [5], [6] in application of high data-rate communications, imaging systems, and remote sensing. The goal of this work is to achieve power amplifiers capable of delivering an output power >20 dBm for mm-wave systems.

## II. TECHNOLOGY

The 120 GHz PAs are designed using IBM 9HP BiC-MOS process. It is a 90 nm SiGe HBT process built on top of a 90 nm CMOS process, with a 10-layer copper metal backend and high-density MIM capacitors (12.2 fF/ $\mu\text{m}^2$ ). The transistor model from the Cadence library results in a peak  $f_t/f_{max}$  of 300/310 GHz at 1.5-2.5 mA/ $\mu\text{m}$  bias current (Fig. 1). However, with the effect of interconnection parasitic resistance and capacitance from M1 to LD modeled in Sonnet, the peak  $f_t/f_{max}$  drops to 290/250 GHz.

Fig. 1 presents the microstrip transmission line used in the PA design for the matching stubs and the power-combining network. A microstrip line is chosen over G-CPW line due to its lower loss (Fig. 1(c)). The 50  $\Omega$  microstrip line is implemented using the top metal LD with 10  $\mu\text{m}$  width and M2\_4B as ground plan (M1\_4B as Vdd plan). The electromagnetic (EM) simulations using Sonnet results in 0.6-0.8 dB/mm loss at 100-150 GHz (0.9-1.1 dB/mm for a G-CPW line). In practice, and from many different other measurements done on IBM 8HP and

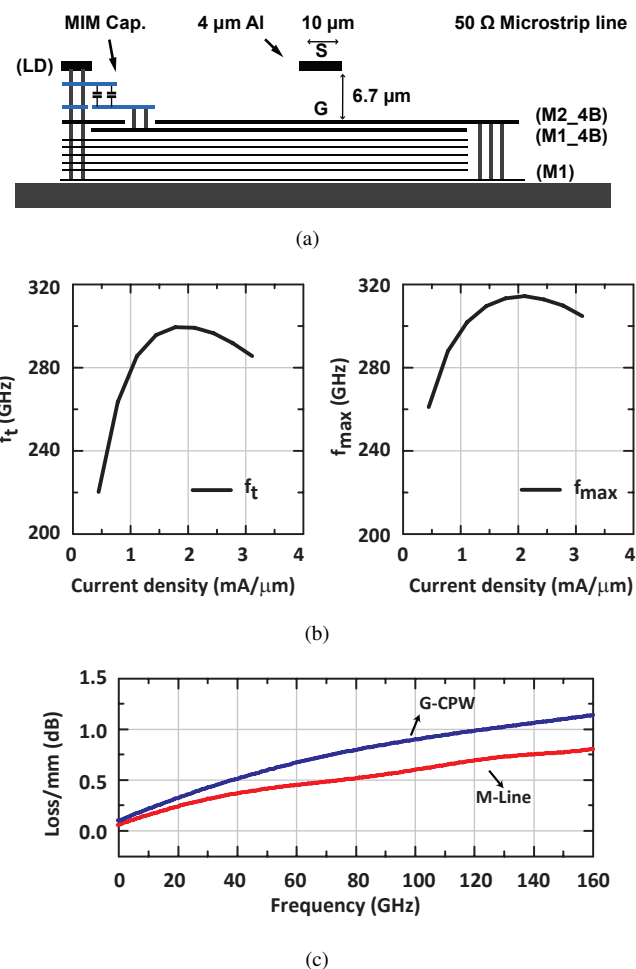


Fig. 1. (a) 50  $\Omega$  microstrip transmission line used in the PA design, (b) simulated  $f_t$  and  $f_{max}$  of 4  $\mu\text{m}$  transistor, and (c) the simulated line loss of 1 mm microstrip line vs. GCPW line.

other processes, the loss is higher than simulated and it is expected that a loss of 1-1.4 dB/mm is achieved at 100-150 GHz.

## III. DESIGN

### A. Single-Ended PA

Fig. 2 presents the schematic of the single-ended PA. The PA consists of four common-emitter gain stages biased

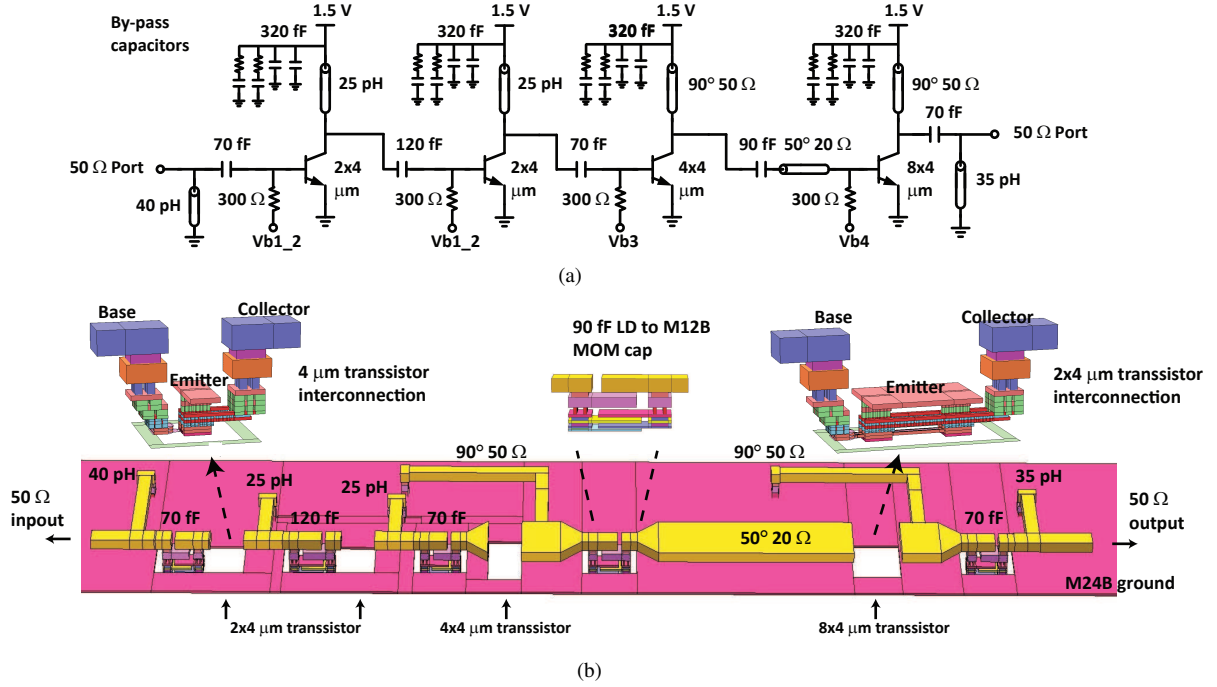


Fig. 2. (a) Schematic of the 120 GHz amplifier, and (b) EM modeling of the 120 GHz amplifier.

in class AB region. Since no foundry power-transistor layout cells are available in the Cadence library, a power transistor is implemented by aggregating smaller, high- $f_t$  npn standard cell. A  $4 \times 0.09 \mu\text{m}^2$  transistor is used as the standard aggregating cell with a single emitter finger, and dual collector, and base fingers (C-B-E-B-C), and are surrounded by a deep-trench isolation ring. The power transistors are biased near their peak  $f_t$  current density at a quiescent current of  $1.2 \text{ mA}/\mu\text{m}$ . The first and second-stage power transistors, Q1 and Q2, consist of two parallel  $4 \mu\text{m}$  npn standard cells while the third stage power transistor Q3 is implemented using four of these standard cells in parallel. The output power transistor Q4 is implemented using four of  $2 \times 4 \mu\text{m}$  npn connected in parallel to form a  $32 \mu\text{m}$  emitter-length device. The first- and second-stage amplifiers provide a small-signal gain of 6 dB gain each at 120 GHz while the third- and fourth-stage provide a gain of 4 to 5 dB each. The third and fourth stage power transistors are scaled by twice the area over the previous-stage transistors to ensure that the output transistor Q4 limits the large-signal compression characteristics. All amplifiers are driven by a 1.5 supplies.

The PA design overcomes the technology's  $1.5 \text{ V } BV_{ceo}$  by presenting a low external base impedance to the power transistor cells [7].  $300 \Omega$  biasing resistors connected at the transistor base nodes are found to have the optimal gain and power performance in the simulation, and the resistors

are implemented using the metal resistor from this process. The resulting effective collector-emitter breakdown voltage allows the output voltage at the collectors to peak above 3.2 V, a factor of 2.1 improvement over  $BV_{ceo}$ .

The EM simulation environment of the matching networks for the 120 GHz PA is shown in Fig. 2(b). The input matching, interstage matching, and output matching networks are implemented using LC-resonant circuits and are all modeled in Sonnet. Compact MOM capacitors, implemented using top metal LD to 6th metal M1\_2B, are widely used in this design as series matching elements where DC-blocks are required. Inductors are implemented using shorted  $50 \Omega$  microstrip lines with different lengths for different inductance values and with associated Q of 14-16 at 120 GHz. MOM capacitors are chosen over MIM capacitors for matching because they show a higher Q value (20-25) than MIM capacitors (10-14). The Vdd stubs connected at the collector nodes of power transistors are followed by dual 320 fF MIM capacitors which are operating close to self resonance and providing a very low impedance ( $\sim 1 \Omega$ ) at 120 GHz.  $50 \Omega$  quarter-wavelength microstrip lines at the collector nodes of Q3 and Q4 are used as RF chock [7], which present an open circuit ( $> 500 \Omega$ ) to the low impedance collector nodes ( $\sim 10 \Omega$ ) and ease the implementation of matching network between Q3 and Q4 and output matching. The input and output ports of the power amplifier are matched to  $50 \Omega$  for the further

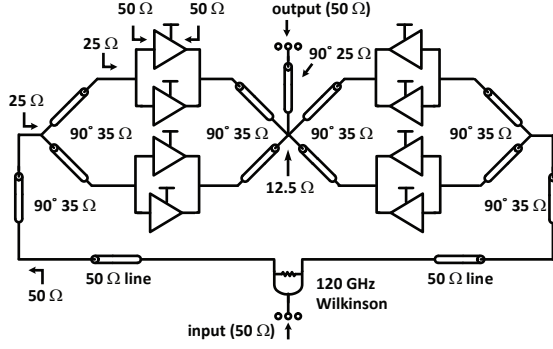


Fig. 3. Schematic of the 8-way power combining amplifier.

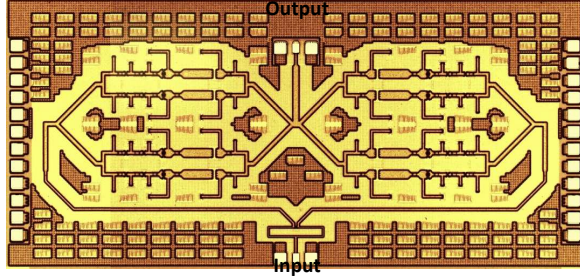


Fig. 4. Chip microphotograph of the 8-way power combining amplifier ( $3.3 \times 1.5 \text{ mm}^2$  including pads).

integration in the 8-way power combining PA.

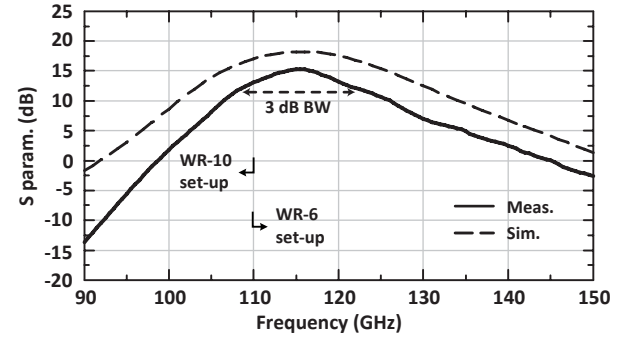
#### B. 8-way Power Combining PA

Fig. 3 presents the schematic of the 8-way power combining PA. The design consists of 8 single-ended PAs to form a two-dimension PA array. Two adjacent PAs in the array are tied together at input and output nodes to form a PA pair. The impedance looking into the output nodes of the PA pair are  $25 \Omega$  and are transferred to  $50 \Omega$  by  $35 \Omega$  quarter-wave microstrip lines at 120 GHz. The impedance at the common node is then  $50/4 = 12.5 \Omega$ , and the four PA pairs are then connected using a  $25 \Omega$  quarter-wave microstrip line to convert the  $12.5 \Omega$  to the  $50 \Omega$  output port. The input 120 GHz signal is distributed using a Wilkinson power divider and a T-junction with quarter-wavelength microstrip lines to present a  $50 \Omega$  impedance to each PA input port.

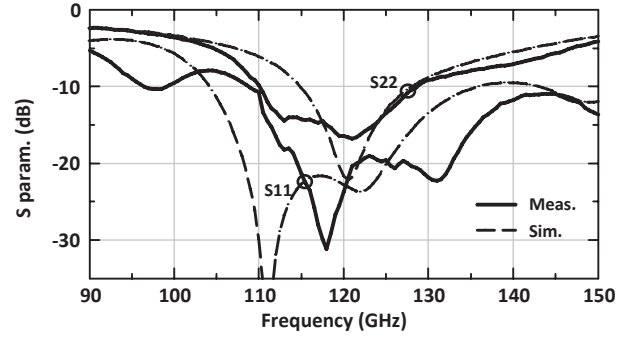
#### IV. MEASUREMENTS

The chip microphotograph of the 8-way power combining amplifier is shown in Fig. 4. The input and output GSG pads are designed to be compatible with both 100- and  $75\text{-}\mu\text{m}$ -pitch GSG probes.

S-parameter measurements are conducted using two different setups. VDI WR-10 extenders are used to measure S-parameter from 75-110 GHz, whereas OML WR-



(a)



(b)

Fig. 5. Measured (a)  $S_{21}$ , and (b)  $S_{11}$  and  $S_{22}$  of the 8-way power combining amplifier.

6 extenders are used for 110-160 GHz measurements. Calibration is done to the G-S-G probe tips using open-short-load standards on a CS-5 calibration substrate and measurements include the input and output G-S-G pads loss (1 dB loss total at 120 GHz). The measured peak small-signal gain for the single-ended PA breakout is 20 dB at 116 GHz with a 3-dB bandwidth of 110 to 122 GHz. The 8-way power combining amplifier has a peak small-signal gain of 15 dB at 116 GHz with a 3-dB bandwidth of 108-123 GHz (Fig. 5(a)). The 5 dB difference in the small-signal gain is due to the additional input distribution network ( $\sim 3$  dB) and the output combining network ( $\sim 1$  dB). The total quiescent power consumption in each case are 143.5 mW (89.7 mA), and 1.13 W (710 mA) from a 1.5-1.6 V supply, respectively.

Fig. 6 shows the large-signal measurement setup. All the measurements are referenced to the GSG probe tips, and include the 0.5 dB output pad loss. The measured  $P_{out}$  versus  $P_{in}$  at 116 GHz with a supply of 1.6 V is shown in Fig. 7 for the 8-way power combining amplifier. The measured  $P_{sat}$  for single-ended PA is  $>10$  dBm from 114 to 134 GHz with a peak value of 13.8 dBm at 126 GHz (not shown), and is  $>17$  dBm for the 8-way combining PA from 112 to 130 GHz. In particular, the 8-

TABLE I  
PERFORMANCE SUMMARY FOR AMPLIFIERS ABOVE 100 GHz

Freq. (GHz)	Tech.	Type	$P_{sat}$ (dBm)	Peak Gain (dB)	$OP_{1dB}$ (dBm)	Peak P.A.E. (%)	$P_{dc}$ (W)	Ref.
114-134	90-nm SiGe	4-stage Single-Ended	13.8	20	11	11.6	0.2 <sup>a</sup>	This work
112-130	90-nm SiGe	4-stage 8-way Comb.	20.8	15	17	7.6	1.52 <sup>a</sup>	This work
160	130-nm SiGe	3-stage Differential	11.5	32	8.5	-	-	[1]
130	130-nm SiGe	3-stage Single and Diff. <sup>b</sup>	7.7	24.3	6	6.8	0.08	[2]
90-98	130-nm SiGe	Quasi-optical power comb. 4-stage	21-23	21.5 <sup>c</sup>	-	5.8	3.3	[8]
140	65-nm CMOS	4-stage Single-Ended	13.2	15	9.9	14.6	0.12	[3]
110-117	65-nm CMOS	3-stage Differential	13.8	15	10.1	10	0.19	[4]

<sup>a</sup>At  $P_{sat}$ .

<sup>b</sup>1<sup>st</sup> stage is single-ended. 2<sup>nd</sup> and 3<sup>rd</sup> are differential.

<sup>c</sup> $P_{on-chip}$  used.

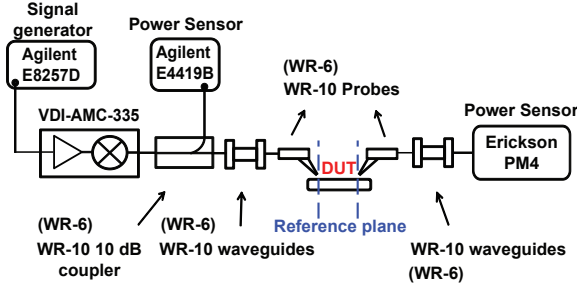


Fig. 6. Power measurement setup.

way power combining amplifier results in 20-20.8 dBm at 114-126 GHz, which is the highest power achieved for any silicon technology. The corresponding large-signal gain at  $P_{sat}$  is 10 dB with a peak PAE of 7.6 % at 114 GHz, and the PAE remains  $>6.3$  % from 114 to 126 GHz. The 8-way power combining amplifier delivers a  $P_{sat} >15$  dBm from 110 to 134 GHz.

## V. CONCLUSION

This paper shows that a reactively-combined 8-way power amplifier with  $\lambda/4$  impedance networks results in low loss power combining at 110-134 GHz, and state-of-art output power over a wide frequency bandwidth.

## ACKNOWLEDGEMENT

This work is supported by the DARPA THz Program under a subcontract from Teledyne Scientific.

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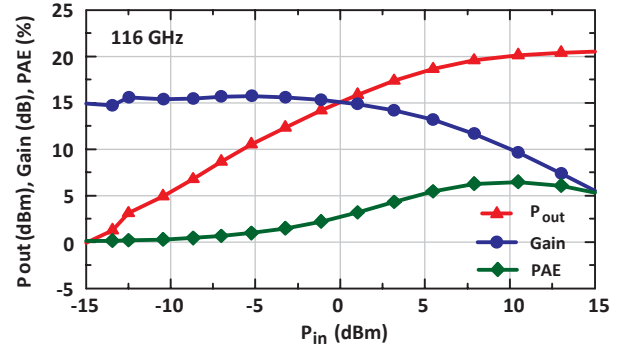


Fig. 7. Measured output power, gain, and P.A.E. vs input power of the 8-way power combining amplifier at 116 GHz.

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