Total Ionizing Dose (TID) Tests on Non-Volatile Memories: Flash and MRAM

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***Abstract* – We report on TID tests of Magnetoresistive Random Access Memory (MRAM), and advanced 4Gbit flash memories from three manufacturers. Both in-situ and biased interval irradiations were used to characterize the response of the total accumulated dose failures.**

***Index Terms*—Flash, MRAM, In-situ, TID**

I. Introduction

Non-volatile memories are widely used in many commercial as well as space applications. NAND flash memories are attractive choices for the massive data recorder requirements for space missions. Previous solid-state recorders were designed around reliable, robust and radiation tolerant dynamic random access memories (DRAM) but current recorders for space missions are being built with commercial-off-the-shelf flash memory. One old memory technology, Magnetoresistive Random Access Memory or MRAM, date back to the 1940's at Harvard by physicists An Wang and Way-Dong Woo, at MIT by Jay Forrester [1], recently gains recognition by its faster write speeds and unlimited endurance.

Memory cells in the flash NAND structure require reading and writing through other cells in the stack (the current 4Gbit part has 32 cells in the stack plus 2 select cells), this architecture results in inherently slower cell access time as shown in Fig. 1. The basic storage element consists of a control gate stacked over an isolated polysilicon gate in the gate oxide, known as a floating gate, a source, and a drain. Data can be interpreted as "0" when charges (electrons) are placed in the floating gate. When electrons are removed from the floating gate, data become "1". The configuration is known as single level or one-bit-per-cell storage since the read-out data can be identified either as "1" or "0". NAND flash memories have a limited number of read and write cycles before which reliability issues occur.

MRAM combines magnetic memory with CMOS technology to achieve unlimited read/write endurance with high-speed operation. MRAM data are stored as magnetic states, rather than charge as in flash technology, so MRAM technology eliminates the problems of wear-out and charge leakage. The basic MRAM element uses a magnetic tunnel junction (MTJ) device for data storage. Each MJT is composed of two magnetic layers separated by a very thin insulating layer. One magnetic is fixed and the other one is free to move. Each magnetic layer has a polarity, a north

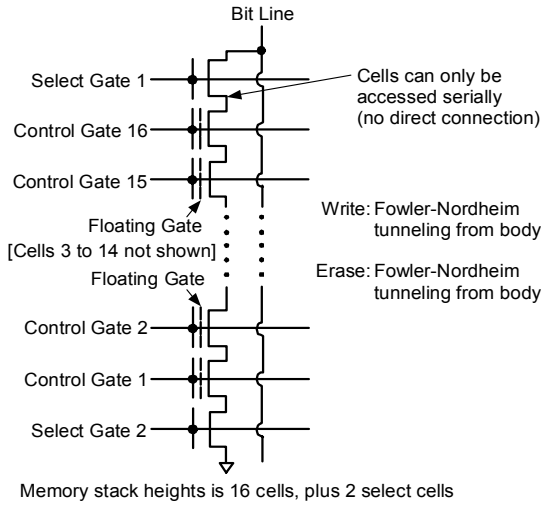

Fig. 1: NAND cell structure, only 16 cells in the memory stack are shown.

pole and a south pole. Both layers can be orientated in parallel direction where their magnetic moments are in the same directions and the MJT device has a low resistance.

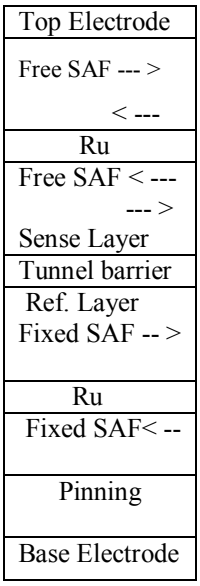

Fig. 2: Magnetic Tunnel Junction stack with Synthetic AntiFerromagnet (SAF) layers. Basic cell of Freescale MRAM.

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In the anti-parallel orientation, the magnetic moments are in the opposite directions and the resistance of the MJT device is high. The parallel configuration allows higher polarized current to flow through the MTJ, while the anti-parallel mode allows smaller polarized current to flow. The anti-parallel orientation represents the binary memory state of 1, and the parallel configuration interprets the binary state of 0.

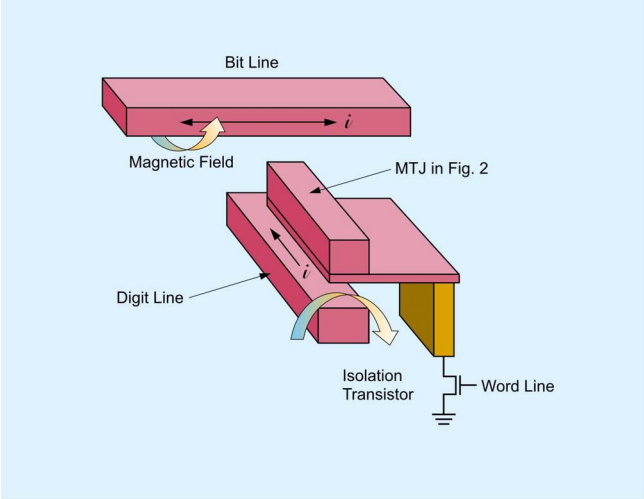

Fig. 3: Presentation of a 1-Transistor, 1MTJ cell showing the write currents, above and below MTJ.

II. Device Descriptions

The NAND-based Samsung, Hynix, and Micron 4Gigabit flash parts are organized as 2112 bytes x 64 pages by 4096 blocks. Programming and read data are transferred between the 2112-byte static register and the memory cell array in 2112-byte increments. During program and read mode, the page can be separated into three sections by the use of an internal pointer. The erase operation is implemented in block increments. The serial read cycle is 30ns and the access time of cell array to register is 25 microseconds. Samsung devices were built on a 90nm process technology.

The flash memory technology has internal charge pump generators to provide higher voltages than their external operating supplies for the programming and erase operations. The flash devices typically require 10 seconds to erase the whole part. Both Samsung and Hynix devices operate with lower currents in all modes up to 30mA. A total of nine devices were used for TID tests, three each from each manufacturer.

Freescale MR2A16A device is organized as 262,144 words of 16 bits. The memory is fabricated with 90nm CMOS process using five levels of metal, and is based on the 1-transistor, 1-magnetic tunnel junction (1T1MTJ) memory cell. Fig. 2 shows the actual MTJ used in the construction of Freescale MRAM memory cell. Each Freescale magnetic layer, also known as synthetic antiferromagnet (SAF), is formed with a non-magnetic coupling spacer layer of Ru sandwiched between two ferromagnetic layers. The exchange between the magnetic layers in the SAF fixes the polarization of the reference or Fixed SAF layer in one direction and keeps the reference layer from switching during write operations. The magnetic polarization of the sense or Free SAF is free to rotate during write. The high current pulses are applied to both write lines as shown in Fig 3. A top sense electrode is not shown for clarity. Bit lines pass above the MTJ. Digit lines are below the MTJ. Digit line is used to provide a field for the free SAF to switch easily and the orientation of the free SAF is controlled by the current direction of the bit line. Write pulses on the two lines are selected to produce the generated fields sufficient to switch the selected cell. All other cells only see a half-selected current write pulse that is not sufficient to change the state. During read operations, the digit line is turned off, the transistor of the selected bit is turned on to bias the MTJ, and the read current is measured and compared to a reference to determine if the resistance is low or high. Based on the unique behavior of a synthetic antiferromagnetic (SAF), the MR2A16A can be programmed effectively without the single-line disturb problem present in early approach to MRAM switching from one state to the other due to Freescale's Toggle mode. In Toggle mode, the same exact pulse sequence is used each time to switch the current magnetic state to the opposite one.

III. Test Set-up

Total dose tests were done at 25° C using the JPL cobalt-60 facility at a dose rate of 25 rad(Si)/s. The flash memories were static-biased during irradiation. Random numbers are programmed into the DUTs to simulate real world data.

Static biased read-only mode tests consisted of the following sequences:

1. Erase, write, and read to validate random numbers
2. Irradiate with DUTs in static-biased boards.
3. Read random numbers to ensure data retention
4. Repeat 1 to 3

The Freescale MRAMs were programmed with random numbers and tested dynamically in-situ with the following three modes:

1 read-only loops

2 read-program-read loops

3 a combination of mode 1 and 2 above

Three MRAMs, serial numbers FS003-FS005, were programmed with random numbers and read during

irradiation in mode *1*. One MRAM, serial number FS001, was tested with mode *2*. Finally, serial number FS002 used mode *3* during irradiation.

The Avnet FPGA board with Xilinx Virtex 2PRO was used to test the Samsung, Micron and Hynix 4Gbit flash memories. The DUTs were erased/verified/programmed and read (EVPR) prior to static-biased irradiation. Pseudo random number pattern was used for simulating real world data.

The Trenz FPGA board with Spartan IIE was used to test the Freescale MRAM devices. The FPGA board and the test board was placed inside the Cobalt chamber. The Trenz board was heavily shielded to prevent upsets from gamma rays. The test pattern was random number pattern. Fig. 4 shows a typical in-situ setup at the JPL Cobalt-60 source.

Fig. 4: TID in-situ test setup at the JPL Cobalt-60 facility

IV. Radiation Induced Failures

MRAM MTJ cells are radiation hardened due to its intrinsic composition. The stored data do not depend on floating charge as it is the case on flash memory elements. Unlike flash technology, MRAMs do not store charge to define the 1 and 0 states. MRAM devices operate at 3.3 volts for all read, and write functions. Therefore, there is no internal charge pump circuitry needed as flash memories. The radiation sensitive areas affecting the MRAM functions are the CMOS sense and program circuitry. Each MTJ memory cell has one transistor, two differential current conveyors, one two-stage comparator, and one regenerator to determine the resistance state during the read operation. The transistor is off during the write operation. The transistors are buried closer to silicon substrate since the MRAM module is the last component to be inserted into the front-end CMOS circuitry.

Flash memories are sensitive to radiation. The overall operation of NAND flash memories requires many clock cycles and commands just like the operation of most microprocessors because of the complex architectures, such as internal state machine, write buffer, multiplexers and registers. Soft errors can be caused by single event transients (SET) in the readout buffer. Failure to erase can be defined as an unsuccessful removal of electrons from floating gates after a number of passes, or a failure of device's ready signal to inform the status register after a specified elapsed time. Single event upsets occur in the state machine and registers. The upsets are very difficult to categorize and interpret because of the many interconnected sub-elements inside the functional block. These upsets will mostly interrupt the intended operation and lock it into an undefined function mode. New generations of shrinking cell area in flash memory complicated the distinction between single event upsets and single-event-functional-interrupt (SEFI)[2],[3]. One recent study had shown the internal charge pump circuitry damaged by exposing to heavy ions [4]. Other study also revealed that heavy ions had stopped the flash memory devices from erasing and programming the blocks and cells, respectively [5].

V. TID Test Results

Three devices were subjected to read-only sequences. They were initially programmed with random numbers before being exposed to radiation. These parts were dynamically read during exposure. The other two went through the read-program-read sequences while irradiated. All five tested parts showed no failure at 40 krad(Si) and below. Device FS001 started having 2 read errors at 45 krad(Si) when irradiated with mode *2*, and had more than 130 read errors at the accumulated dose of 55 krad(Si). Two devices, FS003 and FS004, had no failure at 60 krad(Si) and below with mode *1*. Serial number FS002, showed only 11 read errors at 50 krad(Si). Fig. 5 illustrates the TID results of all five devices. In a typical multi-year space mission, the read sequence is often used more than the programming sequence, unless the application requires constant update of recording data. The TID results of the read-only sequence show that most MRAM devices will survive the total accumulated dose up to 60 krad(Si).

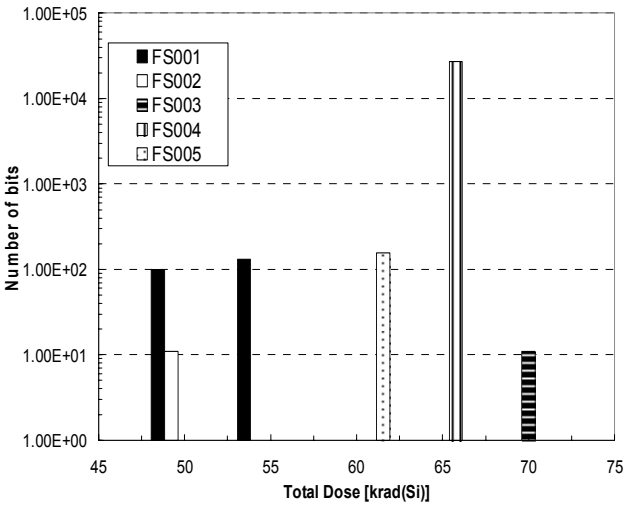

Fig. 5: TID results for the MRAM (Bit read errors versus total dose)

As we mentioned in sections II and IV, the front-end CMOS circuitry is the main area sensitive to radiation effects. The CMOS transistors are buried under five layers of metal and two layers of poly. All five parts were allowed to anneal at 25°C for 24 hours, then they were electrically tested. After 120 hours and 720 hours of annealing respectively, they were tested and the results are shown in Table I. Three devices, FS002-003 and FS005, can be read-programmed-read after 120 hours at 25°C.

TABLE I
The number of failed bits after hours of anneal

s/n	*24 hrs*	*120 hrs*	*720hrs*
FS001	103	635	0
FS002	8	0	N/A
FS003	32	0	N/A
FS004	34656	42489	0
FS005	306	0	N/A

The flash memory devices of the following three manufacturers Hynix, Samsung, and Micron were tested. All shared the same operation codes for most basic operations, such as, block erase, page read, and write. They were statically biased during irradiation and went through the sequence of read/erase/verify/program/read. The same sequence of read/erase/verify/program/read applied to many earlier studies of TID on flash memory devices. The first generation of NAND flash memories failed to erase at the very low dose rate of 10krad(Si) [4].

The Hynix flash devices had no failure of any block of memory cells at 25 krad(Si) and below. The Hynix part, s/n 1953, failed to write to all 4028 blocks at 35-40 krad(Si). The second Hynix, s/n 8, had more than 3000 un-programmed blocks after 35 krad(Si). There were 240 failed-erased blocks and 4096 failed-programmed blocks after 45 krad(Si) with Hynix part s/n 1498. After 24 hours at 25°C annealing, five out of 4,096 blocks could be erased. We also tested three Samsung parts. The Samsung 4Gbit parts started having less than 10 blocks that could not be programmed after 25 krad(Si). The Samsung DUTs showed no major failure at 45 krad(Si) and below. They lost the ability to erase at 60 krad(Si). After 20 hours at room temperature, all three parts recovered and function normally with the erase/write/read capabilities. Micron parts performed well compared to the other two manufacturers. The Micron devices had only few bad blocks and still functioned even after 100 krad(Si). Table II summarizes the TID levels of the flash memory parts.

TABLE II
TID levels and anneal

Device	*TID levels*	*20hrs anneal (25°C)*
Micron 4Gb	90Krad(Si)	Yes
Samsung 4Gb	45Krad(Si)	Yes
Hynix 4Gb	25Krad(Si)	No

VI. CONCLUSIONS

MRAM devices withstand the effect of TID up to 60 krad(Si) with only a few read errors. The dynamic in-situ configuration provides the worst-case condition. MRAM tested under dynamic sequence starts having read errors at 50 krad(Si). After 120 hours annealing at 25°C, three out five parts recovered and functioned normally. After 30 days, two more recovered and could be reprogrammed with new data.

As mentioned in section I, the write operation requires applying high current pulses to the two lines that pass above and below the selected cell. The high current pulses can impact on the reliability of the MRAM. One of the issues is the electro-migration. A strong external magnetic field poses a possibility of bits switching states. Depending on its intensity, the magnetic field can damage both layers of cells and the 1 or 0 state can be stuck indefinitely. The density of MRAM components lags behind flash memory devices. One approach is developing a pair of multiplayer storage cells to create a multi-bit memory cell [6].

TID tolerance of Micron NAND flash memory has improved. Only a few blocks cannot be programmed at 100 krad(Si). Previous generations of flash devices showed functional failures after 10-15krad(Si) [4],[7]. The worst case is static biasing during irradiation. As the cells are scaled down further, heavy ions reduce the charge retention capability of the floating gate. Heavy ions, at LET as low as 32 MeV-cm^2/mg, also can damage the charge pump circuitry to stop devices from erase.

The NAND flash memory eventually will move beyond the 30nm technology by the next decade, 2010's, and the density of NAND device will reach to 32-64Gb or above, based on the current scaling trend of flash technology [8].

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology

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