SYSTEM INTEGRATION OF A COAXIAL FERRIMAGNETIC NONLINEAR TRANSMISSION LINE ARRAY

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Abstract

This paper describes the system integration of a four element, nonlinear transmission (NLTL) array. The HPM system components include a negative polarity 40 kV capacitor charging supply, a trigatron spark gap, a solid-state trigger generator, four delay lines with biasing coils, four coaxial ferrimagnetic NLTLs with biasing coils, eight dc current supplies, and four TEM horn antennas. A National Instruments cRIO FPGA based controller is used to interface the capacitor charging supply, the biasing coil power supplies and the trigger generator to a laptop based GUI. In order to minimize impact from EMI, all lines were properly shielded and the data acquisition equipment was located a sufficient distance away from the NLTL array. The GUI consists of options for controlling the current output on all 8 power supplies for biasing purposes, as well as pulse options that include repetitive pulsing based on the number of pulses or for a specific length of time. Pulse duration for the capacitor charger, the command charge, and the trigger can also be adjusted. An emergency stop button is included for safe shutdown of the trigger generator and all power supplies. A diagnostics setup is outlined describing the placement of inline coaxial D-Dot probes and a high voltage probe for laboratory testing.

I. INTRODUCTION

This paper outlines a diagnostic setup as well as a control system setup for a Non-Linear Transmission Line (NLTL) array. The NLTL system itself consists of an array of four 12" delay lines, four NLTL lines, and four TEM Horn antennas. A trigatron spark gap is used as a switch for the system with a trigger generator providing the initial trigger to collapse the gap. The diagnostic system setup describes the equipment used to collect data at different parts of the NLTL system. This includes inline and radiated field intensities as well as capacitor charging on the spark gap. The control system setup describes the equipment used to remotely operate the NLTL system using a Hight Voltage (HV) power supply, 8 biasing power supplies, and a National Instruments (NI) cRIO controller.

Figure 1 shows the block diagram of the layout of the system. The HV power supply charges the capacitor bank on the spark gap and the Pulse Generator is used to trigger it. The pulses are then fed into the dynamic delay lines in order to phase the pulses across the array and provide maximum power at the output. The pulses then travel into the main NLTL lines producing microwaves at approximately 3.5 GHz. The TEM Horn antennas are then used for microwave emission. The biasing power supplies are used to bias both the dynamic delay lines as well as the NLTL lines.

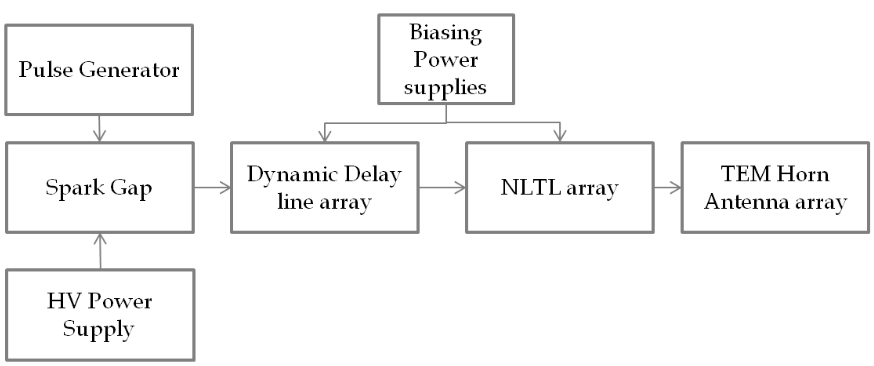

Figure 1. NLTL System Block Diagram

II. DIAGNOSTIC SETUP

There are two main sources for collecting diagnostic data from the NLTL. One is found on the couplers between the main NLTL lines and the TEM horn antennas. These couplers contains a D-DOT probe for field measurements within the NLTL. This coupler fits between each piece of the system and can be changed to measure field strengths at different locations in the system. The other source is a Prodyne D-DOT probe that is placed 3m away from the antennas for radiated measurements. It has a $3x10^{-4}$ m^2 equivalent area and a frequency response of up to 5.5GHz and a rise time of .064 ns, which are both adequate for measuring the 3.5 GHz microwave emissions produced by the system [1]. A high voltage probe is also used to measure the voltage on the capacitor bank of the spark gap to watch for pre-breaks or no breaks on the spark gap.

Three oscilloscopes are used for measurements. A 12 GHz, 40 GSa/s oscilloscope is used to collect data from the radiated D-DOT probe to determine if the lines were correctly phased. A 50 GHz, 160 GSa/s oscilloscope is used to measure electric field strengths on individual lines. A 600 MHz, 4 GSa/s oscilloscope is used to check for pre-breaks or no breaks on the spark gap from the high voltage probe.

III. SYSTEM EQUIPMENT

The main equipment used to control the system consists of 8 biasing power supplies, a HV power supply and a NI cRIO controller.

The cRIO is used to control the entire system. It consists of a 9004 controller which is used to receive input data, and a chassis which contains a 40MHz FPGA used for signal generation and communication. There are three different C-modules that are used for communication and signal generation. A 9474 C-module is a sourcing digital output module which is configured as a sinking output to correctly inhibit the HV power supply. A 9401 C-module is a bidirectional digital module which is used for signal generation for the pulse generator and can operate at frequencies of up to 10 MHz. Lastly, a 9871 C-module is used to provide RS-485 serial communication between the FPGA and the biasing power supplies.

For the biasing power supplies, the Sorenson XG 40-38 power supplies provide adequate power (1500 W) as well as remote operation with a daisy chain feature. This lets as many as 30 power supplies be interconnected with jumper cables, but only one is connected to the controller through RS-485 serial communication. This means data can be relayed through only one connection but will be passed to the correct power supply. Remote operation includes voltage and current settings, power enabling and disabling, as well as error checking.

To charge the capacitor bank on the spark gap, a TDK Lambda 802L is used. It is used to charge the capacitors up to -40 kV and can output up to 8000 W of power. It is able to charge capacitor bank in under 1 ms which is necessary for a 1 kHz operation frequency. It also has a remote inhibiting option which is used for remote operation.

IV. CONTROL SYSTEM SETUP

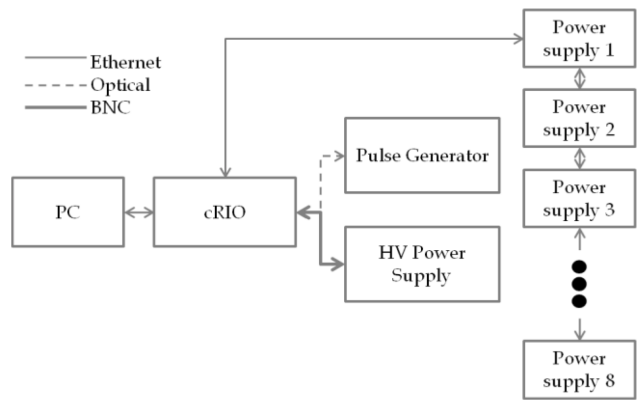

Figure 2- Control System Block Diagram

Figure 2 shows the block diagram for the control system. The graphical user interface (GUI) is accessed on a laptop and is used to control the overall system. The information on the GUI is then passed on to the cRIO which consists of two parts: a controller portion which is used to collect, configure and pass setup data, and an Field Programmable Gate Array (FPGA) portion which is used for signal generation and communication. The cRIO controls communication between the biasing power supplies through the 9871 C-module, the inhibiting signal on the HV power supply through the 9474 C-module, and signal generation on the pulse generator through the 9401 C-module.

The GUI on the front panel is shown in figure 3. It contains a main operation tab used for control of the system as well as an options tab for other configuration. On label A, the input controls are used for current outputs on each individual biasing power supply. A magnetic field strength is inputted, which is converted to a current through software which then biases the lines to provide that field strength. A button next to each control is used to disable or enable individual power supplies.

Label B contains the setting for the repetition rate of the system. The repetition frequency can be specified in Hertz and the number of shots can be set either by shot count or a dwell time in milliseconds. Label C contains the button that is used to clear alarms that appear on the biasing power supplies. These alarms include voltage and current overprotection as well as device hardware failures. Each numeric input control on the GUI has the ability to turn red in case one of these errors is detected on a power supply.

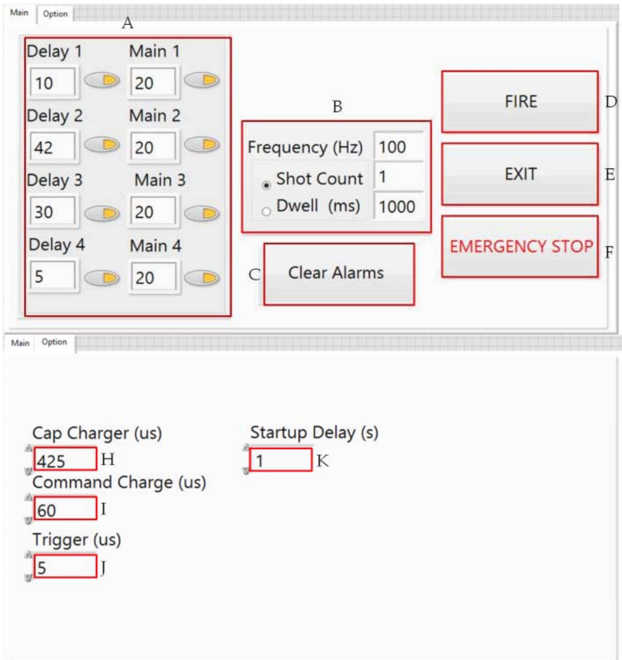

Figure 3- System Graphical User Interface

Label D,E, and F consist of 3 buttons. Label D is used to output signals to enable the power on the supplies, send pulses to the pulse generator at the desired frequency at number of shots, and send the inhibit signal to the HV power supply. Label E is used to exit the GUI after system operation is finished. Label F is used to safely abort operation of the system. It will send disable commands to each biasing power supply and HV power supplies and will interrupt signal generation to the pulse generator.

The options tab has configuration times for the pulse generator as well as the inhibit signal to the HV power supply. The cap charger (label H) control is used to determine how long to charge the capacitors using the HV power supply to reach the desired voltage of -40 kV. The command charge control (label I) is used to specify the time to charge the onboard capacitors that are found on the pulse generator. The trigger control (label J) specifies how long the trigger signal should be in order to trigger the pulse generator. All these indicators are specified in microseconds. The startup delay (label K) is used to provide a delay between the time the biasing power supplies are enabled and the time the pulse generator is triggered. This lets current and voltage values settle on the power supplies which makes the system stable before it is pulsed.

V. SOFTWARE ARCHITECTURE

All programming for the control system is done using National Instruments' LabVIEW software. This allows for one continuous programming paradigm between each different pieces of hardware. There are two main virtual instruments (VI) that are used to control the FPGA and the controller respectively.

The controller VI uses a variation of a producer consumer loop architecture to both take user input and control the system. the VI consists of 2 main loops, one to take user input and fire the system and the other to for command configuration for the biasing power supplies. A queue structure is used to pass data between each loop since it is a lossless transportation medium (assuming the queue stack is large and traffic is small). This means no data commands can be overwritten which can possibly damage the system.

The first loop takes in user inputs for the biasing power supplies and pulse generators. It sends the biasing power supply commands to the second loop through the queue structure and converts the pulse generator timing values to FPGA timing values which are then transferred to the FPGA. There are also error checking commands that are sent in order to check for error flags on the biasing power supplies.

The second loop is used to send the biasing power supply commands to the FPGA for serial communication to the power supplies. It uses an interrupt scheme to acknowledge each byte that is sent to the FPGA.

The FPGA VI uses a single cycle timed loop to generate instruction at every clock cycle. This means anything inside the loop will run at 40 MHz. This allows for accurate signal generation in the nanosecond range. The single cycle timed loop generates the signals for the pulse generator as well as the inhibit signal for the HV Power Supply. Another while loop is used for generating the serial data for the biasing power supplies and is configured for a 9600 baud rate.

VI. Summary

A diagnostic setup has been shown for radiated and inline field data collection on different parts of an NLTL System that is capable of producing microwaves at frequencies of approximately 3.5 GHz. A control system schema has also been implemented, with software and hardware functionality described in detail.

VII. REFERENCES

1. (n.d.). Retrieved June 15, 2015, from http://www.prodyntech.com/wp-content/uploads/2013/09/D-Dot-Free-Field-W2.pdf