

Solid State Linear Transformer Driver (LTD) Development for HPM Sources

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Abstract

The Marx pulse generator topology has been widely used in pulsed power applications^{1,2}. Another pulse generator topology, the linear transformer driver (LTD), has been developed³ that may serve as a viable alternative to the Marx generator. LTDs utilize inductively added stages to achieve high voltages and currents. Unlike a Marx generator, each stage in an LTD features multiple bricks, all of which are ground referenced and allow current to be distributed amongst an arbitrary number of switches. This allows for LTDs that utilize solid-state switches, potentially resulting in more compact and reliable pulse generators. A solid-state, >10 kA peak current, multiple-stage LTD is developed. The generator's performance will be analyzed for viability as a replacement for driving a high power microwave generator.

I. INTRODUCTION

The traditional Marx topology of pulse generators utilizes a number of stages charged in parallel and subsequently switched to discharge in series in order to obtain voltage multiplication. While this allows for high voltage output with low charging voltage, it requires robust, high-voltage, high-current switches that must handle the full load current. Traditionally, spark-gap switches are used as they fulfill these stringent requirements.

Another pulse generator topology, the linear transformer driver (LTD), has been developed and may serve as a viable alternative. Similar to a Marx generator, the LTD utilizes a number of stages charged in parallel. However, the LTD topology takes advantage of magnetic coupling to achieve voltage multiplication in the form of inductively added stages. This allows for each stage to be ground-referenced, which opens the door for lower voltage, solid-state switches to be used. In addition, each stage can be composed of multiple bricks switched in parallel, allowing current division between the switches in each stage. Thus, smaller, low-profile switches can be used to reduce overall system size and inductance. Figure 1 shows a schematic representation of a 3-stage LTD.

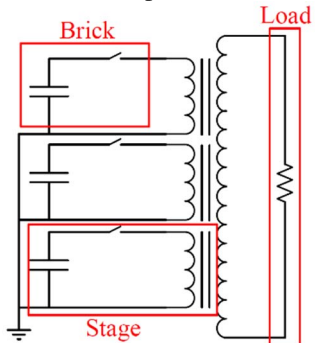


Figure 1. Schematic representation of a 3-stage LTD

II. BRICK DESIGN

A. Solid-State Switch

While the LTD topology reduces the stress encountered by individual switches, robust solid-state switches are chosen to ensure reliable operation over long time periods. For this application, the Silicon Power CCSSC14N40A10 n-type thyristor was chosen due to its high current-carrying capabilities as well as its high hold-off voltage. The thyristor can be used to hold off up to 4 kV and conduct up to 10 kA repeat current. This allows for use in high-current, rep-rated systems. In addition, this thyristor switch features a low-profile design, as shown in Figure 2, which allows for a reduction the physical height of each stage and the overall LTD.

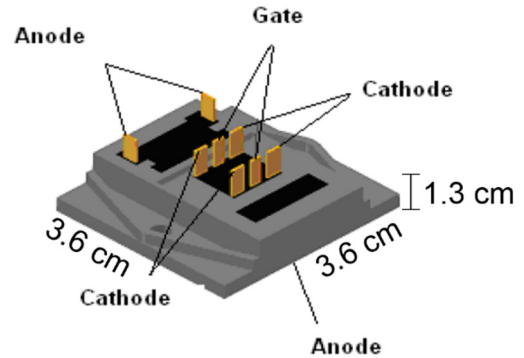


Figure 2. Silicon Power Thyristor CCSSC14N40A10 [6]

While this switch alone will allow for LTD stage charging voltages up to 4 kV, a series combination of two switches allows for increased charging voltage up to 8 kV. This increased charging voltage will improve the overall compactness of the design, as less stages will be needed to produce a high voltage output. This does, however, introduce increased complexity to the thyristor driving circuitry. In addition, the PCB and stage design must take into account the increased isolation necessary for the higher charging voltage in order to avoid breakdown.

B. Low-Inductance PCB

In order to ensure fast rise time for the output pulse, the inductance within the switching circuit must be minimized. In addition, sufficient clearance must be present between high differential voltages in order to prevent breakdown at charging voltages up to 8 kV.

The thyristor triggering circuit utilizes pulse transformers to drive the series thyristor pairs. The pulse transformers are driven in parallel to ensure that both thyristors are switched on equally. This avoids asynchronous switching which could cause an over-voltage condition on one of the thyristors. In

addition, 20 M Ω high-voltage resistors are connected in parallel with each switch to ensure equal voltage sharing.

The capacitor discharge path through the thyristors is critical to ensure fast pulse rise time. The inductance in this loop, and thus the area within the loop, must be kept as small as possible. As shown in Figure 3, the discharge path flows from the top of the board, through the thyristor pair, through the load, and returns on the bottom of the board.

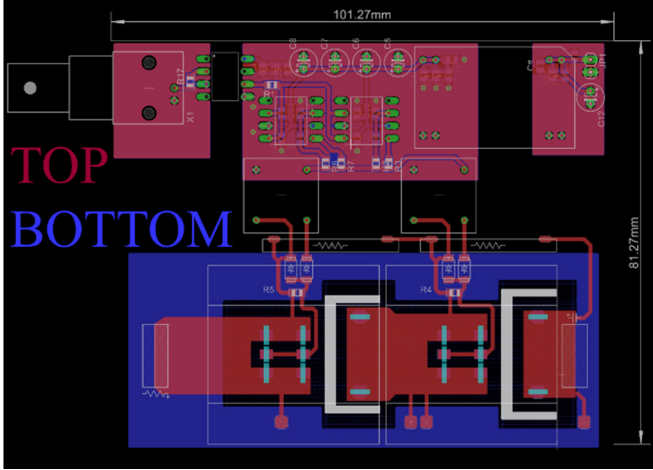


Figure 3. LTD brick PCB design with series thyristor switching. Red – Top of PCB, Blue – Bottom of PCB

Due to the through-hole packaging of the thyristors, slots were cut into the PCB to increase clearance between high voltage and ground. Some sample waveforms taken when discharging a 12.5 nF capacitor into a 1 Ω load are shown in Figure 4.

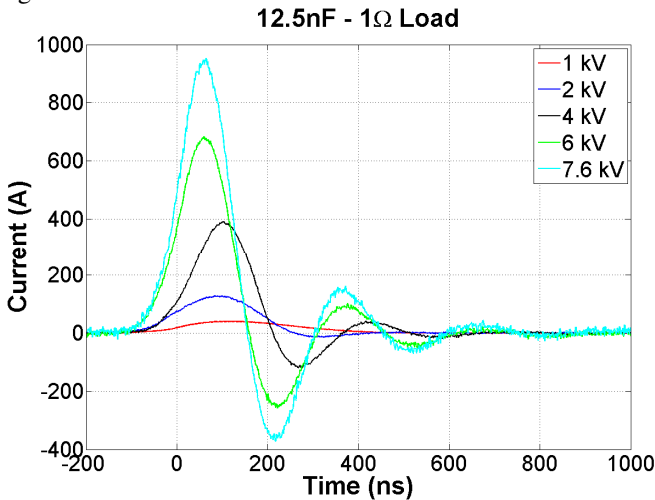


Figure 4. LTD single brick discharge waveform

III. STAGE DESIGN

The LTD stage consists of a number of bricks connected in parallel. Each brick consists of a 50 nF capacitor, with six bricks in each stage. Each stage consists of 300 nF total capacitance charged to 8 kV, or 9.6 J of energy per stage. As shown in Figure 1, this stage is then discharged into a single-turn primary winding around a central magnetic core. The

individual bricks are arranged radially around the toroidal core. In order to achieve increased output voltage, additional stages are stacked. The secondary winding, also a single-turn, is realized by a center conductor inserted in the middle of the toroidal core with return conductors on the outside of the core. Single-turn windings are used to maintain low inductance throughout the system.

A. Magnetic Core

Traditionally, Metglas magnetic cores are used for compact pulsed power applications due to its high saturation flux density of 1.5 T. However, a newer magnetic material, nanocrystalline, offers much lower core loss at the higher pulsed frequencies and has similarly high saturation flux density at around 1.23 T. Since it is new material, there is very little information available that characterizes the material. Using the method presented in [8], the BH curve for the nanocrystalline magnetic material was measured, as shown in Figure 5.

Nanocrystalline BH Curve

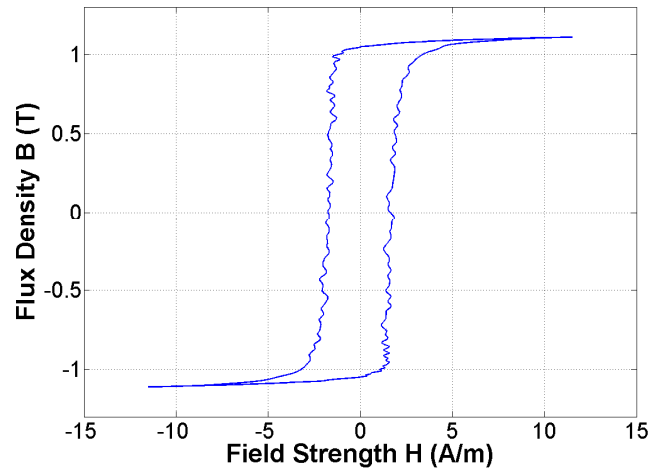


Figure 5. Nanocrystalline measured BH curve at 60 Hz

The magnetic core in each stage provides coupling between the individual LTD stage and the output conductor. It must be capable of sustaining the required volt-seconds of the driving pulse without being too large in order to decrease stage size. The relationship between magnetic flux and applied voltage is shown below. Φ represents the magnetic flux in the core, B the magnetic flux density in the core, A the cross-sectional area of the core, V the applied voltage, and N the number of turns.

$$\Phi = B * A \quad (1)$$

$$V = N * \frac{d\Phi}{dt} \quad (2)$$

Combining equations (1) and (2) yields (3) below, where δB represents the saturation flux swing of the magnetic material.

$$\int V dt = N * A * \delta B \quad (3)$$

As obtained by integrating the primary voltage waveform in simulation, the required volt-seconds of the driving pulse per stage was calculated as 1.3 mVs. In addition, the full magnetic flux swing of the nanocrystalline core from negative remnant flux density to saturation is found to be 2 T from the measured

BH curve. Using these values, the minimum required cross-sectional area of the magnetic core was found to be 6.6 cm^2 . In order to reduce core losses further, an increased cross-sectional area of 9.7 cm^2 was chosen. This additional area ensures that the core will provide sufficient flux swing. The height of the core was chosen to match the tallest component of the driving circuitry to keep the vertical dimension of each stage as small as possible. The final core size was selected with inner radius of 2.5 cm, outer radius of 8.9 cm, and a height of 1.6 cm from MK Magnetics.

B. Stage Geometry

A CAD model of a single LTD stage is shown in Figure 6. The LTD stage consists of a centralized toroidal magnetic core with six bricks placed radially around the core. Each capacitor is connected to the top portion of the primary winding. The bottom portion of the winding then connects to the bottom of the thyristor switching board to complete the discharge circuit.

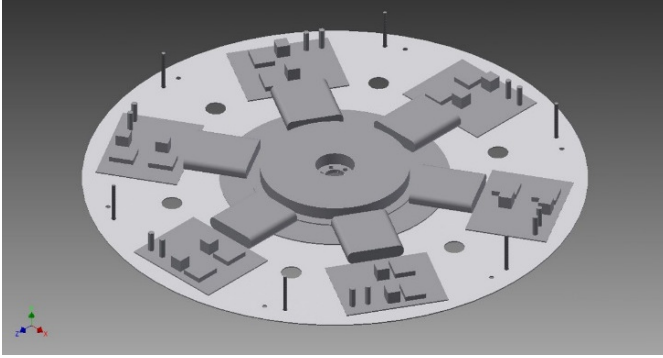


Figure 6. 3D CAD model – LTD stage

The secondary winding of the LTD consists of a center conductor that passes through the middle of the magnetic cores in each stage and return conductors that complete the loop around the outside of the magnetic cores. These return conductors are placed as close to the outside of the magnetic core as possible to maintain low inductance. A model of the primary and secondary winding geometry for a single stage was developed in COMSOL Multiphysics, as shown in Figure 7.

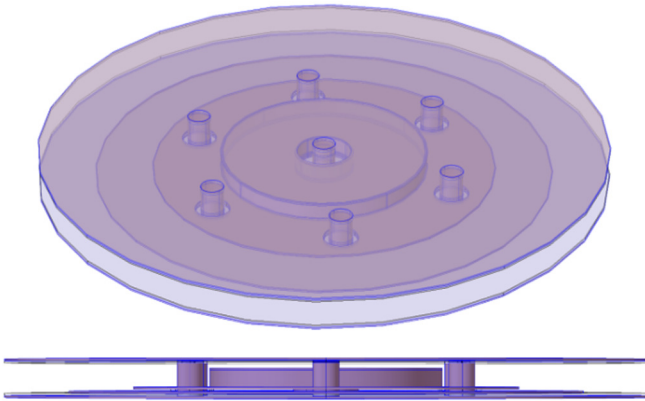


Figure 7. 3D COMSOL model – LTD stage w/ secondary

While the secondary winding of the LTD can be approximated with coaxial geometry, this results in inaccurate estimates for the inductance. Using COMSOL, a 3D model was developed to obtain more accurate estimates for the inductance of the secondary geometry. Utilizing the magnetic fields interface within COMSOL, the secondary winding was excited with a normalized current. The results were analyzed to find an approximation for the inductance per stage of the secondary winding. The current density within the secondary winding was plotted as shown in Figure 8 to ensure the simulated current was flowing in the correct loop.

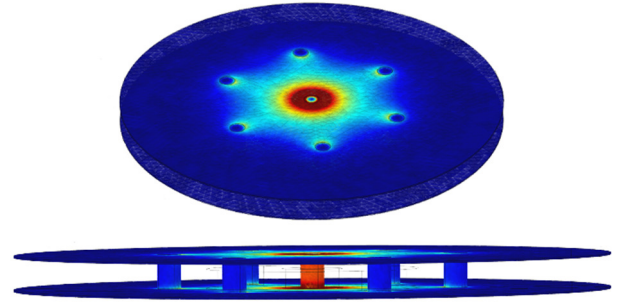


Figure 8. 3D COMSOL simulation – Secondary current density

With both stationary and frequency dependent studies in the vicinity of 5 MHz, the inductance of the secondary geometry was calculated to be $\sim 16 \text{ nH}$ per stage.

IV. COMMAND-CHARGING

For rep-rated operation of the LTD, a command-charging approach will be required to recharge the stage capacitance after each shot. While resistive charging, RC charging, offers simplicity, it is a very inefficient and slow charging method. H-bridge charging is an alternative charging method that offers quick and efficient charging with added complexity. A basic schematic representation of an H-bridge charger is shown in Figure 9.

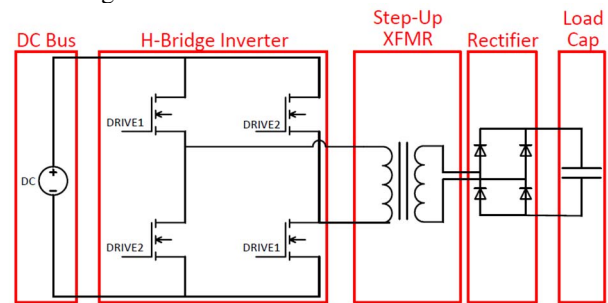


Figure 9. H-bridge capacitor charger schematic representation

A compact, wall-powered, h-bridge topology capacitor charger is under development at the time of this writing. The charger utilizes a 170 V DC bus inverted with a MOSFET h-bridge and stepped up to 8 kV with a transformer. This output is then rectified and will be used to charge the LTD capacitance. Using a dsPIC microcontroller with built in PWM modules, the duty cycle of the output waveform can be varied to adjust the current supplied to the load and improve efficiency.

V. FURTHER IMPROVEMENTS

In addition to command-charging, further improvements to the LTD design will be implemented. Active reset circuitry to quickly reset the core to the opposite tail of the BH curve after every pulse is required for rep-rated operation. After each pulse, the magnetic core will be very close to saturation. As shown in the Figure 5, due to the square anneal of the core, the remnant flux density remains close to this saturation point. The magnetic flux density can be reversed by applying a magnetic field in the opposite direction to the pulsed magnetic field. The core must be reset before any subsequent shots to prevent the core from saturating.

While the brick design has been optimized for low inductance, there remains room for improvement within the LTD stage geometry. Using COMSOL Multiphysics, the coupling between each stage and the secondary winding will be simulated and analyzed for viable improvements.

VI. CONCLUSIONS

The LTD design presented here shows an alternative approach to a high voltage, high current pulse generator. The LTD has many advantages over traditional Marx generator topologies, including low charging voltage and current division between switches. The use of solid-state switches allows for compact brick and stage design, which leads to a system with overall lower inductance and smaller physical dimensions.

In addition, the LTD design shows promise as a viable alternative to a Marx generator previously built¹ to power HPM sources. This system utilized spark gaps and higher charging voltage per stage. The output of this Marx system into a matched load yielded a pulse width of 200 ns and rise time of 50 ns. Initial LTD brick testing exhibits similar pulse shape characteristics using solid-state switches.

The proposed LTD will be expanded into a larger scale implementation with >10 stages in order to achieve higher

output voltage. This multi-stage LTD will be constructed and analyzed for viability in driving HPM sources.

VII. REFERENCES

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