

Layer Separation Optimization in CMOS Compatible Multilayer Optical Networks

Adam M. Jones [1,2], Christopher T. DeRose [1], Anthony L. Lentine [1], Douglas C. Trotter [1], Andrew Starbuck [1], and Robert A. Norwood [2]

[1] Sandia National Laboratories, contact: adaajone@sandia.gov [2] University of Arizona

Abstract: We explore the design space surrounding a CMOS compatible silicon nitride over silicon-on-insulator 3D optical layer for photonic interconnection networks and compare the results with single layer approaches.

The ever-rising rate of data generation and transfer continues to supply a strong demand for improved device density and efficiency in electrically and optically connected networks [1,2]. Silicon-on-insulator waveguides present an attractive option for significantly enhancing device density in photonic interconnection networks because the high index contrast enables a reduction in the size of many common optical components. Unfortunately, waveguide crossing performance degrades in high index contrast systems because the magnitude of the field scattered from the intersection scales with the index perturbation. Increasing device density and number of channels in a given network leads to a corresponding increase in the required number of waveguide crossings; this represents a significant design challenge as the scattered field causes path-dependent insertion loss and optical crosstalk.

Several approaches have been developed to mitigate loss and crosstalk in planar silicon waveguide crossings [3-7]. These established approaches typically result in a larger on-chip area and/or exhibit a narrow-band response thus limiting their applicability in wavelength division multiplexed networks. Multi-layer optical networks have been suggested as an alternative to planar approaches with the expectation that physically disjoint waveguide crossings will enjoy a decrease in excess loss and crosstalk [8]. We use silicon and silicon nitride as the guiding layers here because both materials exhibit low propagation loss across the optical telecommunication bands and are available in most modern CMOS fabrication lines thus enhancing the viability of the technology for commercial application.

In this paper, we describe detailed loss and crosstalk calculations (and measurements) for multilayer silicon nitride over silicon-on-insulator waveguide crossings. We show that crosstalk values exceed -60dB for interlayer thicknesses greater than 400 nm, although for thin layers, the excess loss can be excessive. However, we also show by example, that the multilayer approach yields performance (loss, crosstalk) and size comparable to or better than existing methods using planar crossings.

Loss and crosstalk are calculated for TE and TM polarizations using the commercially available software FDTD Solutions by Lumerical [9] over a range of vertical gaps (figure 1) and provide experimentally measured crosstalk values for a few cases. We then calculate the excess loss of vertical transitions of various lengths and vertical gaps (figure 2). Excess loss values for 1, 10, and 20 waveguide crossings are plotted along with the vertical transition loss data to help visualize the regimes in which each component dominates the total loss.

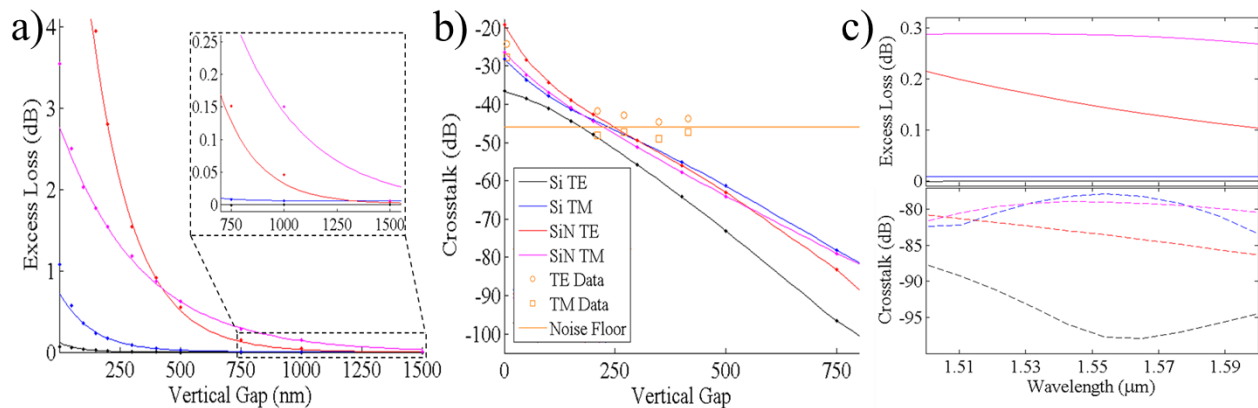


Figure 1 Simulated excess loss (a) and crosstalk (b) vs. gap for silicon and silicon nitride input ports and wavelength dependence of the excess loss and crosstalk for a 750 nm gap (c). Data provided is the geometric mean of the crosstalk for both ports. The legend denotes input port and polarization and applies to all figures.

While the performance crosstalk and loss values for the silicon waveguide inputs behave as expected, the excess loss of the silicon nitride input is significant, requiring gaps exceeding 1 μm to reduce the excess loss below 0.2 dB per crossing. This, in turn, places a constraint on the transition length required to achieve a desired path loss.

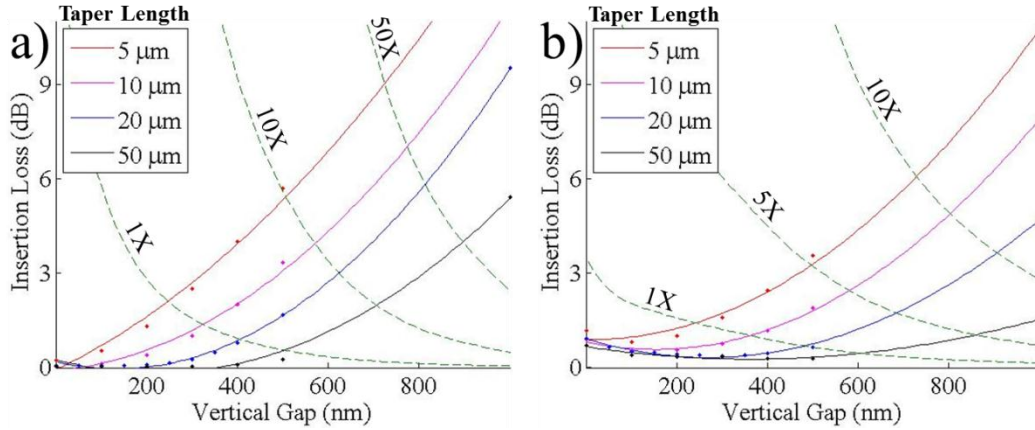


Figure 2 Comparison of vertical transition (solid lines) and crossing loss (dashed green lines, number of crossings traversed in bold) for TE (a) and TM (b) modes. All crossing loss measurements are for the silicon nitride input.

In designing multi-layer optical networks, one faces a tradeoff between crossing performance and transition loss, which scale directly and inversely with gap, respectively. Transition loss decreases with increased length, but this increases the on-chip area [10]. The optimal design heavily depends on the use case and must be determined for each application. As a simple example, we analyze the system in figure 3a with a single input and a range of crossing waveguides. We compare the performance of vertical crossings to a reference planar crossing assumed to have 0.2 dB loss and -40 dB crosstalk with a 10 μm waveguide separation (figure 3b). Loss for the silicon input and crosstalk for both cases are superior in the vertical crossing and are omitted as optimization variables.

From figure 3b we see the loss per vertical crossing must be lower than its planar counterpart to be a viable option; this sets a lower limit on the vertical gap. The upper limit is set by the on-chip area as the transition length becomes prohibitively long for reasonable loss values. Between these limits, one can use this approach to intelligently choose the optimal crossing geometry at each intersection within a given system.

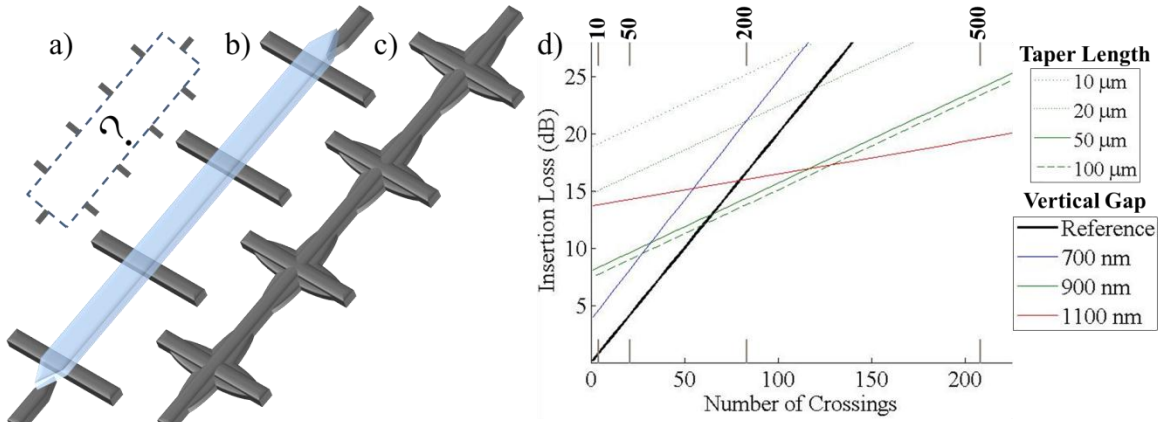


Figure 3 Schematic of a waveguide with four crossings (a), example vertical (b) and planar (c) crossings, and performance comparison of these structures (d). The short bars at the bottom/top of (d) indicate where the on-chip area of the planar structure exceeds the multi-layer structure area. The numbers next to each bar indicate taper lengths in micrometers.

- [1] D.A.B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," Proc. IEEE 97, 1166-1185 (2009).
- [2] M. Lipson, "Guiding, Modulating, and Emitting Light on Silicon – Challenges and Opportunities," J. Lightwave Technol. 23, 12 (2005).
- [3] P.J. Bock, *et. al*, Opt. Exp. 18, 15 (2010).
- [4] S.G. Johnson, C. Manolatu, S. Fan, P.R. Villeneuve, J.D. Joannopoulos, and H.A. Haus, Opt. Lett. 23, 23 (1998).
- [5] Y. Sakamaki, T. Saida, M. Tamura, T. Hashimoto, and H. Takahashi, IEEE Photon. Technol. Lett. 18, 19 (2006).
- [6] H. Liu, H. Tam, P.K.A. Wai, and E. Pun, Opt. Comm. 241, pp. 99-104 (2004).
- [7] W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, Opt. Lett. 32, 19 (2007).
- [8] A. Biberman, G. Hendry, J. Chan, H. Wang, K. Bergman, OFC, OMM2 (2011).
- [9] <http://www.lumerical.com/tcad-products/fdtd/>.
- [10] R. Sun, M. Beals, A. Pomerene, J. Cheng, C. Hong, L. Kimerling, J. Michel, Opt. Exp. 16, 16 (2008).

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.