High Speed, Direct Detection 1k Frame-Store CCD Sensor for Synchrotron Radiation

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***Abstract*–This work presents the development of a high speed, direct detection, 1k Frame Store CCD camera for synchrotron radiation. We review the research and development of this detector from small scale prototypes to a megapixel sensor, highlighting design challenges and solutions, and reporting on the achieved imaging performance. Further, we report on performance improvements obtained by implementing a second-generation fast readout integrated circuit manufactured in 0.25µm CMOS technology, as well as a voltage buffer chip manufactured in high voltage 0.35µm CMOS technology. The camera presented in this paper is high vacuum-compatible to allow for soft X-ray detection.**

INTRODUCTION

Many experiments at soft X-ray synchrotron facilities such as the Advanced Light Source (ALS) at Lawrence Berkeley National Laboratory (LBNL) are performed with X-rays that range from a few hundred electron volts (eV) to around 8keV in energy. Direct X-ray detection using silicon detectors is very efficient in this energy range. The limiting efficiency factor for low X-ray energies is the thickness of the entrance window. The thinner the entrance window is the higher the detection efficiency will be. On the high end of this energy range the limiting factor is the detector thickness. The thicker the detector is the higher the efficiency will be. Figure 1 shows the detection efficiency for a 300 µm thick CCD with a 10, 50 and 100 nm thick entrance window.

Recent X-ray detector developments in this area have focused on direct detection and high frame rate. Examples of such developments are the pn-CCD [1] and the compact fast CCD (cFCCD) at LBNL [2]. The latter is a 480 x 480 sensor matrix with 30µm square pixels read out at up to 200 frames per second (fps). In this paper we present the second generation of LBNL fast CCDs called 1K frame store CCD (1kFSCCD). This detector has a matrix of 1920 x 960, 30µm square pixels, read out in an almost column parallel configuration with 192 output ports running at a maximum 200 fps when operating in frame store mode. Besides the frame store mode this camera can operate in full frame mode reading 1920 x 1920 pixels at a reduced frame rate of 100 fps.

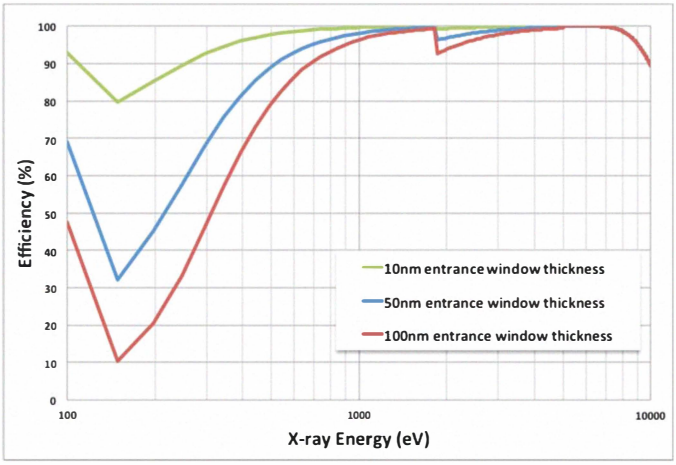

Figure 1 – Typical detector efficiency of a fully depleted 300µm thick silicon detector with 10nm, 50nm, and 100nm of inert silicon representing an entrance window.

The reminder of this paper is organized as follows: Section I describes the detector system, including the camera head, readout system, cooling system and power supply. Section II shows the initial results of this new camera system. Section III concludes the paper and presents suggestions for future work.

I. DETECTOR SYSTEM DESCRIPTION

The 1kFSCCD detector system includes (i) a camera head, (ii) a Camera Interface Node board (CIN), (iii) a readout system, (iv) a power supply and (v) a cooling system. Figure 2 shows the block diagram of the camera system and how each block interacts with each other to implement a complete system. These subsystems are detailed in the following subsections.

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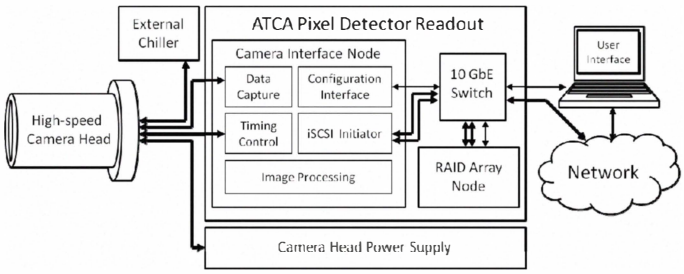

Figure 2 - 1kFSCCD camera block diagram.

A. The camera head

The camera head contains the detector, all the electronics needed to clock and bias it and a cooling system. Figure 3 shows the clock and bias board (green board on top), the CCD carrier (at the center) with the 1kFSCCD and two digitizer boards (at the bottom) that complete the camera head electronics. Figure 4 shows the camera head assembled to its cooling system and the camera vacuum chamber for standalone applications.

To reduce the thermally-generated leakage current in the CCD, the CCD carrier is cooled to -50ºC while the rest of the electronics is cooled to +20ºC by a cooling system with two closed loops. The camera head was produced to be compatible with high vacuum (better than 10^{-7} Torr) to avoid water condensation and freezing on the detector when operating at low temperatures. A second reason to have the camera head vacuum ready is to be compatible with installation in the same vacuum as the target sample and the X-ray beam, which is a requirement for soft X-rays applications.

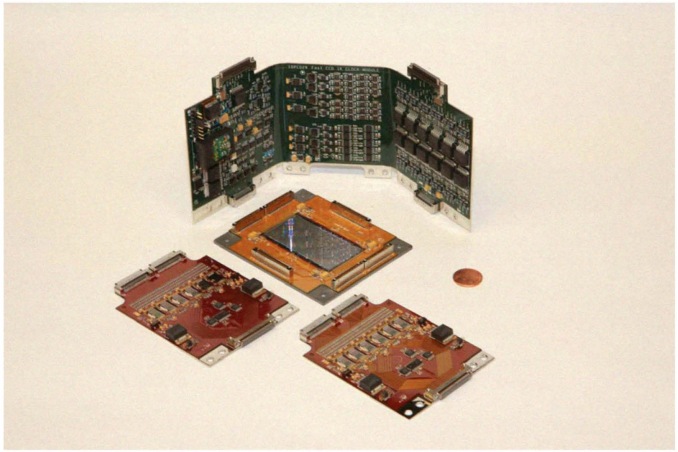

Figure 3 – Electronics boards used in the 1kFSCCD camera head. The clock and bias board (green board) is shown on top, the CCD carrier with the 1kFSCCD is in the center, while the two digitizer boards are at the bottom.

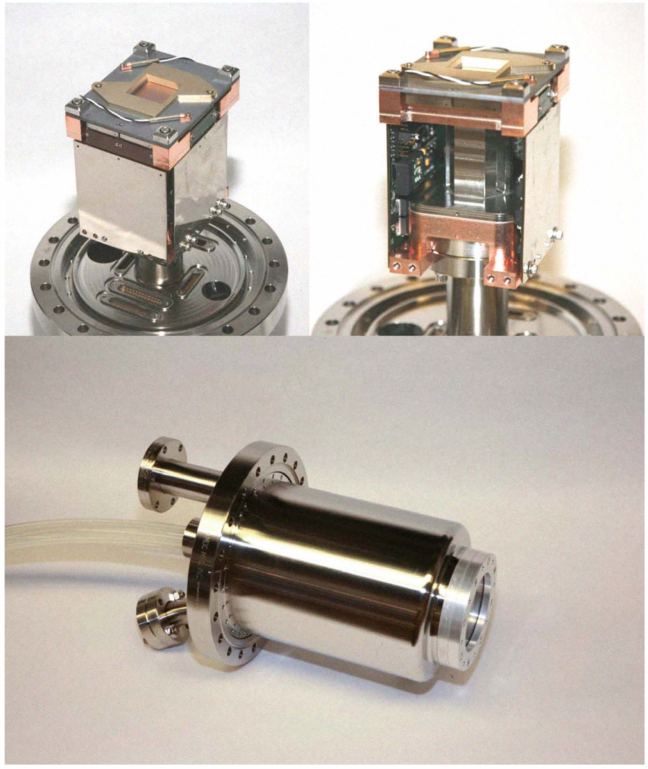

Figure 4 – (top left) 1KFSCCD camera head with its electronics boards exposed. On the top board one can see the frame block that is used to optically block the frame store area and two temperature sensors. (top right) Camera head without one of the digitizer boards installed. This exposes the cooling system and the clock and bias board. (bottom) The 1kFSCCD standalone vacuum chamber.

B. The detector

The 1kFSCCD is the second generation X-ray CCD designed at LBNL using the concept of almost column parallel readout. The development started with a first small scale prototype featuring a pixel matrix of 20 x 480 pixels (figure 5.a) and intended as proof of principle of this architecture; on the same wafer we included the first generation Fast CCD (FCCD) with a 480 x 480 pixel matrix (figure 5.b), which was meant to extend this architecture to a larger scale prototype to be tested in real X-ray applications. The 1kFSCCD has a 1920 x 1920 pixel matrix and is shown in figure 5.c. All these sensors have square pixels on a 30 µm pitch. The sensors have 4, 96 and 192 output ports, respectively. Ten columns are multiplexed into each sensor output. In order to accommodate all these outputs, the last 6 rows of pixels on the top and bottom of the CCD have a tapered area. As described in [3], the fast CCD sensors can operate at high frame rate because they have many outputs and because their clock lines have been metal strapped.

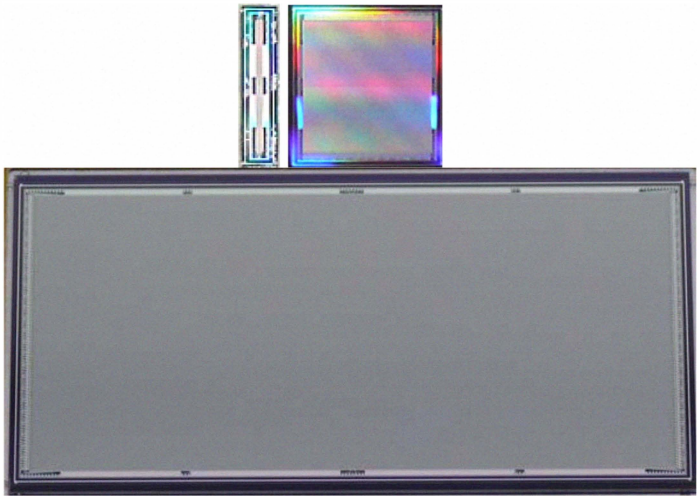

Figure 5 – Top left is the 20 x 480 CCD, top right is the 480 x 480 CCD and at the bottom is the 1920 x 960 1kFSCCD.

Many CCD sensors used in scientific applications operate in full frame mode. In this mode the entire pixel matrix is used to collect data. The 1kFSCCD can operate in this mode and in frame store mode. When operating in frame store mode the sensor is divided in three areas. The center area (half the size of the total pixel matrix area) is used to collect data. The other two areas (each one a quarter of the total pixel matrix area) are used to store a frame transferred in two halves from the imaging area after each exposure cycle. In order to differentiate the imaging area from the frame store area, a mechanical light block is added to the camera head as shown in Fig. 4 (top left). The time to transfer the image from the imaging area to the frame store is 500 µs. After the image is completely stored in the frame store area, it is readout from it at the same rate as the full frame mode but with two benefits. First, the frame rate doubles since the number of rows per frame is reduced by half and this lead to a readout time that is half of the full frame mode. Second, a new image starts being acquired during the frame store readout time effectively increasing the detector efficiency by reducing the dead time between frames.

All CCD sensors presented in this paper have the same output stage circuit as illustrated in Figure 6. We perform Correlated Double Sampling (CDS) to filter the CCD output signal. In normal CDS operation, charge is shifted out pixel-by-pixel. The RESET transistor, M2, is used to force the floating diffusion to a known voltage – which is then digitized. The signal charge is then deposited on the floating diffusion, and digitized again. Subtracting the signal and reset levels reduces low frequency noise components. The output source-follower M1 is biased off-chip by a load resistor R_L, and drives a capacitive load C_L. Transistors in our CCD process are of relatively poor quality, so that the time constant C_L/g_m sets an effective readout rate limit. As a consequence we collect only about 2/3 of the total charge due to the rise-time of the output transistor. Collecting all of the charge will improve signal-to-noise by 50%. To accomplish that we designed a new custom-made buffer chip that is described next.

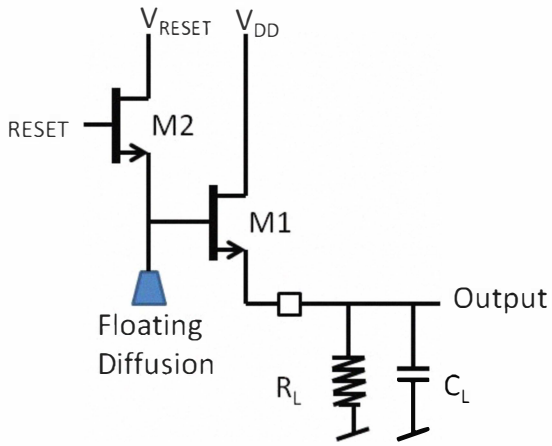

Figure 6 – Simplified schematics of the 1kFSCCD output stage.

C. *The buffer chip*

In order to operate the detector at increased speed and improve its performance, we have designed and fabricated a 16-channel chip in 0.35µm High Voltage CMOS technology to buffer video signals from the 1kFSCCD. This chip provides the current bias for the detector output and, if placed close to the 1kFSCCD, improves the signal-to-noise ratio of the overall system while simultaneously decreasing the overall power consumption. Figure 7 shows the block diagram of the buffer chip. The circuits inside the dashed lines are repeated 16 times in the chip. The source follower and the cascode transistors provide the bias current for the CCD outputs while the buffer circuit is used to buffer the video signal from the CCD output. The 1kFSCCD outputs are directly bonded to the buffer chip thus significantly reducing the load capacitance C_L. The CCD output stage impedance is about 4 kΩ while the output of the buffer chip is only 100 Ω. These two effects together improve the gain of the camera when running at high speed. The layout of the buffer chip is shown in Figure 8.

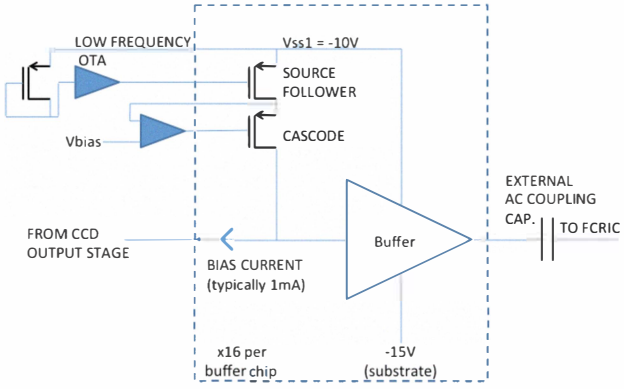

Figure 7 – Buffer chip simplified block diagram.

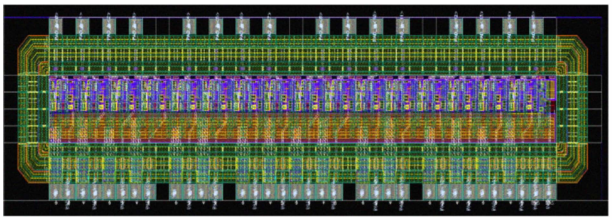

Figure 8 –Layout of the 16-channel buffer chip fabricated in 0.35 µm High Voltage CMOS technology

D. Digitizer board

The camera head for the 1kFSCCD contains two digitizer boards. Each digitizer board implements 6 custom readout ICs (named FCRIC2 – Fast CCD Readout Integrated Circuit generation 2) that pre-process and digitize the data from the top and bottom halves of the CCD. The FCRIC2 chip has been developed since the 1kFSCCD camera has 192 outputs and the high density of analog outputs makes discrete readout impractical. The CCD output is AC-coupled to the input stage of the FCRIC2, where the signal is amplified and converted from single-ended to differential. The differential output voltage signal is then integrated by a differential multi-slope integrator. This integrator integrates the video signal and the reset signal with opposite sign, this way thus implementing CDS by subtracting the reset level from the video level. The resulting signal is then digitized by a 12-bit pipelined analog to Digital Converter (ADC). The multi-slope circuit implements 3 gain stages and the digital result consists of the ADC mantissa and 2 bits representing the gain (1, 2, or 8). The FCRIC2 contains 16 identical channels sharing a common digital back end. They also share common analog services, including a band-gap voltage reference. The FCRIC2 was designed and fabricated in a commercial 0.25µm CMOS process, and covers a die area of 4.8 x 8.3 mm^2.
With respect to a first generation design (FCRIC [3]) two performance improvements have been made. The first one was to improve the power supply rejection ratio by changing the following items: (i) the bias circuitry for the first stage amplifier and the single-to-differential amplifiers have been modified following the techniques presented in [4]; (ii) in the same two stages, an on-chip 100kΩ resistor was added in series with the power supply line to improve its decoupling performance; (iii) the band-gap circuit was improved by adding a decoupling circuit as described in [5]. The second improvement was done to increase the maximum pixel rate that can be digitized. Simulation showed that the analog latch circuit that exists right before the ADC was limiting the maximum speed. We traced the cause of this slowness to the latch control circuit and improved its performance by adding a booster circuit. After that modification, the FCRIC2 was capable of processing a pixel in 800ns, better than the specification of 1µs and the performance of its first generation (1.2us).
Besides the FCRIC2 ICs the digitizer boards have two 3.3Vdc low dropout voltage regulators to reduce the noise level at the front-end of the ICs. The boards also have a clock fan-out circuit. Lastly, since all the communication from the digitizer boards is done in LVDS, these boards have converters from CMOS to LVDS for the control signal of the FCRC2.

E. Clock and bias board

A CCD sensor is essentially an analog device and in order to produce an image it requires analog biases and analog clocks. For soft X-ray applications the CCD must often be inside a vacuum chamber very close to the sample, and can typically be moved to view the sample at different angles. For the cFCCD [2] this was achieved by keeping all of the clocks and bias circuitry on the air side of the vacuum interface and connecting the analog bias and clock signals to the CCD through vacuum feed-through connectors and long cables. This had the advantage of keeping the sensor head lighter, and allowing the clock and bias electronics to be cooled with ambient air. Unfortunately, the long cables between the analog signals and the CCD degrade the signal-to-noise ratio of the CCD outputs. Typical noise for the system due to digital pickup was 157e^- with the long cables and 27 e^- when running with short cables.
To improve the signal-to-noise ratio on the 1kFSCCD, the clock drivers and bias electronics were moved inside the vacuum, closer to the CCD. The digital interface signals, which are not sensitive to long cable lengths, are routed as LVDS signals to and from the CIN module (see details later in this paper for the CIN). The LVDS signals provide the digital clock signals to the CCD, along with a digital interface to program local DACs. The digital clock signals go through clock driver chips that have their voltage rails controlled by the DACs. The DACs are also used to control the various bias signals needed by the CCD. With this arrangement, the typical distance that the signals need to travel from its source to the CCD is about 2 inches. Since the signal paths are contained in PCBs that directly connect to the CCD top board, they are static with respect to the camera head motion. This will eliminate a source of noise variations experienced with the cFCCD.
In addition to the LVDS signals, there is a power connector that provides the clock board with partially regulated power. The clock module further regulates the power with on-board components to minimize any noise coming into the system from the power cables.

F. Cooling system

The CCD is cooled to -50ºC using an immersion type chiller with the probe (evaporator) located within the camera body. The camera electronics are also cooled through this system but maintained at a higher temperature. Additionally, the camera must reside within a high-vacuum environment in order to both thermally insulate the system and avoid trapping gasses on the sensor due to its low temperature. Optionally, the camera can reside within either its own independent vacuum chamber (typically for hard X-ray applications) or within the user's experimental chamber (typically for soft X-rays

applications). Figure 9 shows a 3D model of the cooling system with a cut-out view to expose the internal circuits that cool the camera head electronics and sensor.

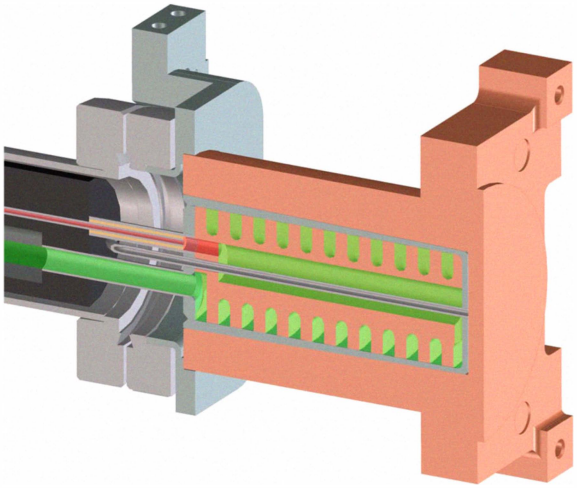

Figure 9 – Model of the 1kFSCCD in-vacuum cooling system. The green area is the expanding gas refrigerant.

G. Back end electronics and readout

The new LBNL pixel detectors are generating an ever-increasing data volume and bandwidth, and to better handle them a new scalable architecture for the back-end readout was needed. The Advanced Telecommunications Architecture (ATCA) PICMG 3.1 specification with a dual 10 Gigabit Ethernet backplane was chosen primarily for scalability, reliability, and availability.

The back-end electronics unit for the 1kFSCCD consists of an ATCA chassis loaded with a 10 Gigabit Ethernet switch board, the CIN, and a 4 Terabyte iSCSI storage board. The unit serves three functions: (i) real-time control of the camera head, (ii) low level image processing, and (iii) data capture and storage.

The CIN will be connected to the camera head either by copper cables or fiber optic links. Fiber coupling the camera head provides electrical and mechanical isolation that is critical for vibration sensitive experiments. These links send configuration data and timing pulses and retrieve digitized data from the camera head at almost 400 MB/s for the 1kFSCCD. The CIN can write data directly to the iSCSI storage board while sending down sampled images to a user interface for monitoring. Alternatively, the CIN can directly send data to remote servers for immediate processing.

Figure 10 shows the CIN board and Figure 11 the ATCA readout system.

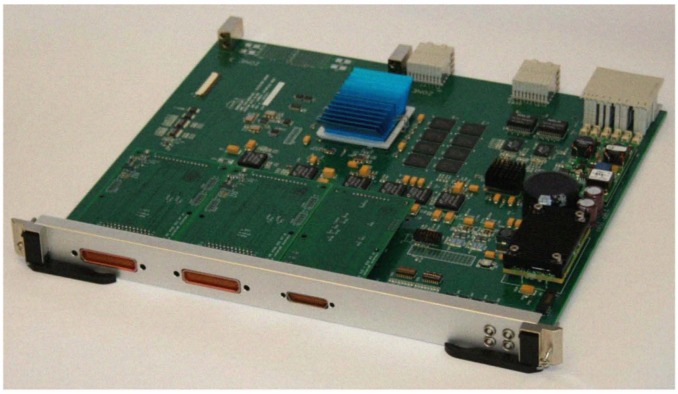

Figure 10 – Camera Interface Node board.

Figure 11 – Camera interface node board (left) and 1kFSCCD ATCA readout system (right).

II. RESULTS

The camera system has been built, assembled and several items that form this system have been tested, such as the detector, the buffer chip, the FCRIC2, the CIN node and the power supply.

The buffer chip has been tested stand-alone and presents a gain of 0.96 with linearity better than 0.5% for an input voltage swing of 500mV. It has also been connected to a CCD and functional performance has been verified. The rise time of the buffer chip has been measured and it is better than 4ns representing an improvement of two orders of magnitude when compared the CCD output stage alone. Figure 12 shows an oscilloscope screenshot acquired during the rise time test while Figure 13 shows the linearity of the buffer chip.

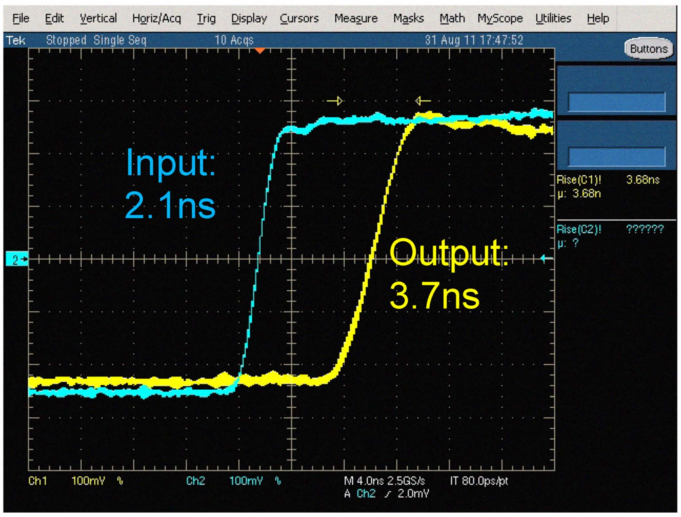

Figure 12 - Oscilloscope screenshot comparing the rise-time of a 1 MHz square waveform with 500 mV_{pp} amplitude at the input (blue trace) and at the output of one channel of the 1kFSCCD buffer chip.

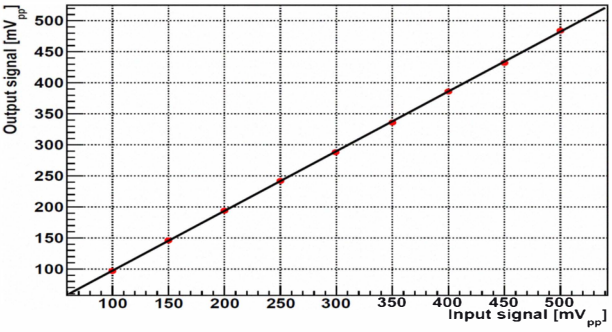

Figure 13 – Buffer chip linearity as measured by injecting a 1 MHz square waveform of varying amplitude in one buffer chip channel and measuring the amplitude at the corresponding output.

The FCRIC2 has also been tested and the PSRR has been improved by a factor of 20dB when compared with FCRIC. FCRIC2 has also been tested at a pixel period of 800ns validating the modifications done to the control circuit of the analog latch circuit. Currently the noise of the FCRIC2 with its input clamped to ground is $13e^-$ and it increases to $27e^-$ when connected to a CCD.

Several CIN node items have been tested. These include all FPGAs, both 1GbE and 10GbE links and all IOs that are connected to the camera head. In terms of communication performance we validated data being transferred from the CIN FPGA to a controller and to a RAID array through the 10GbE.

III. Remarks and Conlusions

In this paper we presented a new X-ray camera system that has been built at the Lawrence Berkeley National Laboratory. This system uses a 1kFSCCD with a 1920 x 960 pixel matrix. The sensor operates in two modes (frame store and full frame with 1920 x 1920 pixel readout) with maximum frame rates of 200 fps.

Initial tests have been done and some of the system characteristics have been reported. Future work will include a full characterization of the the camera using X-ray sources ranging from soft to hard X-rays, and the test of various options for the back process and detector thickness to get a broader energy range response.

Acknowledgment

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