

Comparison of Two Different Methods to Produce Thin-Window Silicon Drift Detectors

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Abstract—We have developed a new method to produce thin-entrance-window Silicon Drift Detectors. To produce the desired thin-entrance-window a double implantation was used. This implantation consists of Boron ions (dose of $1 \times 10^{14}/\text{cm}^2$ at 10 keV) plus a second implant of Phosphorus ions (with a dose of $4 \times 10^{12}/\text{cm}^2$ at 50 keV or dose of $9 \times 10^{11}/\text{cm}^2$ at 80 keV) through 500 Å of silicon dioxide. The second Phosphorus implantation compensates for the tail portion of the Boron ion implantation, so that the net Boron ion distribution will result in a thinner “dead” silicon layer and an elevated electric field near the silicon surface. We will compare test results from this newly developed thin-window with those from our previous development, where the thin junction was created using a single implantation of Boron ions (dose of $1 \times 10^{14}/\text{cm}^2$ at 10 keV) through a 500 Å thick silicon dioxide. All testing was done in the U3C beam line at the National Synchrotron Light Source at Brookhaven National Laboratory.

I. INTRODUCTION

THIS paper describes improvements made to the thin-entrance window on a custom Silicon Drift Detector (SDD). An array of these detectors is intended for use as an X-Ray Spectrometer (XRS), suitable for mapping the surface elemental composition of planetary bodies. This specific design is intended for mapping the Jovian system – mainly Europa. This development is a collaborative effort between NASA Marshall Space Flight Center (MSFC) and Brookhaven National Laboratory (BNL).

The total SDD array area is designed to be 25 cm^2 , with each pixel being around 2-3 mm across. The detector will operate at an extremely high rate of up to one million counts/s cm^2 and will be radiation dose tolerant to 250 krad. An energy resolution of around 100 eV at 280 eV will be maintained as well a power budget, excluding cooling, of 10 W. The elements of interests are: C, O, S, Na, Mg, K, Cl, N, Ca, P and Fe. Thus the detector will span the energy range of ~0.2 to 7 keV.

The major challenge of this system is detecting the lowest energy among all the elements of interests, which is

the K_{α} line of Carbon at 280 eV. This requires the detector and its readout electronics to have a low equivalent noise charge (ENC) of around 10 e^- . Low energy detection also requires use of a thin-entrance window that must be able to attenuate ultraviolet light while allowing x-ray transmission. Past experience has shown that a 50 nm aluminum layer is sufficient to eliminate surface charging while allowing better than 65% x-ray transmission for 280 eV x-rays. The silicon following this aluminum layer should be efficient from the surface. Any realistic implantation will result in a given junction layer depth and “dead” layer depth. In this work we have developed a new method for making the thin-entrance window for this detector. We will compare this method to our previous version to determine the best approach for producing SDDs for a Europa-type mission.

II. SIMULATION

Our first attempt at developing a thin window involved a single implantation method, and is described in a previous publication [1]. This previous method involved a single boron implantation (dose of $1 \times 10^{14}/\text{cm}^2$ at 10 keV) through a 500 Å silicon dioxide and an annealing was performed at 700 °C for 30 minutes, which was already developed for the purpose of to reduce the “dead” layer thickness. To reduce the “dead” layer thickness even more we decided to try a technique that involved multiple implantations. This decision was arrived at after determining that further reduction in the implantation energy has little effect on the detector performance and that a modification of the implantation has little effect on the detector process in general. The idea was to place an additional phosphorus implant directly behind the boron implant in order to compensate for the tail portion of the boron doping profile. The net boron ion distribution results in a thinner “dead” silicon layer and an elevated electric field [2, 3] near the silicon surface.

We use SILVACO 2D simulation tools to model this implantation. Its Athena tool allows us to build a desired device by following actual process steps. Its Atlas tool enables us to apply different bias conditions and to obtain potential profiles and the electric field distributions near the surface of the silicon.

Manuscript received November 13, 2009. This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC02-98CH10886. This work was also funded in part by the NASA Research Opportunities in Space and Earth Science, Planetary Instrument Definition and Development Program.

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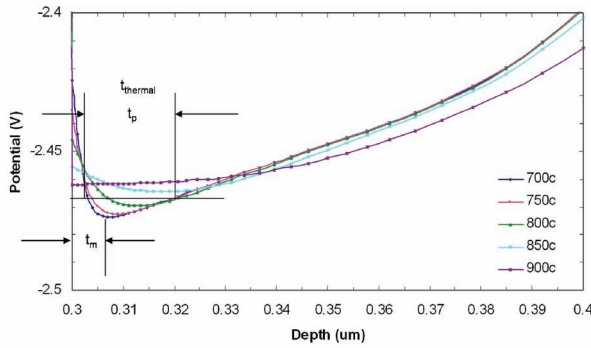


Fig. 1. The simulation results of potential profiles near the silicon surface for various annealing temperatures of the device produced by the single implant method of Boron 10 keV ($1 \times 10^{14}/\text{cm}^2$) implanted through 500 Å of SiO_2 on substrate of $n<111>$, $5 \text{ k}\Omega\cdot\text{cm}$ silicon.

The simulated electric potential profiles near the surface are shown in Fig. 1. From this plot it is evident that the 700°C annealing yields the thinnest possible “dead” layer for the implant energy and dose necessary for our application (Boron at 10 keV, and dose of $1 \times 10^{14}/\text{cm}^2$). These values have been fixed for all simulations discussed in this paper. The distance from the potential minimum to the surface corresponds to the “dead” layer, defined as t_m in reference [1] and also marked in Fig.1.

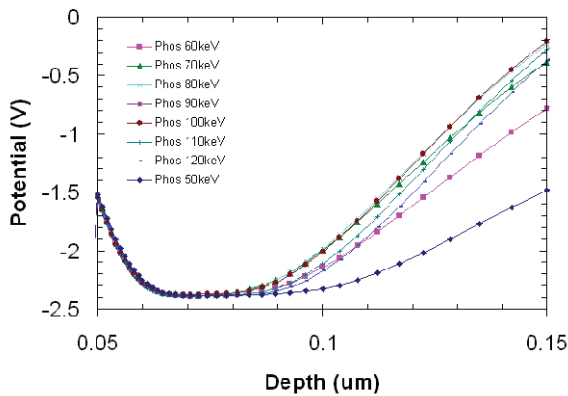


Fig. 2. The simulation results of potential profiles near the silicon surface for double implantation with various Phosphorous energies by fixing the Phosphorous dose at $1 \times 10^{13}/\text{cm}^2$ implanting through 500 Å of SiO_2 on a substrate of $n<100>$, $4.5 \text{ k}\Omega\cdot\text{cm}$ silicon.

By setting the optimum annealing temperature at 700°C, a series of simulations of electric potential profiles near the surface was conducted for various phosphorus implantation energies at a given dose of $1 \times 10^{13}/\text{cm}^2$ behind the boron implantation, as shown in Fig. 2. After determining the optimum implantation energy range we chose energies of: 90, 80, 70, 60 and 50 keV to simulate the potential profiles for a variety of phosphorous doses behind the boron

implantation. For each of the potential distributions we calculated the effective width $t_{\text{eff}} = \sqrt{(t_{\text{thermal}}^2 + t_{\text{range}}^2)}$, where t_{thermal} is the effective flat (width) due to the thermal potential KT/q (25 mV), as t_p (defined in reference [1]). The range of photoelectron in silicon is given by t_{range} and is a constant for a given x-ray energy ($\sim 5 \text{ nm}$ for 300 eV). In order to have a “dead” layer that is as thin as possible, we had to minimize t_{eff} . We also had to limit the magnitude of the electric field (due to additional phosphorus implantation) on the junction so that it does not reach the silicon breakdown field of $3 \times 10^5 \text{ V/cm}$. These constraints limited our choice of Phosphorous implant energy to 50 and 80 keV and their corresponding doses. Fig. 3 shows our final choice of boron and phosphorus double implantation doping profiles (B 10 keV, $1 \times 10^{14}/\text{cm}^2$ plus P 50 keV, $4 \times 10^{12}/\text{cm}^2$ and B 10 keV, $1 \times 10^{14}/\text{cm}^2$ plus P 80 keV, $9 \times 10^{11}/\text{cm}^2$) in comparison to the control implants in terms of the net doping profile. Figs 4 & 5 show the resulting electric field, and the potential profiles near the silicon surface, respectively, for the different implantation methods.

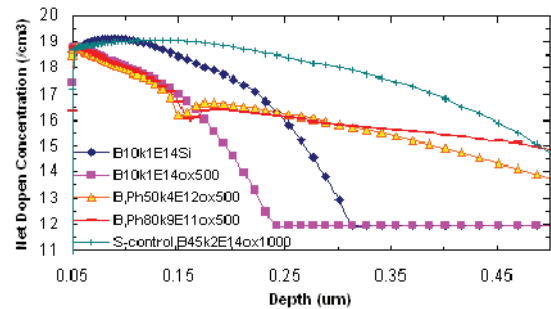


Fig. 3. The simulation results of the net doping profiles near the silicon surface from double-1 implant method (B 10 keV, $1 \times 10^{14}/\text{cm}^2$ plus P 50 keV, $4 \times 10^{12}/\text{cm}^2$) and double-2 implant method (B 10 keV, $1 \times 10^{14}/\text{cm}^2$ plus P 80 keV, $9 \times 10^{11}/\text{cm}^2$) compared to the single implant method (B 10 keV, $1 \times 10^{14}/\text{cm}^2$) through either 500 Å of SiO_2 or no SiO_2 .

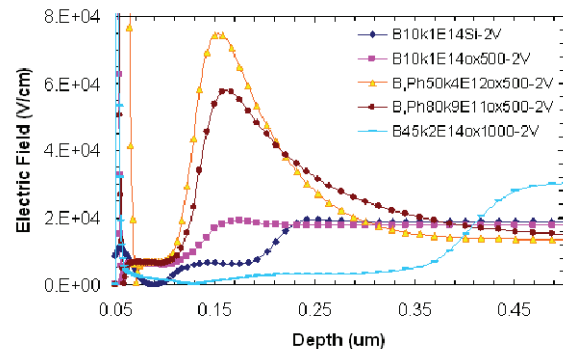


Fig. 4. The simulation results of the electric field near the silicon surface from double-1 implant method (B 10 keV, $1 \times 10^{14}/\text{cm}^2$ plus P 50 keV, $4 \times 10^{12}/\text{cm}^2$) and double-2 implant method (B 10 keV, $1 \times 10^{14}/\text{cm}^2$ plus P 80 keV, $9 \times 10^{11}/\text{cm}^2$) compared to the single implant method (B 10 keV, $1 \times 10^{14}/\text{cm}^2$) through either 500 Å of SiO_2 or no SiO_2 .

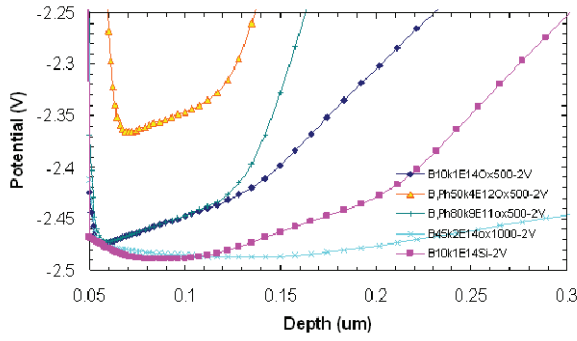


Fig. 5. The simulation results of the potential distribution near the silicon surface from double-1 implant method (B 10 keV, $1 \times 10^{14} / \text{cm}^2$ and P 50 keV, $4 \times 10^{12} / \text{cm}^2$) and double-2 implant method (B 10 keV, $1 \times 10^{14} / \text{cm}^2$ plus P 80 keV, $9 \times 10^{11} / \text{cm}^2$) compared to the single implant method (B 10 keV, $1 \times 10^{14} / \text{cm}^2$) through either 500 Å of SiO_2 or no SiO_2 .

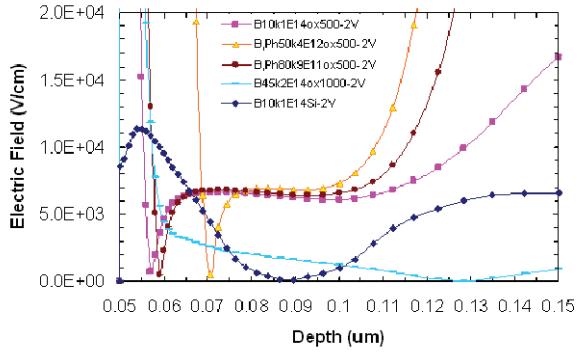


Fig. 6. This is a blow up of the Fig. 4. It shows the detailed electric field distribution near the surface of the silicon. The definite “dead” silicon thicknesses, t_{dSi} , were obtained from the graph corresponding to the lowest electric field (sharp points) position in silicon depth.

III. FABRICATION AND DC CURRENT TEST

Following this recipe, we fabricated two groups of diodes (p+/n/n+) using our new “double” implant method: “double-1” (B 10keV, $1 \times 10^{14} / \text{cm}^2$ plus P 50 keV, $4 \times 10^{12} / \text{cm}^2$) and “double-2” (B 10keV, $1 \times 10^{14} / \text{cm}^2$ plus P 80 keV, $9 \times 10^{11} / \text{cm}^2$) together with control diodes using our standard single implant method: “s-control” (B 45 keV, $2 \times 10^{14} / \text{cm}^2$) and the mini-control samples with single implant: “single” (B 10 keV, $1 \times 10^{14} / \text{cm}^2$). We also included a single implant control sample in the test, the so called “old-single” (B 10 keV, $1 \times 10^{14} / \text{cm}^2$), which had been fabricated in the past without back-sputtering and with a long annealing time. Then these two groups of diodes were tested for the DC current measurement at the National Synchrotron Light Source (NSLS) UV beam line U3C [4] located at BNL. This beam line is used for absolute radiometric calibration in the 50 to 1k eV x-ray range. The related parameters of the diodes are listed in Table I. The test results are shown in Figs. 7, 8, 9, 10 and 11.

Table I

Second U3C run					
Diode #	2	3	4	5	6
Device #	1627-83	1628-110	1627-6	1628-19	1481-10
Impl.	double-2	single	double-2	single	old-single
Al (um)	0.118	0.123	0.113	0.118	0.158
Al Err. (um)	0.010	0.002	0.003	0.004	0.003
Area (cm ²)	0.1	0.1	0.25	0.25	0.25
First U3C run					
Device #	1581_17	1581_14	1481_10	1602_22	1600_25
Impl.	double-1	double-1	old-single	double-1	s-control
Al (um)	0.086	0.112	0.158	0.111	0.088
Al Err. (um)	0.007	0.002	0.003	0.002	0.003
Area (cm ²)	0.25	0.25	0.25	0.25	0.25

IV. RESULTS AND DISCUSSION

The test results in Fig. 7 show that the efficiency of the “old-single” implant diode with a long annealing time is the best among the rest of the diodes in the first U3C beam test. Long hour annealing reduces the defects caused by implantation. Signal electrons drifting through the implanted region have a smaller probability to be captured by traps, thus, increasing the efficiency of the detector. The “double-1” implant diode’s efficiencies seem to be better than the “s-control” diodes. Among different wafers: 1581_14 and 1602_22, when the implantation parameters are identical, the diodes have different efficiency responses for each different processing treatment. Moreover, among the same wafer: 1581_17 and 1581_14, the efficiencies of the different diodes are different. This means that the processing needs to be more uniform.

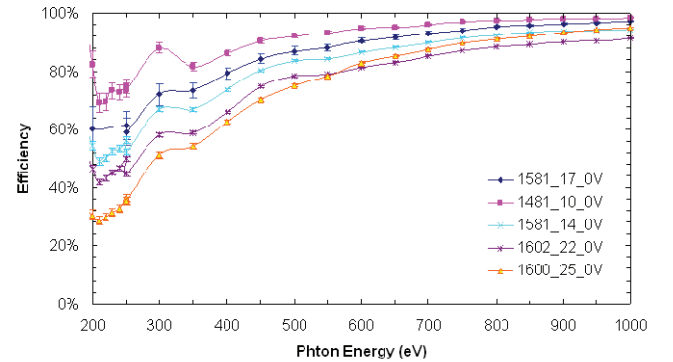


Fig. 7. The DC current result of the first U3C run show the efficiencies of different samples fabricated in different parameters verses the photon energies. The results are after correcting for aluminum, definite “dead” silicon and native silicon dioxide.

Fig. 8 shows that the efficiency of the “old-single” implant control diode deteriorates in the second U3C beam test. This diode was produced without back-sputtering during the fabrication process. Therefore, there is a thin layer of oxide remaining between the silicon and the metal contact layer. In addition, Fig. 8 also shows that the efficiency of the mini-single-implant control diodes, so called “single” implant, are similar to the ones of the “double-2” implant diodes. Among the same wafer: 1627-83 and 1627-6, the efficiencies of the different diodes are very similar. The little difference is due to the size difference which causes different leakage current. This means that the process have been improved in terms of uniformity.

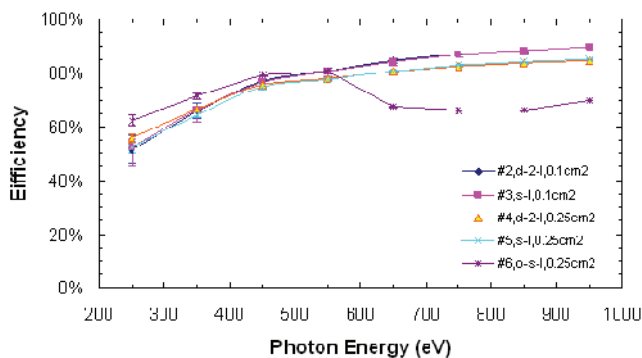


Fig. 8. The DC current result of second U3C run shows that the efficiency of the old-single implant diode deteriorates. The results are after correcting for aluminum, definite “dead” silicon and native silicon dioxide.

Fig. 9 shows that higher beam fluxes result in decreased diode efficiencies. This confirms that there is a thin oxide layer remaining between the silicon and the metal contact. The diode deterioration is due to radiation damage, which causes an increase of the oxide charges in this thin oxide layer, and effectively extending the “dead” silicon thickness. This results in a decrease of the efficiency of the detector’s performance.

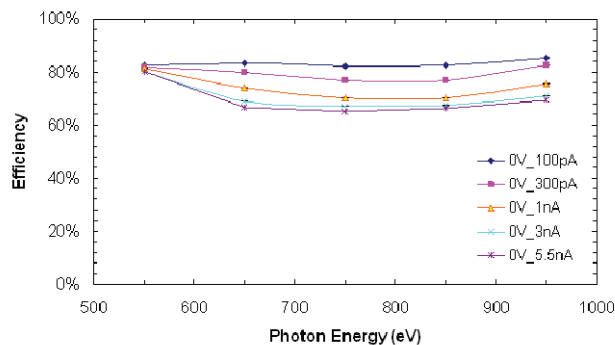


Fig. 9. The DC current result of the old-single implant diode, which was produced without back-sputtering, shows its efficiency deteriorating

with an increase of the beam fluxes due to a thin layer of oxide between the aluminum layer and the silicon substrate. The results are after correcting for aluminum, definite “dead” silicon and native silicon dioxide.

Fig. 10 shows that the diode that was fabricated with back-sputtering (used to remove the thin oxide layer between the silicon and the metal contact) did not exhibit a decrease in efficiency caused by higher beam flux. Instead, the detector became more resistant to radiation. Therefore, the removal of the thin layer of silicon dioxide between the silicon substrate and the aluminum metal contact in the entrance window can result in a radiation hardened detector, ideal for operation in harsh radiation environments such as that of Europa.

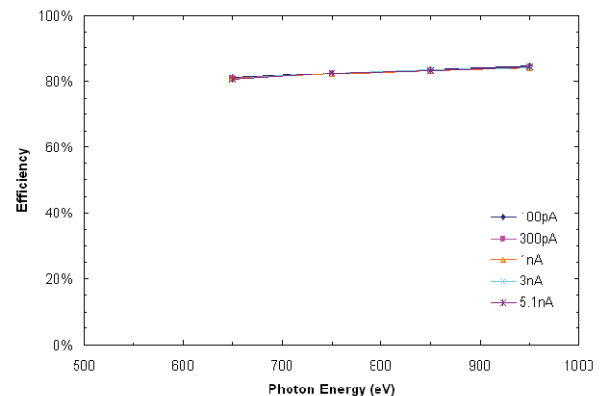


Fig. 10. the DC current result of the diode, which was produced with back-sputtering to remove the native oxide between aluminum layer and the silicon substrate, shows that its efficiency is not influenced by the beam fluxes. The results are after correcting for aluminum, definite “dead” silicon and native silicon dioxide.

Fig. 11 shows that “double” implanted diodes (“double-1” and “double-2”) have better efficiency responses than our standard implanted diode (“s-control”), but not necessarily better than the mini-single implanted diode (“single”). The “double-1” implanted diodes have slightly better efficiency than the “double-2” implanted diode. The “old-single” implanted diode deteriorated from the first U3C test to the second U3C test. This confirms that this “old-single” implanted diode was fabricated without a back-sputtering process. There must still be a thin layer of silicon dioxide between the silicon and the aluminum layer. It is believed that radiation damage is responsible for this diode deterioration, due to the presence of this thin layer of silicon dioxide.

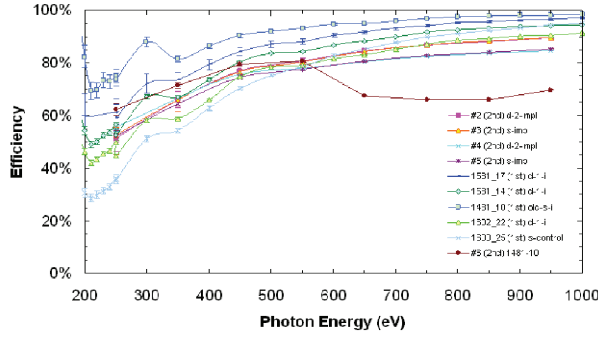


Fig. 11. The results of the DC current test show the efficiencies of these two groups of diodes. The results are after correcting for aluminum, definite “dead” silicon and native silicon dioxide.

All efficiency data were modelled using the combined transmission through an aluminium window layer (t_{Al}), native silicon dioxide (t_{SiO_2}), definite “dead” silicon (t_{dSi}) and silicon “dead” layer (t_{Si}) [1, 5], given as follows:

$$eff_{(model)} = e^{-t_{Al}/\lambda_{Al} - t_{dSi}/\lambda_{Si} - t_{SiO_2}/\lambda_{SiO_2} - t_{Si}/\lambda_{Si}}.$$

X-ray attenuation lengths (λ) are taken from the CXRO online database. The aluminium window layer’s thickness, t_{Al} , is taken from the Table I. The native silicon dioxide thickness, t_{SiO_2} , is 0.003 μm . The definite “dead” silicon layer thickness, t_{dSi} , is the position in silicon depth corresponding to the lowest electric field (sharp points) in Fig. 6. The graph is a blow up of the Fig. 4. The detailed electric field distribution near the surface of the silicon can be clearly seen, where t_{dSi} is 0.021 μm for “double-1” implant, t_{dSi} is 0.0095 μm for “double-2” implant and t_{dSi} is 0.007 μm for “old-single” implant. Only t_{Si} is the fitting parameter, therefore we obtain the “dead” layer thicknesses, t_m , listed in Table II for various process parameters.

Table II

Second U3C run					
Diode #	2	3	4	5	6
Device #	1627-83	1628-110	1627-6	1628-19	1481-10
Impl.	double-2	single	double-2	single	old-single
Back-sputtering	yes	yes	yes	yes	no
Anneal at 700°C	30 min	30 min	30 min	30 min	17 hr
Area (cm ²)	0.1	0.1	0.25	0.25	0.25
t_m (um)	0.095	0.097	0.103	0.107	0.094
First U3C run					
Device #	1581_17	1581_14	1481_10	1602_22	1600_25
Impl.	double-1	double-1	old-single	double-1	s-control
Back-sputtering	yes	yes	no	yes	yes
Anneal at 700°C	30 min	30 min	17 hr	30 min	30 min
Area (cm ²)	0.25	0.25	0.25	0.25	0.25
t_m (um)	0.061	0.084	0.036	0.121	0.143

I. CONCLUSION

The detector fabricated with a “single” implant through 500Å of oxide, without back-sputtering and with long hours of annealing, exhibits the best efficiency. However, this efficiency was seen to deteriorate by radiation damage. Long hour annealing does reduce the defects caused by implantation. Signal electrons drifting through the implanted region have a smaller probability to be captured by traps, and thus increase the efficiency of the detector.

The back-sputtering process, which removes the thin silicon dioxide between substrate and metal contact, can improve the detector’s radiation hardness.

The detectors to which the “double” implant method was used did not show a significant improvement in terms of efficiency and “dead” layer thickness compared to the ones fabricated with “single” implant through 500Å of oxide with back-sputtering. The detectors fabricated with the “double-1” implant method have a slightly better efficiency and “dead” layer thickness than the ones fabricated with “double-2” implant.

The above conclusions are only based on this DC current test, which is not complete picture of the “dead” layer investigation. It is a first step for the production of the

SDDs [5] for this project. Further charge collection spectra measurements on SDDs are needed.

ACKNOWLEDGMENT

The authors would like to thank R. Beuttenmuller for his support during the DC current experiment and B. Kennedy for general help.

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