

The XAMPS detector for the X-ray Pump-Probe instrument at LCLS

Gabriella A. Carini, *Member, IEEE*, Angelo Dragone, *Member, IEEE*, Wei Chen, Jack Fried, Anthony Kuczewski, Zheng Li, Joseph Mead, Paul O'Connor, Jean-Francois Pratte, *Member, IEEE*, Pavel Rehak, Kevin Wolniewicz and D. Peter Siddons.

Abstract— An integrating fast readout detector is being developed for the X-ray Pump Probe (XPP) instrument at the Linac Coherent Light Source (LCLS). The detector is based on X-ray Active Matrix Pixel Sensors (XAMPS) with their dedicated readout ASICs. It covers a dynamic range of more than 10,000 photons of 8 keV energy with a resolution better than half photon FWHM. The frame of 1024 x 1024 pixels will be read out within the repetition rate of the X-ray laser pulses which will be as fast as 120 Hz. The structure of the sensor allows full fill factor and ~100% efficiency at the energy of interest.

I. INTRODUCTION

The Linac Coherent Light Source (LCLS) is the first X-ray free electron laser (FEL) already operational in Menlo Park (CA) [1]. Particularly the X-ray Pump-Probe (XPP) instrument will use the hard X-ray pulses, namely 8 keV, from the LCLS to probe the transient state of matter generated by a fast optical laser. The instrument is comprised of an integrating detector with large dynamic range, large area and fast readout needed to cope with the intense (10^{12} photons), short (<100 fs) pulses at the expected 120 Hz repetition rate.

The detector is being developed at Brookhaven National Laboratory (BNL) and is based on X-ray Active Matrix Sensors (XAMPS) with their dedicated front-end ASICs. The 1 Mpixels frame has to be read out within the ~8 ms allowed by the maximum operating repetition rate with a readout noise better than 1 photon, providing a dynamic range of 10,000 photons per pixel per frame and a quantum efficiency better than 90% at 8 keV. The point spread function is defined by the pixel size of $90\ \mu\text{m} \times 90\ \mu\text{m}$.

The challenging requirements for this system have been accomplished by the 64 x 64 pixel prototypes and the final 1024 x 1024 pixel system is currently being completed.

II. XAMPS AND FRONT END ASIC

The XAMPS is a monolithic device built on high resistivity silicon [2-6]. Typically the 100 mm silicon wafers have a resistivity greater than 4 k Ω ·cm and a thickness of

400 μm . Square matrices with n rows and n columns with $n=16, 32, 64, 128, 256, 512$ are fabricated on each wafer. Each pixel of the matrix is $90\ \mu\text{m} \times 90\ \mu\text{m}$ and contains an integrated JFET switch to control the charge readout. The channel of the JFET is formed by a deep n-implant, while standard n^+ and p^+ implants constitute drain/floating-source and gate respectively. The pixels are separated by a combination of p^+/p -deep implants and a deep p-implant under the drain prevents the charges to drift toward the drain. The junction is formed in the backside by a typical p^+ implant which is used to fully deplete the device.

Two phases characterize the operation of this device: data accumulation and data readout. During the first phase the JFET switches are open. The charge generated in the sensor by interactions with an absorbed photon or by thermal generation drifts. It is stored on a capacitor which occupies most of the pixel area. The switches are then closed during the second phase to allow the charge to flow to the drain, that is connected to readout lines. A sufficient time to readout the 3.5 pC corresponding to the full well capacity of the pixel is a few microseconds.

The sensor is wire bonded as shown in Fig. 1 for the case of a 64 x 64 pixels prototype and read out by the dedicated Front-End XAMPS (FEXAMPS) ASIC [7].

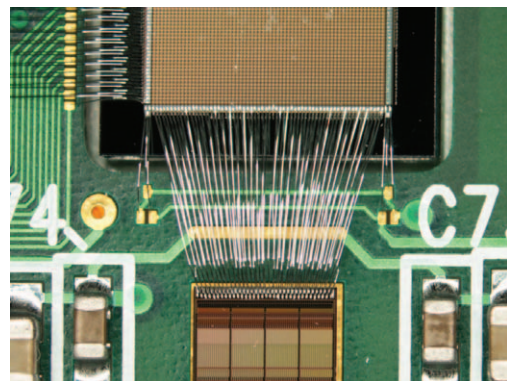


Fig. 1. 64 x 64 pixels sensor and dedicated ASIC wire bonded on the prototype board.

Due to the periodic structure of the LCLS beam, the FEXAMPS ASIC is designed according to a time-variant approach to maximize the readout speed. It provides low-noise charge integration, real time adaptive filtering and correlated double sampling. In order to cope with the large input dynamic range a charge pump scheme implementing a zero-balance measurement method has been introduced. It provides an on chip coarse amplitude digital conversion and thus it allows a measurement of the residuals with the

*Manuscript received November 20, 2009. Use of the National Synchrotron Light Source, Brookhaven National Laboratory, was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-98CH10886."

Gabriella A. Carini, Wei Chen, Jack Fried, Anthony Kuczewski, Zheng Li, Joseph Mead, Paul O'Connor, Pavel Rehak and D. Peter Siddons are with Brookhaven National Laboratory, Upton, NY 11973 (telephone: 631-344-3004, e-mail: carini@bnl.gov).

Angelo Dragone is with SLAC National Accelerator Center, Menlo Park, CA 94025 USA.

Jean-Francois Pratte is with Universite' de Sherbrooke, Sherbrooke, Quebec, Canada.

required resolution. The residuals conversion is performed with an external 14-bit ADC.

The 64 channels of the ASIC are arranged in 4 groups of 16; each one connected to its own analog and digital multiplexers and dedicated outputs. The 4 blocks are readout in parallel to speed up the readout procedure. The acquisition is controlled by a single periodic signal (slot control, SC) whose period defines the readout time slot. This signal is synchronized to the LCLS beam trigger. During the active part of the SC period the charge is read out from the pixels and sampled. During the inactive period stored data are readout and the system reset. Each channel implements a low noise charge integrator with a programmable double polarity pulsed reset, a 2nd order non inverting programmable LP filter, two double correlated double samplers and a discriminating charge pump circuit.

A new version of the FEXAMPS ASIC has been designed to extend the dynamic range, improve the linearity and resolution of the system [Fig. 2]. It implements also a double gain preamplifier and a programmable number of pump steps. The new ASIC (as well as the previous one) has been fabricated in TSMC CMOS 0.25 μm technology. It has already been tested and results are reported in the next paragraph.

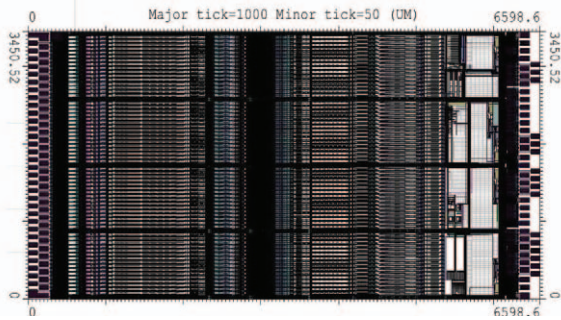


Fig. 2. Layout of the new version of FEXAMPS.

III. EXPERIMENTAL RESULTS

A prototype board with a 64 x 64 pixel XAMPS sensor, a FEXAMPS ASIC for the readout and a SwitcherIIb ASIC [8] to drive the switches has been fabricated. Each column of the sensor is read out by a dedicated electronics channel and each row is driven by an output of the SwitcherIIb chip. Discrete external 4 channel, 14 bit and 20 Msample/s commercial ADC are used to convert the output analog signals from the FEXAMP ASIC. It is connected via an LVDS interface to a FPGA prototyping board (Xilinx ML505 Virtex-5) that controls the acquisition. The data acquisition system readout through a Labview VI using 1 Gb ethernet. It should be noted that due to the low leakage current of the sensors all the measurements reported were performed without cooling.

A. Low noise measurements

To study the noise performance the prototype system was tested at the readout time required to read the full Mpixel frame $\sim 8 \mu\text{s}$ per row. The cumulative histogram distribution for the system is shown in Fig. 3. It can be noticed that

sigma corresponds to 5 ADU that is 660 e- rms (0.29 8 keV-photons rms) or 0.66 8 keV-photons FWHM.

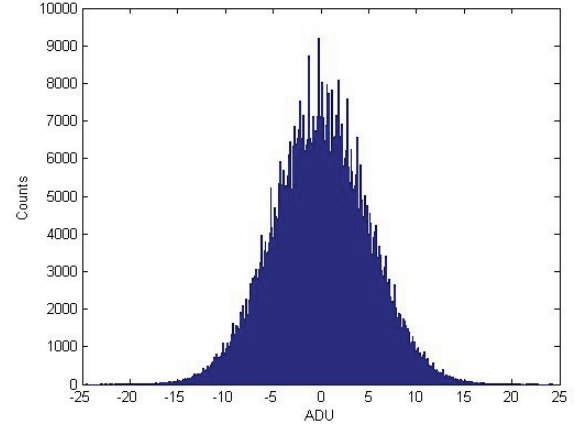


Fig. 3. Cumulative histogram distribution as function of ADC units.

B. Charge pump and dynamic range

A new feature of this FEXAMPS ASIC is the possibility to optimize the charge pump by settings four parameters: gain, number of pumps, pump threshold and pump height. As previously mentioned the chip implements a double gain preamplifier and a programmable number of pump steps. In the case of single gain mode we use 8 pump steps and in the case of double gain 16 steps. Then the pump threshold and the pump height can be adjusted to maximize the dynamic range as shown in Fig. 4.

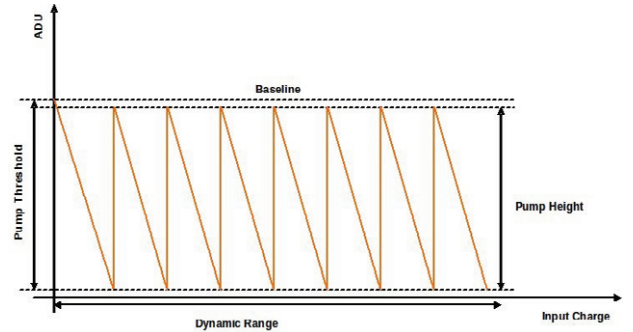
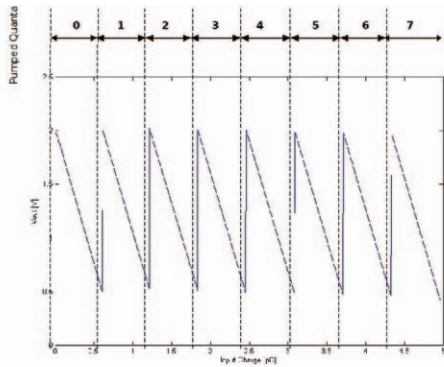


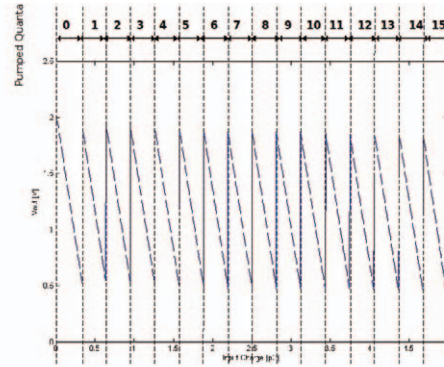
Fig. 4. Optimization of the dynamic range by setting the charge pumps parameters.

In Fig. 5 results of tests on the FEXAMPS ASIC for the cases of single gain with 8 pump steps (a) and double gain with 16 pump steps (b) are shown. The measurements were performed with a 20 pF capacitor at the input to simulate the sensor capacitance and 1 pF capacitance to inject with an external pulser.

The full well capacity of the sensor pixel has been studied at the National Synchrotron Light Source (NSLS) at the beamline X12A. For this experiment a monochromatic beam of 8.3 keV was focused with a pair of Kirkpatrick-Baez mirrors down to a size of $\sim 30 \mu\text{m} \times 50 \mu\text{m}$ at the detector position to illuminate a single pixel and collect data at several integration times. The results are shown in Fig. 6.



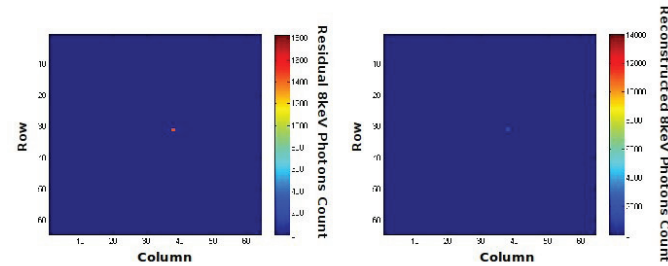
a)



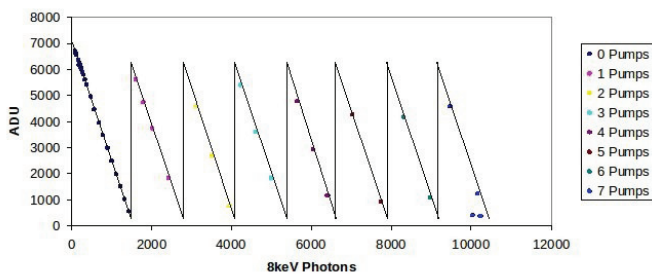
b)

Fig. 5. Pump quanta vs injected charge for the cases of single gain with 8 pump steps (a) and double gain with 16 pump steps (b).

The system was operated with the nominal readout time parameter of 8 microsecond per row. In order to accumulate more charge the integration time was adjusted from 0.1 to 30 milliseconds. This enabled us to activate each charge pump and saturate the sensor (see Fig. 6).



a)



b)

Fig. 6. Full well capacity studied on a single pixel: a) residual value just before and after soon the first pump; b) entire dynamic range for the case of single gain and 8 pump steps.

The two last points of this curve move to the left because the data are background subtracted: in fact the leakage current increase with the integration time.

IV. FINAL REMARKS AND CONCLUSIONS

The final detector comprises four XAMPS arrays of 512 x 512 pixels. The four sensors will be mounted onto a single board and wire bonded row by row and column by column to form a full module. The sensors are tested prior to cutting and mounting on a double-sided probe-card testing machine developed in house. The main board contains also sixteen 64-channels FEXAMPS ASICs for the readout, sixteen Switcher II ASICs and eight 14-bit ADCs. A second board is used as interface between the detector head and a Reconfigurable Cluster Element (RCE) developed at SLAC. A power load analysis reveals that a modest temperature profile inside the detector housing can be maintained by water-cooling and with a proper heat distribution (Fig. 7). The detector will be mounted on a robot arm.

Since the readout electronics is wired bonded at the side of the sensor and the ring JFET integrated in the pixel is intrinsically radiation hard [9] the detector is radiation hard.

Finally tests of the first small prototypes of 64 x 64 pixel XAMPS array read out with the 64-channel FEXAMPS showed that the system in a small scale is functional and meets the desired specification.

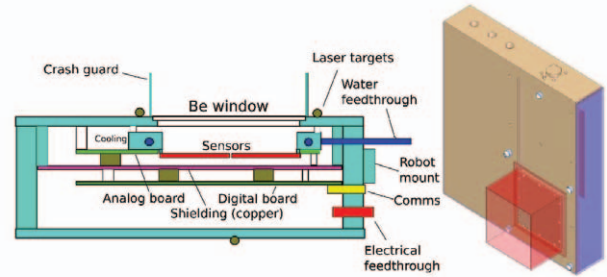


Fig. 7. Schematic and 3D rendering of detector assembly and housing.

ACKNOWLEDGMENT

The authors wish to thank Rolf Beuttenmuller, Don Pinelli, John Triolo, Rich Mitcha, Shu Cheung, Tony Lenhard, Don Elliott.

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