EPI's partner collaborations and open source embrace fuel Europe's chip design landscape

Best practice category: Partner collaboration and open ecosystems

Stakeholder group: Associations and trade organisations

Value chain position: R&D

General Information

The European Processor Initiative (EPI) is a project under the EuroHPC JU whose aim is the design and implementation of a roadmap for a new family of low-power European processors for exascale computing, high-performance Big Data and a range of emerging applications. To that end, EPI brings together 30 partners from 10 European countries – including research institutes, universities and industry stakeholders – who collaborate to advance Europe's high-end chip designing capabilities.

The project spans three streams: General Purpose Processor, Accelerator Processor and Automotive. The project's Phase 1 spanned nearly three years (December 2018-November 2021), with Phase 2 kicking off in January 2022.

Activities and best practices

The project's Phase 1 concluded with several accomplishments. Firstly, the EPI partners defined the architectural specifications of Rhea, the first generation of the EPI General-Purpose Processor (GPP) implementation and its future derivatives. Moreover, they developed the European Processor Accelerator (EPAC) test chip proof of concept by relying on wholly European design and RISC-V, an open standard Instruction Set Architecture (ISA). Finally, in its Automotive stream, EPI partners developed a proof of concept for an innovative embedded high-performance computer (eHPC) platform and associated software development kit (SDK), paving the way for cost-effective and safe autonomous cars.

Launched by the Euro-HPC Joint Undertaking in January 2022, the EPI Phase 2 builds on the achievements of Phase 1. With Phase 2, EPI hopes to strengthen the competitiveness and leadership of European industry and science, develop European microprocessor technology with drastically better performance and power ratios, and tackle important segments of both broader and emerging HPC and big-data markets. In particular, EPI will move forward with the development of the European microprocessor, targeting future European exascale supercomputers by applying technological enhancements to the baseline of Rhea. Therefore, the work on the "Common Platform" – which is common to the GPP and Accelerator streams – will be further developed at hardware and software levels.

In order to demonstrate the capability of EPI architecture for Autonomous HPC, the consortium focuses on finding and optimising the HPC scaling path within another embedded market, namely video surveillance for smart cities and infrastructures. The latter use cases will be evaluated, analysed and profiled using simulation tool chains of all the platforms developed in Phase 2, with the end goal of extracting key algorithms related to security, energy efficiency and ease of deployment requirements. As an autonomous application requires a full scale HPC processor from edge up to the central HPC cloud, co-design with the other streams will define and properly finetune all the parameters required.

To enable continuum computing – computing that combines edge with IoT, AI, HPC and networks – the applications on edge must be able to exchange with HPC servers. The EPI-based blade developed for HPC must provide the adequate network interface for connection to edge networks. Therefore, HPC vendors and end-users will analyse how EPI technologies fit within the HPC market and propose valuable HPC products based on the General Purpose processor Rhea2 or accelerators developed in Phase 2.

The different proposals must meet standard HPC requirements, with a focus on security, but also new requirements, such as a training phase in ML for emerging applications. Several scenarios are under analysis for high-speed interconnect between HPC nodes, all seeking the best technology and topology for the needed bandwidth and latency.

Challenges addressed with this practice

EPI facilitates a collaboration among 30 partners from various research institutes, universities, and industry stakeholders to foster a comprehensive ecosystem for semiconductor research and development. By pooling together knowledge bases and cross-sectoral expertise, EPI enables the efficient development of a common European solution. Finally, by using open source solutions when possible, the provided solutions help to avoid vendor lock-in and minimise reliance on proprietary software, thus enhancing the digital sovereignty in the EU semiconductor sector.