

A Model for Flash Analog-to-Digital Converters with Bit-Extended Error Table Linearization

Christopher D. McGuinness, Eric J. Balster, Frank A. Scarpino

Abstract—This paper provides a fundamental overview of important metrics and concepts regarding A/D nonlinear distortion. Once reviewed, a sub-bit compensation technique is presented, analyzed, and simulated in the context of a high-speed flash converter. A model is presented to represent the compensator as well as the pre-compensated converter. It is shown that the BEET method of error compensation creates a greater SFDR and SINAD for a converter than traditional error-table compensation. Yet, the BEET method has only a slight increase in hardware complexity compared to traditional error tables.

Index Terms—Error correction, data conversion, nonlinear distortion, compensation, table lookup, simulation.

I. INTRODUCTION

High speed and precision analog to digital converters are increasingly important as digital technology continues to absorb traditional analog signal processing applications. The growth of digital signal processing embraces broad application areas and increasingly includes higher clock rate digital circuitry. Increasing digital clock rates facilitate implementation of digital signal functionality for higher frequency signals. This effect feeds an increasing demand for high rate converters. Also, as digital signal processing migrates further into RF front ends, dynamic range and other metrics, such as spur free dynamic range, become important parameters for high rate A/D converters. In some cases, designers may supply on-chip linearization or calibration [6]. In situations where the end user requires on-demand linearization and recalibration, but this capability is omitted from the preferred commercial component, it may be possible to provide such means by the use of an FPGA integrated with other suitable components (e.g., D/A converter) [10, 12]. Many compensation techniques, in current form, are not well suited for such implementations [1, 2, 13]. Other recalibration techniques, such as the bit-extended error table (BEET) method, can be readily adapted for high-speed FPGA integration [8]. In this paper, a BEET compensation technique is presented in contrast to a traditional error table compensator. It is found that the BEET technique yields greater improvements in spur-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SINAD) than its traditional counterpart. Section 1 discusses the metrics and terminology

used for analyzing ADC nonlinearities. Section 2 provides a brief overview of ADC linearization methods. Section 3 discusses the BEET method of compensation. Section 4 provides simulation results of BEET compensators applied to flash converters. Section 5 introduces an implementation of BEET compensation for single and interleaved flash converters.

II. ADC NONLINEARITIES

ADC nonlinear distortion can be attributed to a few sources. Clock jitter, gain error, nonuniform quantization bins, and quantization noise are among the most significant contributors [3, 9]. For the purposes of this development and analysis, the ADC's nonlinearities are considered static.

A. Quantization Noise

The difference between the analog, sampled signal and a digital signal may be modeled as a quantization noise signal added to the original signal. Therefore, the spectrum of the sampled signal consists of the original analog spectrum and its images as well as a quantization noise floor [5]. If the quantization noise is sufficiently white (e.g., with the assistance of a dithering signal), then the signal to quantization noise (SNR) floor is expressed as

$$SNR = 6.02N + 1.76(dB), \quad (1)$$

where N is the number of bits which the converter produces. For an 8 bit converter, the signal to noise ratio is approximately 50dB. If a larger signal to noise ratio is desired, a converter that produces more bits may be employed. Therefore, in principle, the application may achieve as large a signal-to-quantization-noise as desired.

B. Nonuniform Quantization Bins

Aside from quantization error, another cause of nonlinearity in an ADC is irregular quantization bin sizes. In an ideal quantizer, the sampled analog signal will be accurately measured and coded according to a linear transfer function. However, this is often not the case. Deviation of the actual quantization transfer function from the ideal case is quantified with dynamic nonlinearity (DNL) and integral nonlinearity (INL) values.

DNL represents the variation between the actual and ideal range of input values that correspond to each output code, given by:

$$DNL(k) = (\Delta_N(k) - \Delta)/\Delta \quad (2)$$

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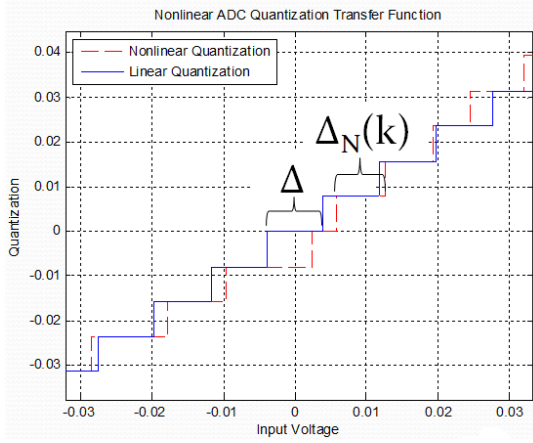


Fig. 1. Varying Bin Sizes: An Example of DNL

Where $\Delta_N(k)$ is the k^{th} quantization level's width and Δ is a linear quantization bin's width. Figure 1 illustrates this definition of DNL. The DNL contains N values and, assuming that the converter transfer function is monotonic, the DNL has a maximum range of $[-1, \infty)$. A DNL of 0 will yield an ideal bin width while a DNL of -1 will yield a missing code.

An ADC's transfer function cannot be described solely with DNL, though. In order to appreciate the affect of the DNL, the INL is defined as:

$$INL(k) = \sum_j^k (DNL(j)) \quad (3)$$

For a linear transfer function the DNL is zero and consequently the INL is also zero. If the DNL is not zero, then the INL is non-zero and the converter transfer function departs from the linear case. The INL departure from the linear case is the primary cause of spurious responses from the converter.

C. Offset and Gain Error

Also known as the full-scale error, the offset error is the difference between the ideal and actual transfer function's threshold for the final quantization level. This is also equal to the k^{th} INL term. It provides a good understanding of how many bits of error are associated with the output terms.

The gain error is equal to the offset error when the actual transfer function is translated to begin at the ideal's origination. The equivalent of this term in INL is the addition of the 1st and the k^{th} terms. Gain error also demonstrates the difference between the actual transfer function's slope and the ideal's slope.

III. IMPORTANT METRICS FOR ADCs

Figure 2 provides an illustrative example of the SNR and SFDR metrics. When the frequency-representation of the quantized sinusoidal signal is analyzed, a few major characteristics can be identified. The first is SNR.

Equivalently calculated using Equation 1, the SNR is also expressed as the relative intensities of the signal to its noise. Figure 2 shows an example of a signal's SNR. Similar in

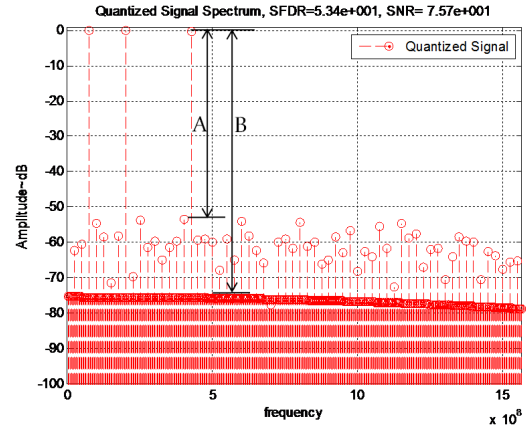


Fig. 2. A) SFDR. B) SNR for a three-tone test signal in a simulated converter.

nature to SNR, SINAD is the ratio of a signal's power to its distortion and noise power. It provides a means to quantify the severity of the distortion. A metric that is particularly useful in determining the amount of distortion within the signal is SFDR. SFDR is the ratio of the signal's intensity to the strongest non-signal frequency content. The effective number of bits (ENOB) of a converter expresses SINAD in a slightly different form. ENOB represents the amount of noise in the converter through an equivalent ideal converter resolution.

IV. LINEARIZATION METHODS

Current methods of in-package linearization, or calibration, vary from the simple to the complex. National Semiconductor's ADC083000 calibrates by trimming a 100 ohm analog resistor to reduce the offset error [11]. There has also been work in more advanced in-package calibration methods [6]. Despite these in-package methods, many methods of linearization occur out-of-package due to their complexity. Volterra-based methods [13], among others [1, 4], are computationally expensive and are inconvenient for on-chip implementation.

The use of reconfigurable devices, such as FPGAs, provide the opportunity to have larger signal metric improvements than industry-provided compensators but without the overwhelming hardware demands of PC-based compensation methods. Also, by using FPGAs, the compensation method is up to the user. Being reprogrammable, an FPGA can be used to implement many different kinds of compensators as long as it fits onto the device. One such method is the error table method. The error table method identifies the transfer function of the ADC, compares the actual transfer function to the ideal case, and stores the errors on a code-by-code basis [2]. One compensation method that is very well-suited for FPGA implementation is bit-extended error-tables (BEET) due to its relative simplicity, effectiveness, and portability onto an FPGA platform [8].

V. BEET COMPENSATION ANALYSIS AND SIMULATION

BEET compensation improves the quality of the information provided by the ADC through additive error correction. Unfortunately, basic error tables only compensate to the nearest

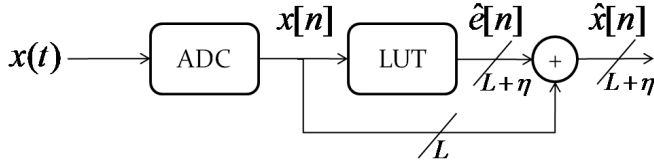


Fig. 3. Block Diagram of the BEET Compensation Process.

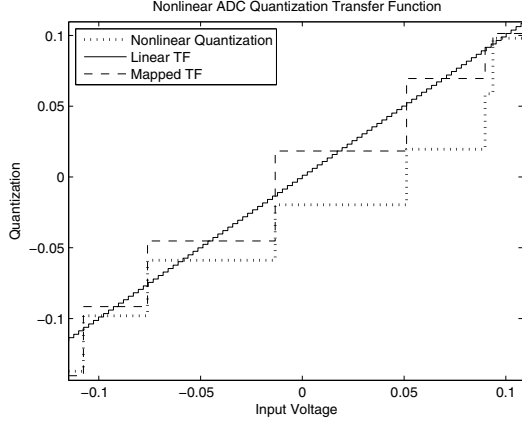


Fig. 4. Comparison of the Original L-bit Transfer Function, the Ideal L+eta Transfer Function, and the Compensated Transfer Function.

whole least-significant bit (LSB). In terms of voltage, a LSB is defined as[7]:

$$LSB = \frac{V_r}{2^L} \quad (4)$$

BEET compensation incorporates midpoint sub-bit error correction, which provides a more linear representation of the data. As a consequence, if L-bit data is extended by eta fractional bits, the resulting code will be L+eta bits long. The impact of an LSB, from Equation 4, is reduced by $\frac{1}{2^\eta}$ if the input voltage range (V_r) remains unchanged. The lengthened code still has the SNR characteristics of an L-bit converter and there is still only 2^L codes. The BEET process is shown in Figure 3.

With the number of quantization codes (N) equalling 2^L , the current quantization bin number being K , $y[n]$ being the quantized signal, $x[n]$ being the input signal, $\Delta_L y$ being the size of an L-bit converter's least significant bit, $\Delta_N L$ being the nonideal bin size, $\delta_{NL}[p]$ being the p^{th} bin width for the nonlinear transfer function, the minimum input voltage equalling V_{min} , and the static dynamic nonlinearity known as a vector ($DNL[m]$), the mathematical representation of an uncompensated ADC transfer function can be described as:

$$\sum_{p=-M}^K \delta_{NL}[p] - V_{min} \leq x[m] < \sum_{p=-M}^{K+1} \delta_{NL}[p] - V_{min}, \quad \forall K \in [-M_N, M_N - 1] \quad (5)$$

where,

$$M_N = \frac{2^L}{2}, \quad (6)$$

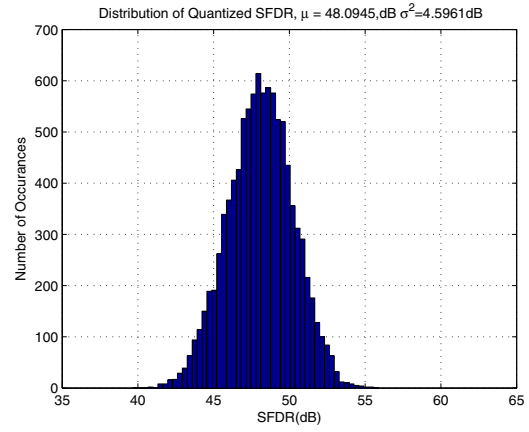


Fig. 5. SFDR of 10000 DNL=0.6 and INL=0.9 ADCs.

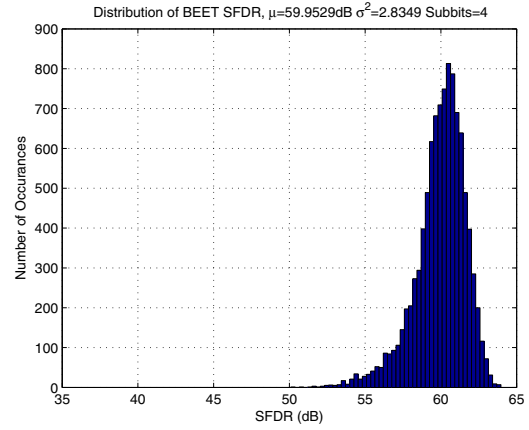


Fig. 6. SFDR of 10000 DNL=0.6 and INL=0.9 ADCs with eta=4 BEET Compensation.

and,

$$\delta_{NL}[m] = \Delta_x(1 + DNL[m]), \quad (7)$$

Note that this is for the traditional mid-riser stair-step transfer function, such as the one partially shown in Figure 1. Should a BEET compensator be applied to the ADC, a new transfer function would effectively be created. A BEET compensated ADC transfer function, with all variables consistent with the previous development and $\Delta_{L+\eta} y$ equalling the LSB of an L+eta converter, is described as:

$$y[m] = K \Delta_{L+\eta} y, \quad \sum_{p=-M}^K \delta_I[p] - V_{min} \leq \delta_{NL}[m] < \sum_{p=-M}^{K+1} \delta_I[p] - V_{min}, \quad \forall K \in [-M_\eta, M_\eta - 1] \quad (8)$$

where,

$$M_\eta = \lfloor \frac{2^{L+\eta}}{2} \rfloor, \quad (9)$$

and,

$$\sum_{p=-M}^m \delta_{NL}[p] \leq x[m] < \sum_{p=-M}^{m+1} \delta_{NL}[p] \quad (10)$$

TABLE I
RESULTS FOR DNL=0.2, INL=0.35. STATISTICS CALCULATED AS A
RESULT OF 10000 SIMULATIONS.

	SFDR (dB)		ENOB (LSB)		SINAD (dB)	
	μ	σ^2	μ	σ^2	μ	σ^2
Quant	55.192	4.709	7.295	0.0274	45.6806	0.9927
BEET 0	58.061	2.415	7.450	0.0072	46.617	0.2624
BEET 1	59.342	2.544	7.575	0.0094	47.366	0.3406
BEET 2	61.405	1.411	7.886	0.0046	49.238	0.1683
BEET 3	61.816	1.382	7.955	0.0044	49.654	0.1576
BEET 4	61.894	1.369	7.968	0.0043	49.734	0.1557

TABLE II
RESULTS FOR DNL=0.6, INL=0.9. STATISTICS CALCULATED AS A
RESULT OF 10000 SIMULATIONS.

	SFDR (dB)		ENOB (LSB)		SINAD (dB)	
	μ	σ^2	μ	σ^2	μ	σ^2
Quant	48.095	4.596	6.189	0.0666	39.021	2.4140
BEET 0	57.682	2.275	7.300	0.0129	45.709	0.4661
BEET 1	58.384	2.921	7.388	0.0181	46.242	0.6548
BEET 2	59.640	2.725	7.618	0.0224	47.625	0.8112
BEET 3	59.901	2.814	7.665	0.0236	47.907	0.8570
BEET 4	59.953	2.835	7.674	0.0238	47.962	0.8616

Essentially, the new transfer function is created by identifying the ideal location of the L-bit transfer function on the ideal $L+\eta$ transfer function. A straight-forward application of Equation 5 and Equation 8 can yield the transfer functions shown in Figure 4.

Notice that what BEET effectively accomplishes is a mapping of the original transfer function onto the ideal $L+\eta$ bit transfer function. Such a mapping improves the linearity of the ADC with a high-resolution midpoint correction. A special case of BEET is for when $\eta=0$, in which case it is a traditional error-table compensator.

VI. SIMULATION OF BEET CORRECTION

Using Equation 5 and Equation 8, various compensators can be simulated into ADCs. Using multiple random ADC transfer functions, the impact of η on the SFDR, SINAD, and ENOB are evaluated. Similar to industry specifications, the random transfer functions are produced with bounded Gaussian DNLs and INLs. For the purpose of this test, the maximum DNL and INL values are measured according to best-fit criterion. Thus, the maximum (DNL,INL) pairings for the simulations are: (0.2,0.35), (0.6,0.9), and (0.5, 1.0). A single sine wave at a frequency of 75 MHz is sampled at a rate of 3.125 GHz.

As shown in Table I, the mean and variance of the histograms show improvement as BEET's η parameter is increased. Notice the improvement in all three metrics for the small DNL and INL. The error table method improved the quantized signal's SFDR by 2.869dB, while BEET improves the SFDR by an additional 3.833dB. BEET also offers significant improvements in SINAD and ENOB. Notice that the SINAD and ENOB trend toward the ideal value of 50dB and 8 bits, respectively. If η is increased without bounds, the converter's SINAD and ENOB will not reach the ideal values because of the uneven quantization bins; however, they will significantly improve towards this value. Figure 5 provides the histogram distribution of the quantized signals' SFDR for

TABLE III
RESULTS FOR DNL=0.5, INL=1.0. STATISTICS CALCULATED AS A
RESULT OF 10000 SIMULATIONS.

	SFDR (dB)		ENOB (LSB)		SINAD (dB)	
	μ	σ^2	μ	σ^2	μ	σ^2
Quant	46.503	5.807	6.152	0.0555	38.800	2.0105
BEET 0	57.867	2.362	6.748	0.0109	42.386	0.3942
BEET 1	58.640	3.073	7.430	0.0185	46.496	0.6721
BEET 2	60.004	2.802	7.681	0.0230	48.003	0.8346
BEET 3	60.287	2.830	7.733	0.0240	48.316	0.8702
BEET 4	60.343	2.844	7.743	0.0241	48.377	0.8752

the (0.6,0.9) case. Figure 6 shows how a BEET compensator, using $\eta = 4$, improves the SFDR for the the identical set of (0.6,0.9) cases Figure 5 represents. The gaussian mean is improved by nearly 12dB, with a dramatic 1.7dB decrease in variance. These values can be seen in Table III in relation to other sub-bit values, ENOB, and SINAD. Note that a BEET compensator with zero additional bits is a traditional error table, and thus can be treated as a special case.

VII. CONCLUSIONS

In this paper, a fractional-bit ADC compensation technique has been discussed, modeled, and simulated. It is shown that the BEET method of error compensation yields more improvement for a converter's SFDR and SINAD than traditional error-table compensation. Yet, the BEET method is still as simplistic as traditional error tables. Reducing the data's LSB size and subsequently improving the accuracy of the uncompensated data benefit the SFDR, ENOB, and SINAD of the data.

REFERENCES

- [1] F. Adamo, F. Attivissimo, N. Giaquinto, and A. Trotta. A/D Converters Nonlinearity Measurement and Correction by Frequency Analysis and Dither. *IEEE Transactions on Instrumentation and Measurement*, 52(4):1200–1205, August 2003.
- [2] E. Balestrieri, P. Daponte, and S. Rapuano. A State of the Art on ADC Error Compensation Methods. *IEEE Transactions on Instrumentation and Measurement*, 54(4):1388–1394, August 2005.
- [3] P. Cruz, N. Carvalho, and K. Remley. Evaluation of Nonlinear Distortion in ADCs Using Multisines. In *IEEE MTT-S Int. Microwave Symp. Dig.*, pages 1433–1436, 2008.
- [4] P. Handel and M. Skoglund. A Calibration Scheme for Imperfect Quantizers. *IEEE Transactions on Instrumentation and Measurement*, 49:1063–1068, October 2000.
- [5] IEEE. IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters. December 2000.
- [6] H. Liu, Z. Lee, and J. Wu. A 15-b 40-MS/s CMOS Pipelined Analog-to-Digital Converter with Digital Background Calibration. *IEEE Journal of Solid-State Circuits*, 40(5):1047–1056, May 2005.
- [7] S. Lloyd. Least Squares Quantization in PCM. *IEEE Transactions on Information Theory*, 28(2):129–137, March 1982.
- [8] H. Lundin. *Characterization and Correction of Analog-to-Digital Converters*. Doctoral Thesis. Royal Inst. Technology, Stockholm, Sweden, 2003.
- [9] F. Maloberti. *Data Converters*. Springer Press, Dordrecht, Netherlands, 2008.
- [10] B. Provost and E. Sinencio. A Practical Self-Calibration Scheme Implementation for Pipeline ADC. *IEEE Transactions on Instrumentation and Measurement*, 53(2):448–456, April 2004.
- [11] National Semiconductor. ADC083000: 8-Bit, 3 GSPS, High Performance, Low Power A/D Converter. July 2009.
- [12] E. Soenen and R. Geiger. An Architecture and an Algorithm for Fully Digital Correction of Monolithic Pipelined ADC's. *IEEE Transactions on Circuits and Systems*, 42(3):143–153, March 1995.
- [13] J. Tsimbinos. *Identification and Compensation of Nonlinear Distortion*. Doctoral Thesis. University of South Australia, Adelaide, Australia, 1995.