

A Dual-port DRAM Component for a Digital RF Memory

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Abstract

This paper describes the design and testing of a dual-port dynamic memory component for a Digital Radio Frequency Memory (DRFM). The use of dynamic memory allows for greater storage capacity than the static memory currently used. In addition, the dual-port nature of the memory allows for access by an external processor. The external processor may be used for signal processing applications such as parameter extraction.

Several memory cell implementations were evaluated, and the three-transistor memory cell was selected. The cell was then modified for dual-port operation. Supporting circuitry such as address decoders and sense amplifiers were also designed. The component was simulated using both a high-level language (VHDL) and circuit descriptions (SPICE). Then, a 32-word by 8-bit memory was fabricated and tested to ensure the validity of the design. Finally, the dynamic memory was used to replace the static memory currently in use.

Introduction

A digital radio frequency memory (DRFM) is an electronic device used in signal acquisition and processing systems to record and process radio frequency (RF) samples in real time [1]. Modern electronic countermeasure (ECM) systems use DRFMs to sample a radar signal sent by an enemy transmitter, inject a time delay and a frequency shift into the sampled signal, and return a false signal to the enemy receiver. By delaying and retransmitting a radar signal that has its frequency shifted, an aircraft can deceive a hostile radar system into tracking a false target or present a large number of false targets to a radar operator [2].

The VLSI DRFM designed by Kranz [3] is limited in the amount of data it can store. It uses a memory array designed with static random access memory (SRAM) cells. Since SRAM cells are relatively large, the VLSI DRFM is

capable of storing only 1K of 6-bit words. In addition, the VLSI DRFM uses a quasi-dual-port architecture. Data is written into a read from the DRFM on separate ports. With this architecture, an external digital signal processor cannot be connected to the DRFM to provide processing of data stored in memory.

The goal of this effort was two-fold: (1) to investigate the feasibility of using a dynamic random access memory (DRAM) array for the DRFM, and (2) to design a true dual-port VLSI DRAM DRFM [4]. The memory array, consisting of DRAM cells, will be used to increase the amount of data the DRFM can store. In addition, the DRFM will be designed with a dual-port architecture that will permit data to be written into and read from memory through a single port. The dual-port architecture will also provide a processor interface which will allow a computer to be connected to the DRFM.

Memory Design

Evaluation of Memory Cells for DRFM Use

A DRFM implemented using DRAM offers several potential advantages. First is the increase in memory storage capability. Another is the decrease in power requirements. A potential disadvantage is the possible need for additional circuitry that will provide periodic refresh. However, since data will be written into and read from each memory location in the DRFM, periodic refresh may not be necessary if the time between the write cycle and the read cycle is short compared with the rate of charge loss due to leakage current.

For this effort, the three-transistor DRAM cell was modified as shown in Figure 1 to provide a dual-port capability. The three-transistor configuration was selected because read operations do not destroy the data stored in memory. By preserving the data after a read, it will not need to be reconstructed by an external digital signal processor in the event the processor is used just to

monitor the stored data.

Operation of the Memory Cell

The write and read operations complement the data input from a port and output from the memory cell, respectively. For this particular design, both read and write operations require the BIT lines to be precharged.

To write data from port 1 to the cell, the port 1 BIT line is first precharged. The complement of the data is then driven onto the port 1 BIT line. The write pass transistor for port 1 (M1) is turned on by asserting the WRITE line. The gate of the storage transistor (M5) charges or discharges depending on whether a 1 or a 0 is to be stored in the cell. The same procedure is followed to write data from port 2 to the cell. However, the port 2 BIT line is driven with the complement of the data to be stored and M2 is turned on by asserting the port 2 WRITE line.

To output data to port 1, the port 1 BIT line is again precharged. The read pass transistor for port 2 (M2) is turned on by asserting the READ line. If a 1 is stored in the cell, M5 will already be on. The BIT line discharges through M2 and M5 and a 0 is read out through port 1. If a 0 is stored in the cell, M5 is turned off and the BIT line cannot discharge. A 1 is read out through port 1. Port 2 reads stored data in a similar manner using M4 to set the BIT line to the value which will be read out. Recall that during the write operation, the complement of the input data is stored in the cell. Thus, when a read operation puts the complement of the stored data on the BIT line, the original data is output to the port.

Design of an External Interface

An interface is necessary to connect an external processor to the DRFM. The external interface takes care of precharging the BIT lines during the read and write cycles, driving the complement of the data to be stored onto the BIT lines, sensing the values stored in memory, and outputting the appropriate values to the ports. Besides connecting an external processor to the DRFM, the external interface also connects the input ADC and the DSSM to the memory array.

The precharge and drive circuitry from a simple external interface were incorporated into a single external interface cell with a modified single-stage differential amplifier. Figure 2 is a schematic of the dual-port sense amplifier designed for the DRFM.

The components for a dual-port dynamic memory for the DRFM were designed. Two memory designs were considered for the VLSI DRAM DRFM: (1) a dual-port memory which uses a NOR address decoder and address driver, and (2) a dual-port memory which uses a NAND address decoder and driver. Both memory designs were simulated as a 1-word by 2-bit memory slice and as a 128-word memory. Results of the simulations indicate that a dual-port memory designed with the NAND address decoder and driver will operate as fast as but dissipate less power compared with one designed with NOR circuitry. Based on these simulation results, a VLSI DRFM DRAM will be designed and laid out using a NAND address decoder and driver.

DRFM Integration

The layouts for the dual-port memory cell, the NAND address decoder and driver, and the external interface were integrated into a 2k-word by 8-bit dual-port memory for the VLSI DRAM DRFM. In addition to these components, a column address decoder using a NAND configuration was designed for the dual-port memory. The layout of the dual-port memory is shown in Figure 3.

The dual-port memory is composed of 16 banks of 128-word by 8-bit memory arrays. Each memory array occupies an area of $4608\ \mu\text{m}$ by $6412\ \mu\text{m}$. One 8-bit external interface is required for each memory array bank. A row address decoder is required for each port of the dual-port memory. A row address driver is required for each row address decoder. A column address decoder is required for each port of the dual-port memory.

In order to realize the benefits of a true dual-port architecture, the VLSI DRAM DRFM was designed to use port 1 to sequentially write captured digitized samples to each memory address and, after a specified delay, output the data to the DSSM. This permitted the use of port 2 for digital signal processing purposes such as data monitoring or data modification. A write address incrementer and a read address incrementer control where port 1 data is written to and read from, respectively.

The write address and read address incrementers were designed with each using 11 counter stages consisting of a pair of flip-flops in a master-slave configuration. An HSPICE simulation was performed on both counter cell layouts. Details are available in [4].

A 2K-word by 8-bit dual-port memory component was designed using the memory cell, NAND row address

decoder and driver, and external interface previously described. A NAND column address decoder was also designed for the memory component to supply the bank-select signals for ports 1 and 2. Next, the design and layout of the port 1 WRITE and READ address incrementers was described. An HSPICE simulation of the WRITE and READ counter cells which make up the address incrementers was performed. Then, a VHDL model of the VLSI DRAM DRFM was created. Behavioral descriptions of the subcomponents which make up the memory component and the control unit were written and used to structurally describe the VLSI DRAM DRFM. A test bench and configuration file was written and used to exercise the model. A simulation of the model indicates that problems still exist with the descriptions of the incrementer and controller subcomponents. After the VHDL had been written, the VLSI DRAM DRFM was laid out in silicon. The layout is not complete since a controller and DSSM must be added prior to fabrication of the VLSI DRAM DRFM chip. Finally, the modes of operation of the VLSI DRFM DRAM chip were described.

Summary

As currently laid out, the 2K-word by 8-bit memory component requires a cycle time of approximately 80 ns. This is equivalent to a speed of operation of about 12.5 MHz. The availability of only 7.9 mm by 9.6 mm of chip area limits the amount of dynamic memory that can be used to 2K 8-bit words. Modifications that are necessary to increase the speed of operation would decrease the amount of available memory even further. For this design, the NAND address drivers and decoders were as fast as the NOR address drivers and decoders, but used less power. The dual-port memory designed permits data to be written into and read from memory through a single port. This gives the DRFM the capability to be interfaced with an external digital signal processor.

Acknowledgements

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References

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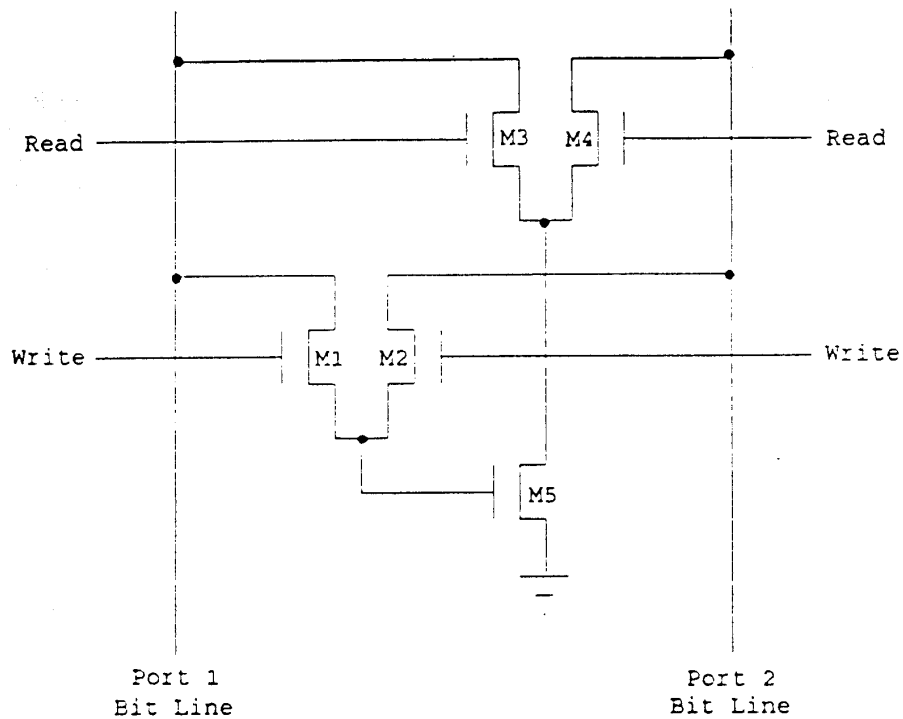


Figure 1. A dual-port DRAM cell for the DRFM.

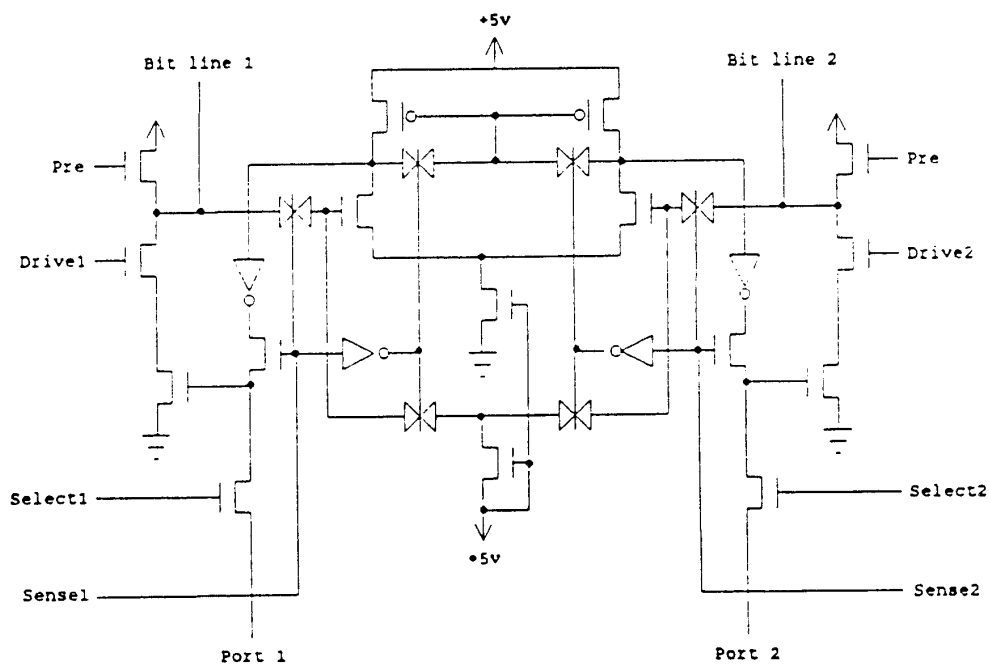


Figure 2. A dual-port external interface cell.

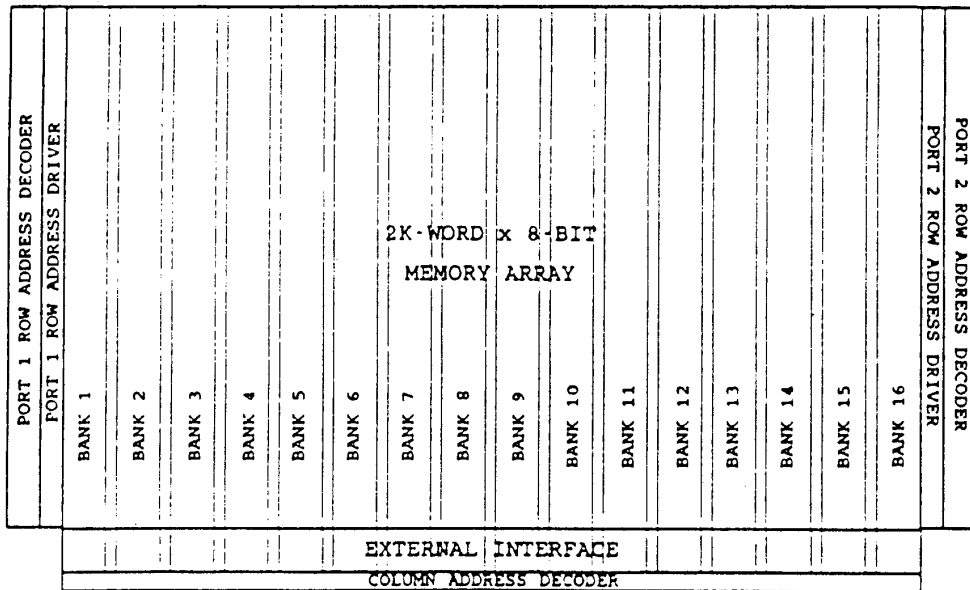


Figure 3. Architecture of a 2k-word by 8-bit dual-port memory