Analysis By Simulation of a Spread Spectrum Intercept Receiver

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Abstract

The purpose of this paper is to evaluate by simulation the performance of a spread spectrum intercept receiver. The Modulation Detection and Classification (MODAC) receiver [1] detects and classifies spread spectrum signals for which the center frequency and other modulation parameters are not known. The MODAC was modeled and simulated using the Block Oriented System Simulator (BOSS)[2]. Simulations were run to test the detection capabilities under varying conditions of noise, narrowband interferers, and internal system parameters.

The MODAC direct sequence stage was found capable of detecting a DS spread spectrum signal up to the point where a narrowband interferer was 14 dB higher in power than the spread spectrum signal. The MODAC frequency hopping stage dependence on the second chip rate detector delay also was in agreement with the analytical expression. The simulation also showed that the MODAC FH stage was more susceptible to narrowband interferers than the DS stage and could not detect a FH spread spectrum signal when the narrowband interferer power was less than 6 dB below the spread spectrum signal.

Introduction

The MODAC is basically a cascade of two chip rate detectors with a narrowband interference reference system. One advantage of the MODAC over other receivers utilizing chip rate detectors is this narrowband interference system, which estimates the background noise and spurious products the chip rate detector may produce. This allows the MODAC to detect spread-spectrum signals with a much lower false alarm rate.

Figure 1 shows a fundamental two-stage MODAC receiver configuration. The first stage detects constant envelope discrete phase modulated signals (phase shift keyed, direct sequence signals), and the second stage detects frequency hop signals. The chip rate detector output signal-to-noise ratio (SNR_o) is given in Reference [3] as:

$$SNR_o = \frac{S^2 W_{in} sin^2[\pi(1 - f_c\tau)]}{N^2\pi^2 W_o(1 - \frac{f_c}{W_{in}} + \frac{2S+I}{N} + \frac{S^2 W_{in}}{N\pi^2 f_c^2})} \qquad (1)$$

where:

SNR_o	-	Output SNR in detecting one chip line sideband
S	-	Input signal power
N	-	Input noise power in bandwidth W_{in}
W_{in}	-	Input noise bandwidth
W_o	-	Output bandwidth of chip detector bandpass filter
f_c	-	Chipping rate of input signal
τ	-	Delay in chip detector
I	-	Narrowband interferer power

This expression shows that the output SNR is maximized when the delay in the chip detector, τ, is one-half a chip period (i.e. $\tau = 1/2f_c$). For any other value of τ the output SNR is degraded.

The chip rate detector has one serious drawback – narrowband interfering signals at the chip detector input degrade its performance. The MODAC receiver's solution to the narrowband interference problem is to add a noise reference channel. The noise reference channel will not eliminate thermal noise, rather it identifies environmental interference and prevents this interference from causing false alarms. Signal detection is accomplished by subtracting the noise channel from the signal channel. A detection is made if the signal channel is greater than the noise channel by some specified threshold.

The noise reference channel consists of another chip rate detector with zero delay. This chip rate detector effectively squares the signal which produces the same second order product terms as in the primary path, since the delay of one-half of a chip period in the primary path is usually too small to affect narrowband interferers [3]. Narrowband interferers will therefore produce the same spurious components in the noise reference channel as in the chip rate detector. Thus, the comparison between the chip rate detector output and the noise reference output will distinguish between chip lines and all other interference.

As shown in Figure 1, another chip rate detector and noise reference channel can be added to detect frequency hop signals. With a FH signal input, the output of the first chip rate detector is periodic and represents a random PSK signal. This PSK signal is a function of the frequency hop rate and the chip detector delay, τ, and can be detected by the second chip rate detector. If the frequency hop rate is less than 50 kHz, then the information spectrum of the PSK signal from the first stage would be in a 50 kHz lowpass bandwidth.

Simulation Models

The MODAC simulation model requires a chip rate detector and a noise reference channel. In the BOSS simulation, these were combined into one module as shown in Figure 2. This module was used for preliminary testing of the chip rate detector concept and then incorporated into the MODAC model.

The MODAC DS stage model is shown in Figure 3. This simulation model contains the CHIP RATE DETECTOR module, CMPLX TONE modules for the down conversion of the signal, and BUTTERWORTH LOWPASS filter modules for the output filtering. With the MODAC DS Stage model constructed, it was necessary to build a test system to use for the simulations. This system was called *MODAC DS TEST SYSTEM* and allows additive white Gaussian noise and narrowband jammers to be added to the input signal.

The MODAC FH model is shown in Figure 4. The MULTI STAGE DELAY, CMPLX CONJG, and MULTIPLIER modules comprise a chip rate detector. The two outputs are then lowpass filtered. Only the real part of the signal is needed at the output because of the delay conjugate multiply operation. The test system built for module MODAC FH STAGE is similar to the test system for the MODAC DS STAGE module. This system was called MODAC FH TEST SYSTEM and allows additive white Gaussian noise and narrowband jammers to be added to the input signal.

MODAC DS Stage Simulation Test Results

The data results presented show the performance change or degradation of the MODAC due to non-optimum chip rate detector delay, the presence of high-level tone jammers, and different signal processing techniques.

The results of three different types of tests will be given. These tests were: 1) varying SNR_i, 2) varying the chip rate detector delay, and 3) varying the power of a single tone jammer. For each test only a single parameter was varied while all other parameters were held constant. Also, all of the output data for these three tests were processed by the chip frequency routine described in Reference [4]. These results will also be given.

The input signal-to-noise ratio, SNR_i, is the ratio of the input signal power to the input noise power. However, the output signal-to-noise ratio, SNR_o, provided here is measured from the output chip line to the next highest magnitude point on the frequency domain plot. Even though this is not the true output signal-to-noise ratio, it does provide a useful measure of the signal available for classification.

The output signal-to-interference ratio, SIR_o, is measured in the same way as SNR_o. This parameter is used when a cw jammer is present. The input signal-to-interference ratio, SIR_i, is measured as the ratio of the input signal power to the input tone jammer power.

a) SNR Tests

Recalling Equation (1), the output SNR for a chip rate detector should have a second order dependence on SNR_o. Figure 5 is a plot of the SNR_o for the Sum of Magnitudes, (SOM), with the second order dependence also plotted. As can be seen, the SOM output has a second order dependence on input SNR.

The MODAC model has the same second order dependence on the input SNR as the chip rate detector. Now that this second order dependence has been validated, the MODAC's dependence on the chip rate detector delay will be examined.

b) Chip Rate Detector Delay Tests

A chip rate detector has a $SIN^2[\pi(1 - f_c\tau)]$ dependence on the chip rate detector delay, τ, as given by Equation 1. SNR_o is maximized for $\tau = 1/f_c$, and degraded for other values of τ. Figure 6 is a plot of normalized SNR_o for SOM, with both sidebands, plotted against the chip rate detector delay, chip frequency product. The theoretical value is also plotted. As can be seen, the output SNR for SOM follows the analytical value very closely.

The MODAC has four chip rate detector delay lines: 15 ns, 40 ns, 100 ns, and 250 ns. These delay lines would be optimum for chip rates of 33.33 MHz, 12.5 MHz, 5 MHz, and 2 MHz respectively. Using the results shown in Figure 6 together with these delay lines, the MODAC can cover the frequency range of 1 MHz to 50 MHz with a maximum 3 dB degradation of SNR_o due to non- optimum chip rate detector delay. The detection of any chip rate outside of this range will be degraded further by non- optimum delay line length.

c)Jammer Tests

These tests were run to determine the effect of a cw jammer on the output SNR. The cw jammer was set to a frequency which would be in the 2 KHz bandwidth of the lower sideband. These tests were run for SNR_i of 0 dB and 10 dB.

Figure 7 is a plot of SIR_o for the SOM case comparing the results for SNR_i equal to 0 dB and 10 dB. This plot shows that for a larger SNR_i , the output SIR is greater for the same input SIR. For this case where SNR_i is increased by 10 dB, SIR_o is increased by about 2 dB. This is not a significant increase, but it is an improvement nonetheless.

d) Chip Frequency Algorithm Evaluation

The final evaluation of the MODAC DS stage involved a phase interpolation FFT algorithm to accurately compute the chip frequency [4]. This algorithm is needed because the 1024 point FFT of the MODAC has a frequency resolution of 4.8828 Hz. Therefore, the detected chip frequency could have an error of up to $\pm$ 2.4414 Hz. This algorithm is intended to give a much more accurate frequency value of a detected chip line.

When a detection is made, this algorithm takes the 1024 time domain data points from the MODAC DS stage and separates them into two sets of 512 data points. Two 512 point FFT's are then computed. The difference in phase between the detected signals chip frequency points in the two FFT's is then used to calculate the chip frequency.

The data from the MODAC DS stage simulation was input to this algorithm. For the cases where the MODAC would have detected a spread spectrum signal (i.e., where the chip line was greater than the noise or any narrowband interferer), the maximum error was 0.71344 Hz and the minimum error was 0.00146 Hz. The error increased with a decreasing input SNR. This algorithm does give much more accurate results than a conventional FFT.

MODAC FH Stage Simulation Test Results

The tests run to evaluate the MODAC FH stage were similar to the tests used to evaluate the MODAC DS stage: 1) varying SNR , 2) varying the chip rate detector delays, and 3) varying the power of a cw jammer. One difference is that the MODAC FH stage has two chip rate detector delays: the delay in the DS stage and a second delay in the FH stage chip rate detector. The effect of varying these two delays and their interrelationship was evaluated. Another difference from the DS stage testing is that the FH stage only looks at one sideband, instead of two as in the DS stage. This reduces the amount of output data to be evaluated.

a) SNR Tests

Figure 8 shows the results of varying the input SNR. The output SNR is fairly constant for input SNR's greater than 0 dB, but SNR_o decreases very rapidly for input SNR's less than 0 dB. These results show that the FH stage will not detect a spread spectrum signal with as low a SNR as the DS stage.

b) Chip Rate Detector Delay Tests

As stated previously, the detection of FH signals involves setting two delays in the MODAC. The first delay, τ_1 , is the delay in the DS stage. This first delay should be adjusted so that it is half the inverse hopping bandwidth of the signal [3]. The first series of chip rate detector delay tests involved varying τ_1 from the optimum value.

Figure 9 is a plot of the results of the chip rate detector delay 1 tests. As can be seen, the FH stage is relatively insensitive to this parameter. Changing the delay from 0 to 10 seconds changed the output SNR by only 2.5 dB. The optimum value for the hop frequency was $7.14x10^{-6}$ sec. So a large change in τ_1 changed the output SNR very little.

The second delay, τ_2, is in the FH stage. This delay should be set to one-half the hop period [3]. The second series of chip rate detector delay tests varied τ_2 from the optimum value. Figure 10 shows the effect of varying τ. This effect should be similar to that of the DS stage chip rate detector delay tests – i.e. a sin^2 dependence. Except for some small deviations, the results follow this sin^2 dependence. Although the MODAC output is relatively insensitive to the first chip rate detector delay, the output does depend very much on the second chip rate detector delay. The adjustment of this delay in the frequency hop mode will be very critical.

c) Jammer Tests

The final test for the MODAC FH stage involved a narrowband interferer. A cw jammer was set to a frequency which would coincide with the 4 KHz detection window of the FH stage. The amplitude of this jammer was then increased to evaluate its effect on FH detection. The input SNR for these tests was held at 40 dB. The results are shown in Figure 11. As can be seen, the jammer power needed to prevent FH signal detection was small when compared to the jammer power needed to prevent DS signal detection as given in Figure 7. The noise reference channel for frequency hop detection was not as effective as for direct spread signal detection.

Conclusions

The primary objective here is to evaluate, via simulation, the performance characteristics of the MODAC spread spectrum receiver. This involved constructing a simulation model of the MODAC using the Block Oriented Systems Simulator (BOSS). This model was then used to determine the spread spectrum detection characteristics of the MODAC in the presence of noise and narrowband interferers. MODAC system parameters were also varied to determine their effect on performance.

The simulation results indicate that the MODAC DS stage's dependence on the chip rate detector delay is indeed $sin^2[\pi(1 - f_c\tau)]$ as given by Equation (1). The MODAC was verified to cover the frequency range 1 - 50MHz with only a 3dB maximum degradation due to non-optimum chip rate detector delay. More delay lines would be needed only if the chip frequency range of interest increased.

For the MODAC DS stage, comparing the results of both sidebands for a signal detection worked better than combining the results into one and then checking for a detection. This was especially true when the input SNR was very small or a high-level narrowband interferer was present. Comparing both sidebands decreases the probability of detection, but also decreases the false alarm rate.

These simulation results showed that the phase interpolation FFT algorithm described in Reference [4] worked extremely well. The accuracy was much better than conventional FFT results, even for low output signal-to-noise ratios. This algorithm will enhance the ability of the MODAC to determine a detected spread spectrum signal's chip frequency.

The MODAC FH stage does not work as well as the DS stage for low input SNRs and in the presence of narrowband interferers. This greatly restricts the ability of the MODAC to detect frequency hop signals.

The simulation results indicated that the detection of FH signals is relatively insensitive to changes in the chip rate detector delay in the DS stage. The FH stage has the same dependence on the second chip rate detector delay as the DS stage has on its delay. Because of this, the selection of the second chip rate detector delay is not as critical as expected.

References

1. Ready, Patrick J. and Douglas R. Anderson. Modulation Detector and Classifier, United States Patent 4597107, (24 June 1986).

2. Shanmugan, K.S. "An Update on Software Packages for Simulation of Communication Systems," IEEE Journal on Selected Areas in Communications, vol. 6, no. 1, Jan 1988.

3. Modulation Detector and Classifier (MODAC) Final Report (Draft), April 1987. Contract F33615-85-C-1742. Fort Wayne IN: ITT Aerospace/Optical Division.

4. Spaulding, Edgar III Implementation of Phase Interpolation (PIE) Algorithm for Detecting a Single Tone in Noise. MS Thesis, AFIT/GE/ENG/88D-47. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson AFB, OH December 1988.

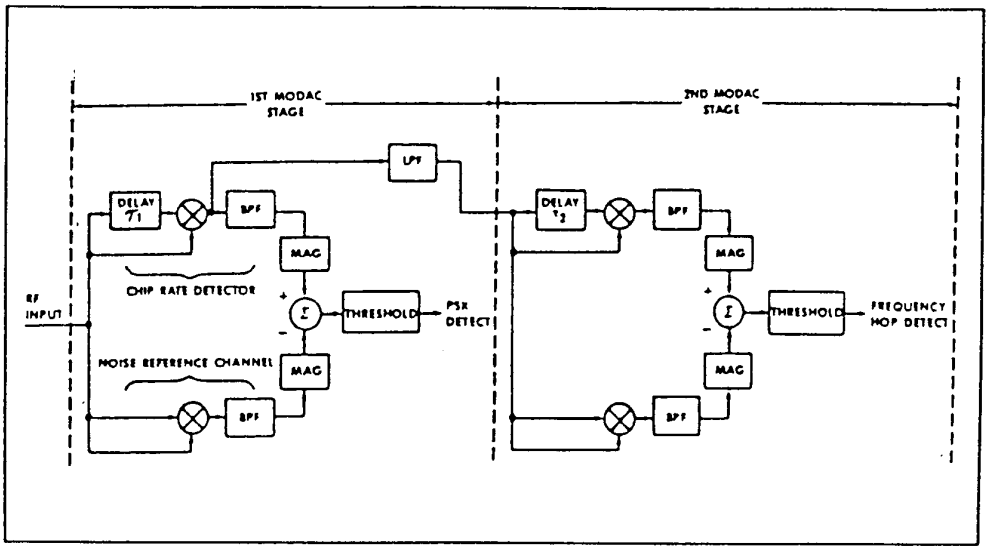

Figure 1. Two-stage MODAC Receiver Configuration (Simplified Diagram)

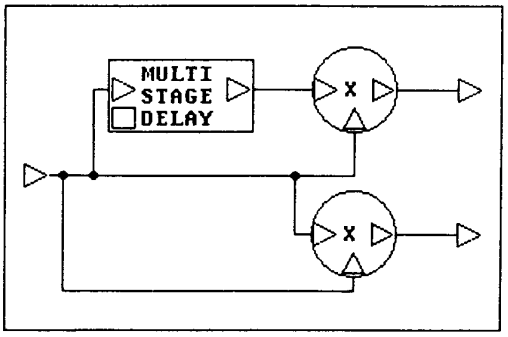

Figure 2. CHIP RATE DETECTOR Module

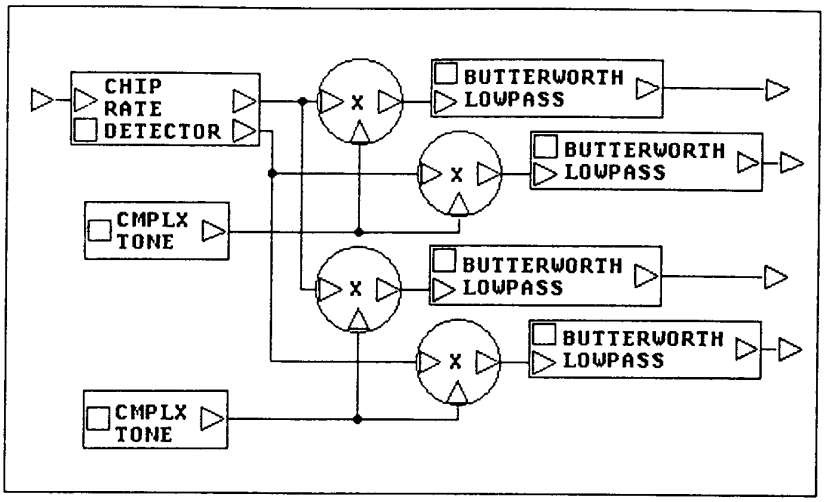

Figure 3. MODAC DS Stage Model

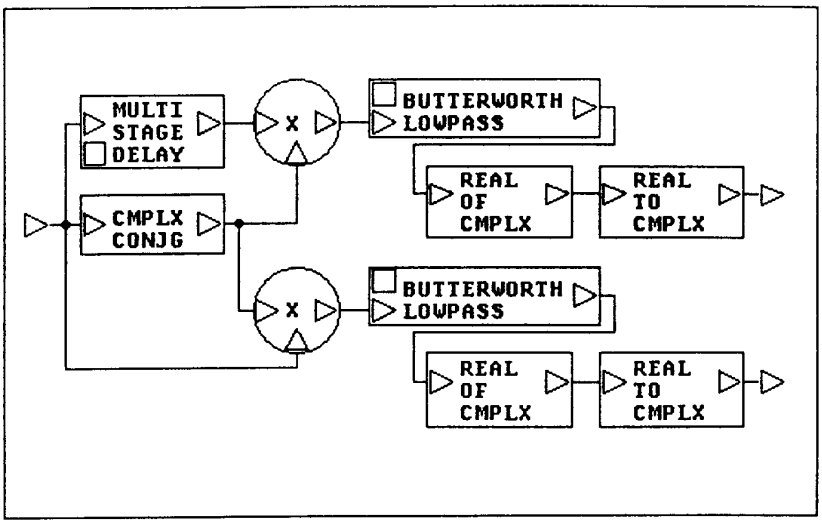

Figure 4. MODAC FH STAGE Module

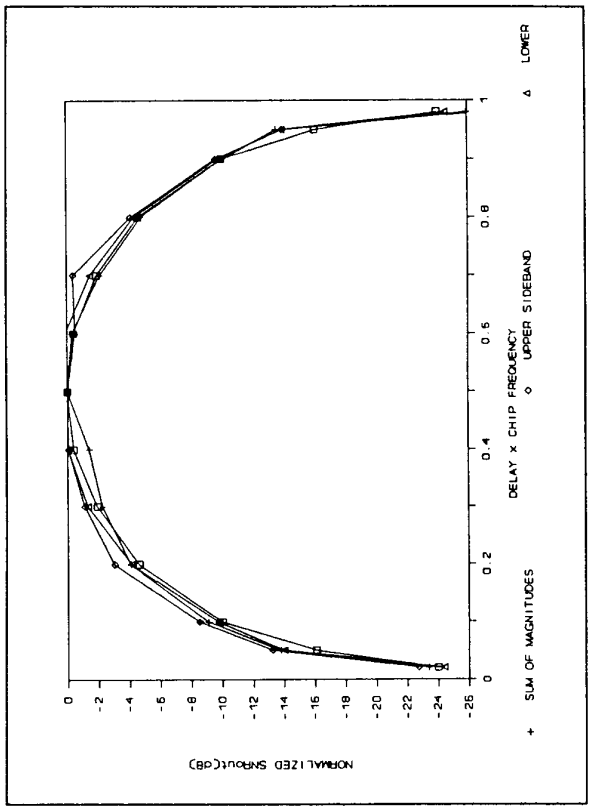

Figure 6. CRD Delay Test Results

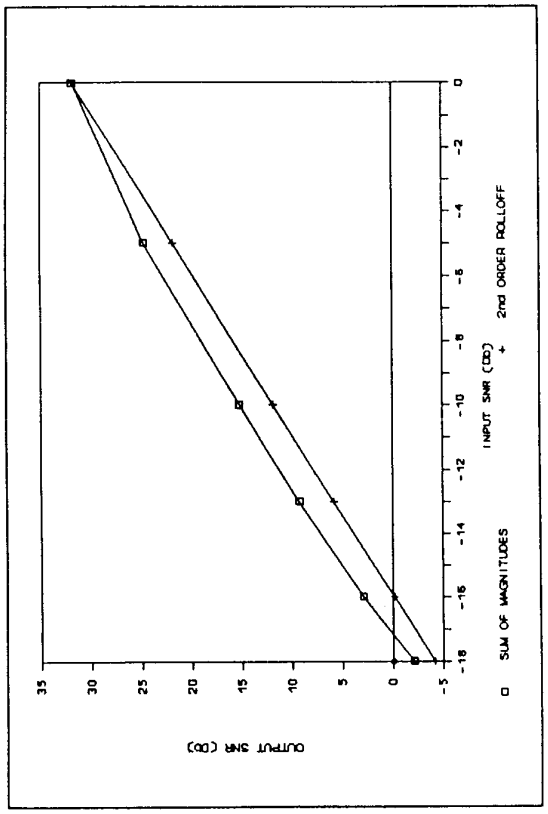

Figure 5. SNR Test MOS Results

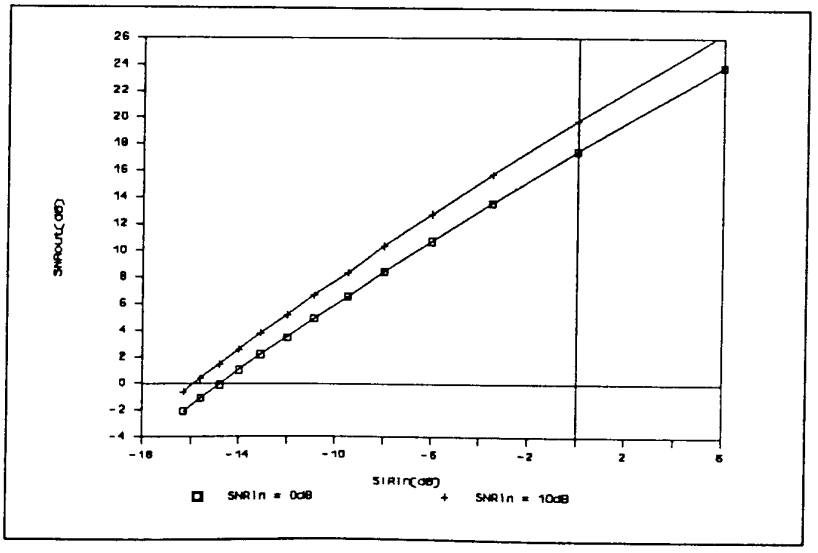

Figure 7. Jammer Tests 0dB SNR_i vs 10dB SNR_i Results

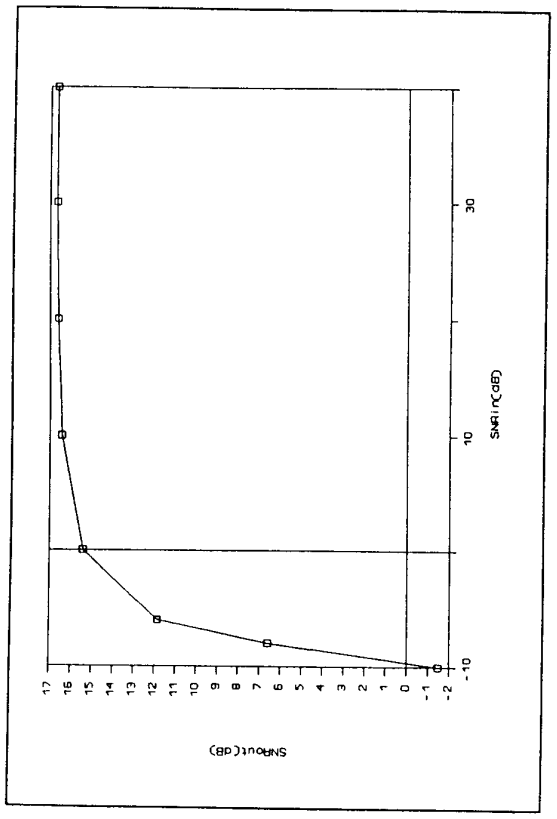

Figure 8. FH Stage SNR Test Results

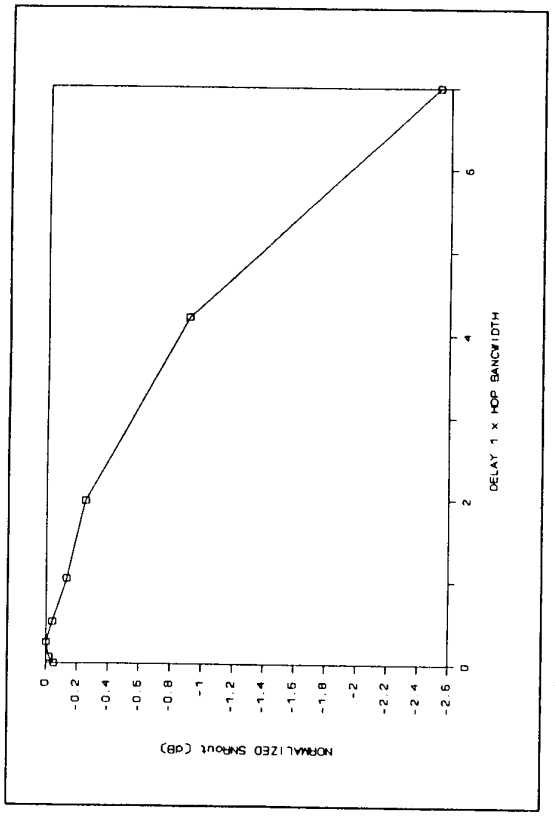

Figure 9. FH Stage CRD Delay 1 Test Results

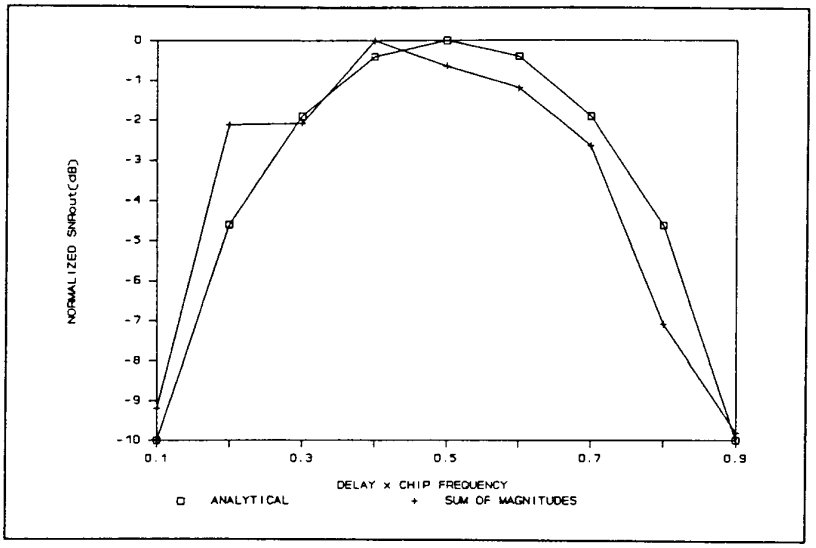

Figure 10. FH Stage CRD Delay 2 Test Results

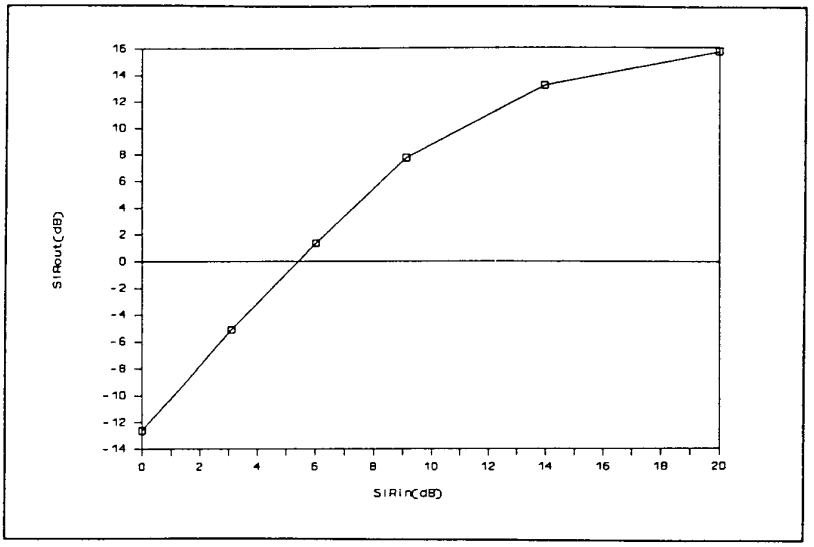

Figure 11. FH Stage Jammer Test Results