Novel 4-Way Combiner for Ka-Band AlGaN/GaN Power MMIC

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***Abstract* — A Ka-band GaN MMIC power amplifier (PA) with a novel 4-way combiner/divider is presented. The on-chip balanced 4-way combiner results in improved input and output return loss, and increased bandwidth. The 32 – 38 GHz two-stage PA produces a maximum power of 6 watts under class-A operation. This is the first report of this novel compact, combiner concept.**

***Index Terms* — power combiner, power splitter, GaN MMIC.**

I. Introduction

The high output power, and high data rates required for communications, electronic warfare and radar applications continue to push the operating frequencies towards the millimeter-wave (mmW) regime to satisfy various commercial and defense systems [1], [2]. The availability of high-power, high-efficiency, linear amplifiers at these frequencies is important for the successful deployment of systems, especially for communication. Traditional traveling-wave-tube amplifiers (TWTAs) [3] are being replaced with wide-bandgap semiconductor devices. GaN on SiC high-electron mobility transistors (HEMTs), and monolithic microwave/millimeter-wave integrated circuits (MMICs) have been demonstrated at mmW frequencies with power densities much higher than those from existing GaAs, or InP technologies [4]. The GaN on SiC technology has showed continuous improvements in output power, efficiency, bandwidth, and reliability [5].

The use of GaN technology at mmW frequencies has witnessed a significant increase in the past few years starting from devices with record power densities, to high-performance MMICs with excellent bandwidth (1–50 GHz [6], and 2–20 GHz [7]), high power [5], and high levels of integration [8].

One of the challenges in PA design is achieving good input and output return loss. In fact, in most cases the optimum power match results in poor output return loss. To meet the return loss requirements, an isolator is often inserted after the PA. This introduces additional losses, cost, and size. A common technique that combines two amplifiers and produces good input/output return loss is the balanced configuration, shown in Fig. 1.

This paper presents a Ka-band MMIC PA with a novel balanced 4-way combiner/divider. The MMIC combines four two-stage PAs using a novel, compact 4-way combiner design. Improvements in bandwidth and input/output return loss have been achieved. It is shown that linearity improvements can be achieved through a biasing scheme for the first and second stages of the amplifier, resulting in a higher 3rd order intercept point than the conventional biases.

II. MMIC Design

Achieving maximum output power from a transistor requires a certain optimum output impedance which, in most cases, is different from the conjugate match condition. This results in poor output return loss. The conventional, balanced amplifier configuration relies on combining two identical amplifiers with a 90° phase shift introduced at the input/output of one of the amplifiers, see Fig. 1.

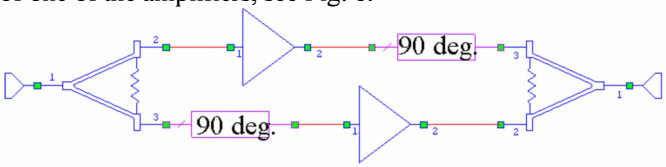

Fig. 1. Balanced amplifier configuration.

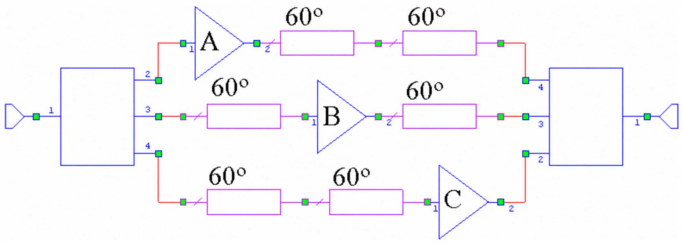

Fig. 2. Three way balanced amplifier.

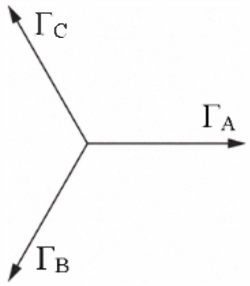

Fig. 3. Vector diagram of relfection coefficiencts from three way balanced amplifier.

The input reflection coefficient Γ_{top} from the top amplifier will have a phase θ, say, while the bottom amplifier's Γ_{bottom} will have a phase of θ + 180°. Hence, the reflection will cancel, resulting in excellent input return loss. The same design approach is also applied at the output with the 180° phase shift in different signal path to achieve equal phase (total path lengths) for all paths. This paper proposes

extending this concept to combining three amplifiers (as shown in Fig. 2), four amplifiers, or N amplifiers. In Fig. 2, at the input of the circuit, we will have Γ_A, Γ_B, Γ_C. If the three amplifiers are identical, then $\Gamma_B = \Gamma_A \angle -120°$, and $\Gamma_C = \Gamma_A \angle -240°$, see Fig. 3. Again, the reflections will cancel. The 1-to-3 splitter at the input can be implemented using various kinds of splitters (e.g. 1-to-3 Wilkinson divider). A simpler divider would be to have 3 parallel λ/4 transmission lines, each with characteristic impedance equal to $\sqrt{(150 \cdot 50)}$. Each transmission lines will match the amplifier's 50 ohm impedance to 150 ohm. The three parallel 150 ohm lines will result in a 50-ohm impedance at the input. In the present case, this concept was implemented to combine four parallel amplifiers with 0°, 45°, 90°, and 135° phase shifts at the input (and output), see Fig. 4. In general, to combine N amplifiers in parallel and achieve good return loss, one should introduce N phase shift lines with $0 \cdot (180°/N)$, $1 \cdot (180°/N)$, $2 \cdot (180°/N)$, $3 \cdot (180°/N)$,…, $(N-1) \cdot (180°/N)$. One of the attractive features of this balanced combining approach is that the additional phase shift lines enable the physical separation of the parallel amplifiers. For example, in the current case, Fig. 4, the top amplifier's physical separation (e.g. at input) necessitates the addition of a transmission line to reach it. However, under normal circumstances, this is not allowed as it will increase the path length (hence, the phase) of the top amplifier, and break the equal phase requirement across different paths. Even if the designer decides to add the extra transmission line length to all the amplifiers (to maintain phase balance), then the designer will be challenged to fit the extra length for the bottom amplifiers (especially for the second one from the bottom). These physical layout constraints are serious, and often disqualify theoretically attractive solutions.

For a PA with linear operation requirement, improvement in linearity can be achieved with the following bias technique, the *balanced*-AB class of operation. The idea is that the linearity of a single stage amplifier is improved by biasing the HEMT in deep class AB such that the gain expansion is balanced by the gain compression resulting in reduced AM-AM compression. The same approach is extended, here to a two-stage GaN/SiC amplifier. In the two-stage amplifier, the first stage is biased in class AB resulting in gain expansion which compensates the gain compression of the second stage. The combined two-stage amplifier results in output performance with reduced AM-AM conversion and, thus, improved linearity.

III. Measured MMIC PA Results

The GaN MMIC PA was fabricated using a process with a HEMT of 0.25μm gate length. The MMIC had a total gate periphery of 3.2 mm at the output stage, see Fig. 5. It was eutectically attached to amplifier housing for heat sinking. The measured small signal gain is shown in Fig. 6, and the output power versus input power is shown in Fig. 7. Good input/output match across most of the band have been achieved with the balanced configuration, indicating that the phases along the four signal path have been realized according to the design concept. The individual, single-ended amplifiers (based on simulations) did not have good input/output match except in a very narrow band. The measured saturated output power is about 6 watts.

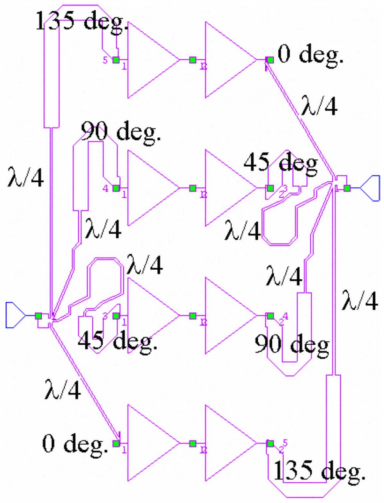

Fig. 4. Four way balanced amplifier.

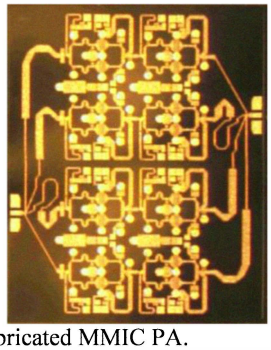

Fig. 5. Picture of fabricated MMIC PA.

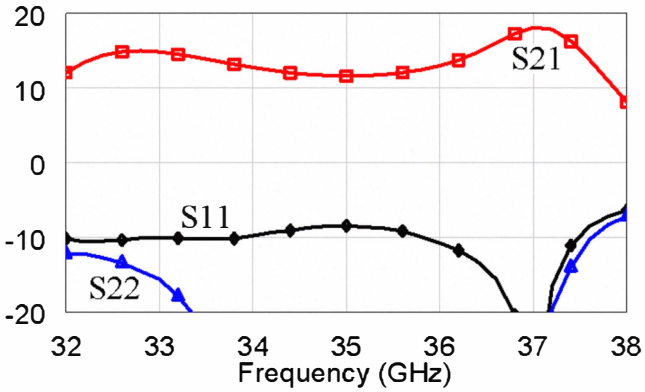

Fig. 6. Measureed S-parameters.

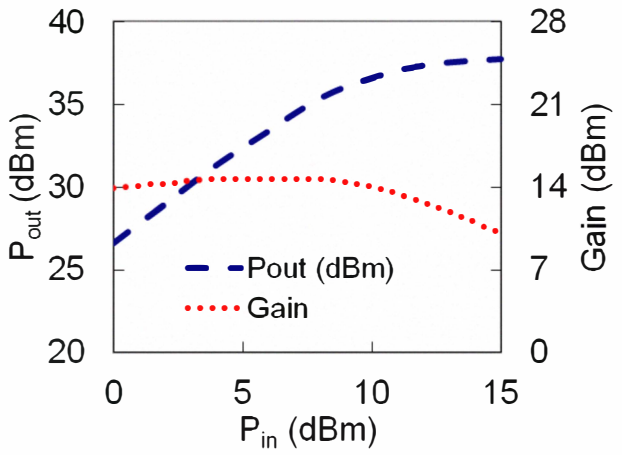

Fig. 7. Output power and gain versus input power at 32.5 GHz, 35 V drain voltage.

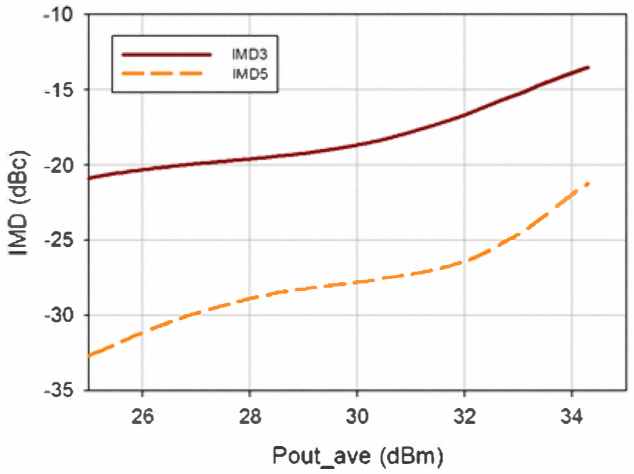

Figure 8. Measured two-tone IMDs of the amplifier.

The linearity was measured using a custom millimeter-wave digital waveform system. The system is capable of generating and analyzing wide range of waveforms including single-tone, two-tone, and digitally modulated waveforms up to 50 GHz.

All of the measurements were carried out in the Ka-band at 32 GHz, and the drain voltage for all amplifier stages was set at 32 V. Furthermore, the gate biases of the first stages in all the parallel branches were provided by a single DC supply and the gate bias of the second stages were provide by another DC power supply.

Fig. 9 shows the measured results of the two-tone intermodulation products (IMDs). The total drain currents in all the first stages, and all the second stages are 0.506 A and 0.777 A, respectively. The transfer characteristics of a mmW GaN HEMT have been shown to have strong dependence on the drain current bias. By optimizing the drain current biases for the first and the second stages separately, it is reasonable to suggest that improved linearity can be achieved. The combination of deep class AB in the first stage, and class A in the second stage results an improvement of 3-dB in IMD3.

IV. Conclusion

A balanced AlGaN/GaN on SiC MMIC PA has been demonstrated in the Ka-band. The use a novel, compact, four-way combiner/divider design has resulted in a two-stage PA with good I/O match across 32–38 GHz, and output power of 6 watts. Using the unique bias scheme for a *balanced*-AB class operation, improved linearity performance is also demonstrated.

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