

Integrated Broadband Lumped-Element Symmetrical-Hybrid N-way Power Dividers

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Abstract—This paper presents a monolithically-integrated, broadband, lumped-element, symmetrical-hybrid power divider centered at 20 GHz which was designed and fabricated to uniformly distribute power to arrays of Josephson junctions for superconducting voltage standards. This solution achieves a ten-fold decrease in chip area, and a two-fold increase in bandwidth when compared to a standard distributed 180°-hybrid by utilizing LC Π sections and a coplanar-waveguide phase inverter instead of transmission lines. A single divider demonstrates 0.5 dB maximum insertion loss, and a 1.5:1 VSWR bandwidth of 13–23 GHz. An eight-way, three-level, binary, power divider network is characterized in a divider/attenuator/combiner back-to-back measurement configuration with a 20 dB match bandwidth from 11.5–21.5 GHz. In the 15–22 GHz band of interest, the maximum insertion loss for the sixteen-way divider network is 1.0 dB, with an average of 0.5 dB.

Index Terms—Cryogenic electronics, Josephson arrays, lumped-element microwave circuits, microwave integrated circuits, power dividers, superconducting coils, superconducting microwave devices, superconducting integrated circuits.

I. INTRODUCTION

This work addresses the design, analysis, and testing of superconducting, microwave, integrated-circuit (IC), lumped-element, symmetrical-hybrid (s-hybrid) power dividers for a National Institute of Standards and Technology (NIST) programmable Josephson voltage standard [1]. On-chip power division is needed to excite multiple arrays of many Josephson junctions (JJs) periodically loading coplanar waveguide (CPW) transmission lines in niobium (Nb) on a silicon (Si) substrate [2]. The goal of the current research is to utilize a monolithically integrated sixteen-way power divider to excite $\sim 250\,000$ junctions at 20 GHz producing a 10 V programmable Josephson voltage standard [3].

The superconducting niobium used for the junctions enables broadband, lumped-element, power dividers with very low loss, compact size, and broad bandwidth compared to commercial and published dividers in CMOS and other technologies [4]–[6]. The authors' two- $\lambda/4$ section Wilkinson divider topology in [6] has the drawback of a 180° delay requiring a balanced N-way topology with reduced amplitude and phase balance. In this work, a s-hybrid based divider is investigated to circumvent these issues at the cost of larger area and a short-circuit DC path. Figure 1 is a micrograph showing a section of a fabricated divider test circuit with a design frequency of 20 GHz and bandwidth of 10 GHz.

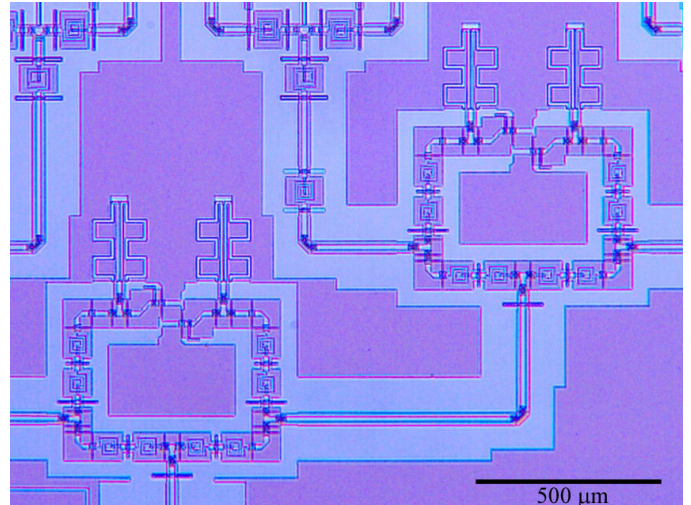


Fig. 1. A micrograph of a portion of the broadband, eight-way divider/attenuator/combiner configuration. Two binary levels of power division utilizing the 20 GHz lumped-element s-hybrid divider are shown. The light colored blue material is Nb, the darker purple material is the silicon substrate.

First, the design of a lumped-element s-hybrid divider unit cell is presented, including cryogenic measurement results from 10–30 GHz. Next, a three-level, binary divider utilizing these unit-cells was designed to meet the challenge of increasing the number of junction arrays under parallel microwave excitation on a chip. Cryogenic measurements are performed on the eight-way divider in a back-to-back divider/10 dB-attenuator/combiner configuration. This configuration preserves the desired matched-load, N-way divider in a two-port through test circuit suitable for insertion loss measurements.

II. PARISI S-HYBRID WITH PHASE INVERTER

A lumped-element Parisi hybrid can be synthesized by replacing the typical physical $\lambda/4$ sections of transmission line with lumped-element equivalent Π networks of $\pm\lambda/4$ electrical length [7]. This lumped-element topology allows a 10-fold reduction in physical length. The availability of superconducting planar spiral inductors allows multiple lumped-element Π sections in a $\lambda/4$ equivalent broadband configuration [4], [7]. The s-hybrid topology introduced in [8] improves the phase and amplitude balance of the divider by creating a five-port

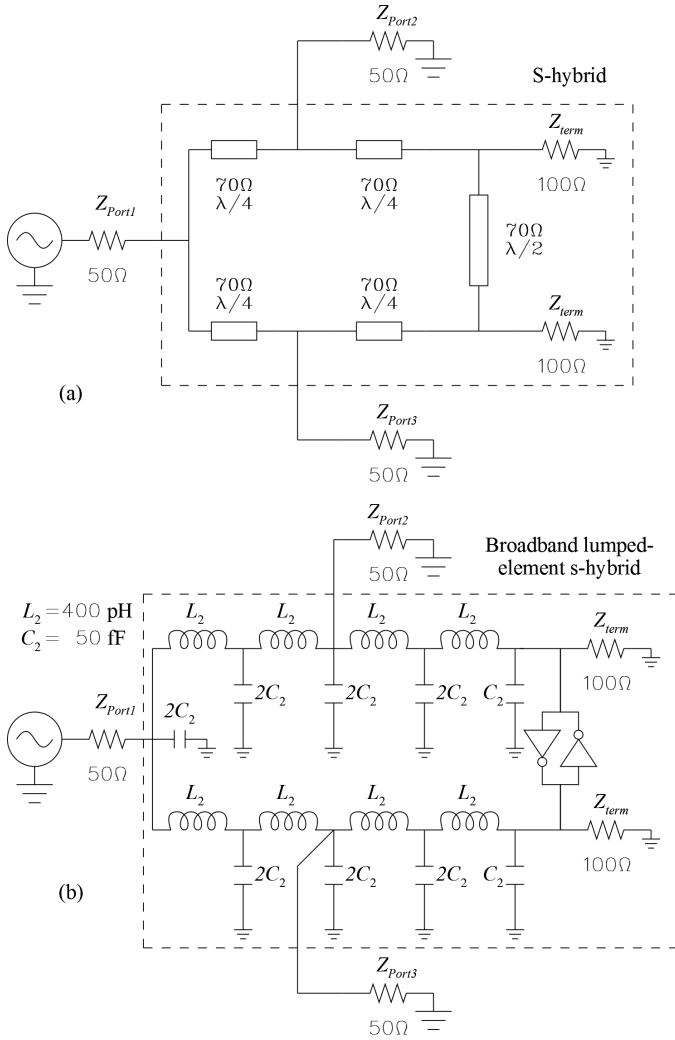


Fig. 2. Broadband s-hybrid power divider circuit schematics: (a) Distributed 50Ω input and output impedance divider, (b) divider with $\lambda/4$ transmission line elements replaced by Π section lumped-element equivalents with values given for a 20 GHz center frequency.

circuit with a central line of symmetry. The bandwidth of the circuit can be further improved by implementing the 180° line section using a broadband CPW phase inverter. The broadband lumped-element s-hybrid power divider, shown in Fig. 2 (b), exhibits approximately double the bandwidth compared to that of a distributed 180° s-hybrid, shown in Fig. 2 (a), in one-tenth the area.

A. Design

The values for a canonical low-pass $\lambda/4$ Π network with series inductance, L_s , and shunt capacitance, C_p , frequency f_0 in hertz, and characteristic impedance Z_0 in ohms are given by [7]:

$$L_1 = \frac{Z_0}{2 \cdot \pi \cdot f_0}, \text{ and } C_1 = \frac{1}{2 \cdot \pi \cdot f_0 \cdot Z_0}. \quad (1)$$

To realize a broader bandwidth $\lambda/4$ equivalent segment, ex-

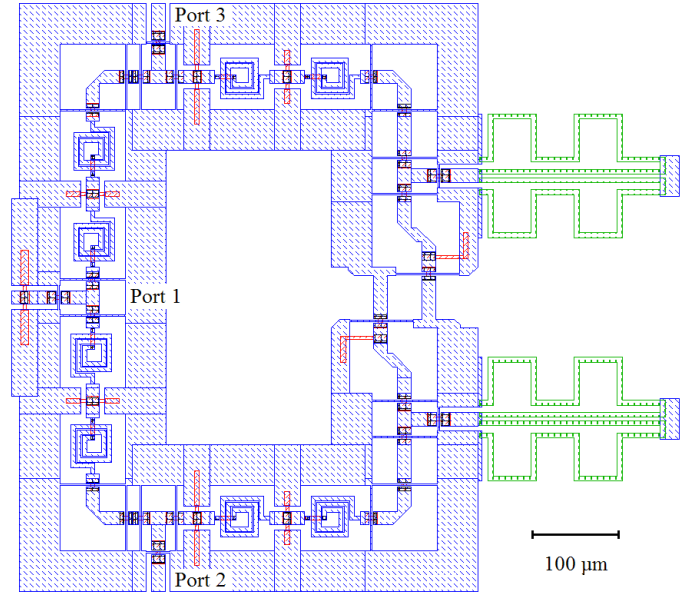


Fig. 3. A layout of the broadband lumped-element 20 GHz s-hybrid from Fig. 2 (c). Red \square hatch is Nb1, black \boxtimes hatch is Nb1-2 via, blue \square hatch is Nb2 and green \square hatch is AuPd. Solid blue lines in the CPW ground planes show the HFSS simulation cell boundaries. Approximate divider dimensions are $800\ \mu\text{m}$ ($0.13\ \lambda$) \times $700\ \mu\text{m}$ ($0.11\ \lambda$) with minimum trace width and spacing of $1.5\ \mu\text{m}$ ($0.0002\ \lambda$).

pressions for multiple LC Π sections in a $\lambda/4$ line can be derived by solving the lumped element equivalent circuit for the desired phase shift response as in [7]. For a two LC Π section $\lambda/4$ equivalent line the L and C values are given by:

$$L_2 = \frac{Z_0}{\sqrt{2} \cdot 2 \cdot \pi \cdot f_0}, \text{ and } C_2 = \frac{\sqrt{2} - 1}{2 \cdot \pi \cdot f_0 \cdot Z_0}. \quad (2)$$

L and C values for a 70Ω $\lambda/4$ section centered at 20 GHz, are given in Fig. 2. These values are well within the range of impedance values realizable in the NIST IC process.

The closed-form circuit models in Fig. 2 were optimized in Ansoft's Designer v3.5¹ circuit simulator using 3-D FEM circuit element models from Ansoft's HFSS v11¹ to correct for layout parasitics. Each superconducting niobium trace is modeled with a 3-D perfect electric conductor (PEC) in HFSS. The solid blue lines in the ground planes of the divider layout in Fig. 3 indicate the HFSS cell boundaries. The final layout was then verified with a complete HFSS simulation.

B. Layout and Fabrication

The NIST superconducting IC fabrication process layer stack is shown in Table I. Minimum line widths and spacings are $1\ \mu\text{m}$ for all layers. This process generates resistors of $\sim 2\ \Omega/\square$, metal-insulator-metal (MIM) capacitors of

¹Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

TABLE I
NIST IC FABRICATION PROCESS LAYER STACK.

Layer name	Material	h [μm]	Properties
Resistor	AuPd	0.13	$\sigma = 4 \text{ E}^6 \text{ } \Omega/\text{m}$
Nb2	Nb	0.70	$\sim\text{PEC}$
MIM oxide	SiO_2	0.30	$\epsilon_r = 4.5$
JJ electrode	Nb	0.17	not used here
JJ barrier	$\text{Nb}_x\text{Si}_{1-x}$	0.01	not used here
Nb1	Nb	0.30	$\sim\text{PEC}$
Oxide	SiO_2	0.15	$\epsilon_r = 4.5$
Substrate	Si	380	$\epsilon_r = 11.5$

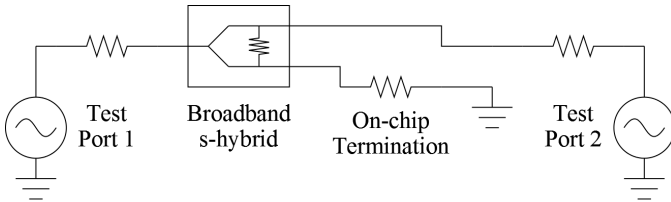


Fig. 4. Three-port divider to two-port network analysis conversion circuit with port 3 terminated on-chip.

$\sim 0.1 \text{ fF}/\mu\text{m}^2$, and under-passed spiral inductors in the range of 100–5000 pH. Lumped $\lambda/4$ sections with L_1 and C_1 integrated into Nb on silicon CPW with a center conductor width of 16 μm and gap of 8 μm can be realized in a 130 μm length of CPW, as compared to 1600 μm for a distributed $\lambda/4$ section at 20 GHz.

Figure 3 shows a typical layout of a 20 GHz design-frequency broadband, lumped-element s-hybrid power divider with 50 Ω input and output impedances. Approximate dimensions of this lumped-element s-hybrid are 800 μm (0.13λ) \times 700 μm (0.11λ), as compared with a standard distributed 180 $^\circ$ -hybrid at 20 GHz, which would be approximately 3000 μm in diameter. A two-port test circuit, shown in Fig. 4 with port 3 terminated on chip was fabricated in the NIST Boulder Quantum Fabrication Facility for unit-cell testing.

C. Testing

Measurements were performed with an Agilent 8722ES¹ vector network analyzer (VNA). Calibration was accomplished using on-chip Through-Reflect (short)-Line (1.5 mm) (TRL) standards with a band of 8–35 GHz at 4 K immersed in a liquid He ($\epsilon_r = 1.005$) dewar. Table II shows a summary of divider test circuit measurement results. Figure 5 shows a comparison of HFSS simulations and measurements for the test circuit in Fig. 4. The 15–22 GHz band is considered the band of interest for this design, allowing for ample tuning around the 20 GHz junction array design point. Average in-band values in Table II are computed as the base-10 logarithm of mean power:

$$\text{Ave}|S_{ij}| = 10 \cdot \log_{10} \left[\text{Mean}_{15 \text{ GHz}}^{25 \text{ GHz}} (|S_{ij}|^2) \right]. \quad (3)$$

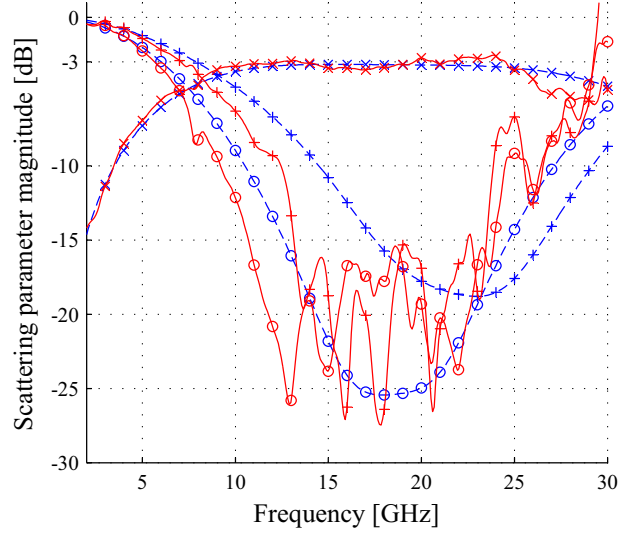


Fig. 5. Broadband lumped-element s-hybrid, Fig. 3, HFSS simulated data (blue dashed lines) and measurement results (red solid lines) from test circuit shown in Fig. 4 using 4 K TRL calibration on chip. S_{11} is marked with \circ , S_{21} is marked with \times , and S_{22} is marked with $+$.

TABLE II
S-HYBRID DIVIDER UNIT-CELL AND EIGHT-WAY DIVIDER
MEASUREMENT DATA CALCULATED FROM THE RESULTS SHOWN
IN FIG. 5 AND FIG. 6.

Test Circuit	Parameter	$BW _{-15 \text{ dB}}$	$\text{Ave} _{15 \text{ GHz}}^{22 \text{ GHz}}$	$\text{Max} _{15 \text{ GHz}}^{22 \text{ GHz}}$
Unit-cell	S_{11}	13–23 GHz	–18.4 dB	–15.4 dB
Unit-cell	S_{22}	10–25 GHz	–19.2 dB	–15.2 dB
Unit-cell	IL	–	0.2 dB	0.5 dB
D/A/C	S_{11}	11–22 GHz	–22.3 dB	–17.9 dB
D/A/C	IL_{total}	–	10.4 dB	11.2 dB
10 dB attn.	S_{11}	13–23 GHz	–25.7 dB	–21.4 dB
10 dB attn.	IL	–	9.5 dB	9.9 dB
D/A/C	IL_{divider}	–	0.5 dB	1.0 dB

Insertion loss, IL , for this work is defined as

$$IL = -10 \cdot \log_{10} \frac{\sum_{i=2}^N (|S_{i1}|^2)}{1 - |S_{11}|^2}. \quad (4)$$

By circuit symmetry and from simulation results, S_{31} is assumed to be approximately equal to S_{21} for insertion loss calculations for the s-hybrid unit-cell.

III. EIGHT-WAY POWER DIVIDER

Many-way power division can be achieved in a corporate divider topology by creating a binary division tree of two-way dividers. Due to chip area constraints only an eight-way division is implemented here with broadband lumped-element Wilkinson dividers [6] for the final level of division. The

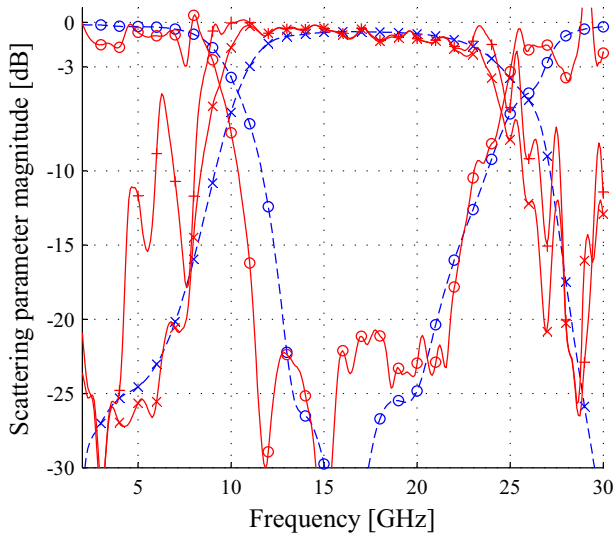


Fig. 6. Divider/attenuator/combiner (D/A/C) configuration eight-way s-hybrid divider measured versus simulated results. S_{21} and IL are calculated by subtracting 10 dB attenuator data from D/A/C test configuration data. Hybrid Designer circuit and HFSS 3-D FEM simulated data (blue dashed lines), and measurements (red solid lines) using 4 K TRL calibration on chip. S_{11} is marked with \circ , S_{21} is marked with \times , and insertion loss is marked with $+$.

number of divisions scales easily in simulation, a 16-way or 32-way division for the PJVS could be easily implemented in a larger chip area.

In order to appropriately characterize a many-way divider, a test circuit is needed that preserves both the desired loading at the output, as well as the ability to measure insertion loss through the device. A simple back-to-back divider/combiner circuit has a fundamental flaw of terminating a divider circuit with its own complex output impedance, rather than the desired real $50\ \Omega$ load needed to obtain valid S-parameters. To solve this problem 10 dB attenuators are monolithically integrated between the divider circuit under test, and the combiner output circuit [6]. The entire eight-way divider/attenuator/combiner network is simulated in Designer using the hybrid simulation methodology discussed in Section II-A. A lithographically identical 10 dB attenuator was fabricated on the same wafer as the divider/attenuator/combiner to allow deembedding of the divider performance.

The eight-way divider/attenuator/combiner configuration test chip was evaluated in the same manner as the unit-cell divider chips, discussed in Section II-C. Figure 6 compares measured and simulated results from the eight-way divider/attenuator/combiner configuration. Table II summarizes the measurement data from the divider/attenuator/combiner (D/A/C), and the 10 dB attenuator (10 dB attn). This divider/attenuator/combiner configuration is a useful measurement technique for characterization of many-port integrated devices.

Assuming the loss in the division is the same as the loss in the recombination, the average and maximum insertion loss through a single eight-way divider network, IL_{divider} , can be computed as half of the total for the divider/combiner, IL_{total} after subtracting the measured insertion loss of a matched, lithographically-identical, 10 dB attenuator on the same chip. The divider/attenuator/combiner measured data set shown in Fig. 6 and Table II has been calculated in this manner. The 1 dB maximum eight-way power divider loss is very small compared to the 3 dB cable loss incurred in the 1.2 m cryoprobe, or to any commercially available broadband divider solution in the 15–22 GHz band [6].

IV. DISCUSSION AND CONCLUSIONS

In this work, broadband, low-loss, compact, lumped-element, many-way, s-hybrid power dividers were demonstrated using a NIST microfabrication process. The lumped-element s-hybrid with a CPW phase inverter demonstrated here has double the bandwidth in one-tenth the area, and improved amplitude and phase balance bandwidth, when compared to a canonical distributed 180° hybrid. This topology can be optimized for improved power handling and heat dissipation with two shunt resistors to ground, when compared to a Wilkinson based divider topology with one signal-to-signal resistor.

A back-to-back test configuration for many-way dividers with integrated 10 dB attenuators was utilized to present a $50\ \Omega$ load at the eight-way divider output while maintaining the ability to measure insertion loss through the device. This innovation allows for improved divider characterization at the cost of fabricating and measuring an additional 10 dB attenuator.

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REFERENCES

- [1] S.P. Benz and C.A. Hamilton, "Application of the Josephson Effect to Voltage Metrology," *Proceedings of the IEEE*, Vol. 92, No. 10, pp. 1617–1629, Oct. 2004.
- [2] P.D. Dresselhaus, et al., "Design of SNS Josephson Arrays for High Voltage Applications," *Applied Superconductivity, IEEE Trans. on*, Vol. 17, No. 2, pp. 173–176, June 2007.
- [3] P.D. Dresselhaus, et al., "Design of a Turn-key 10 V Programmable Josephson Voltage Standard System," *Conference on Precision Electromagnetic Measurements Digest*, June 2008.
- [4] A.R. Kerr, et al., "A Superconducting 180° IF Hybrid for Balanced SIS Mixers," *17th International Symposium on Space and Terahertz Technology*, May 2006.
- [5] J.G. Kim, and G.M. Rebeiz, "Miniature Four-Way and Two-Way 24 GHz Wilkinson Power Dividers in $0.13\ \mu\text{m}$ CMOS," *IEEE Microwave and Wireless Components Letters*, Vol. 17, No. 9, pp. 658–660, Sept. 2007.
- [6] M.M. Elsbury, et al., "Broadband Lumped-Element Integrated N-Way Power Dividers for Voltage Standards," *Microwave Theory and Techniques, IEEE Trans. on*, in review.
- [7] S.J. Parisi "180° Lumped Element Hybrid," *Microwave Theory and Techniques, Symposium Digest*, Vol. 3, pp. 1243–1246, June 1989.
- [8] J. Hughes and K. Wilson "High Power Multiple Impatt Amplifiers," *European Microwave Conference, 1974. 4th*, pp. 118–122, Oct. 1974.