Concept for an All-Digital Satellite Communications Earth Terminal

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ABSTRACT

Current DoD requirements call for a single Enterprise Terminal supporting up to 48/96 (threshold/objective) transmit and 56/112 (threshold/objective) receive communications carriers, not considering future expansion. The number of links supported by an Enterprise Terminal dictates aggregate servicing capacity. A single Teleport/standardized tactical entry point (STEP) site can consist of five or more terminals operating in several frequency bands. Each carrier requires individual converter and modem chains, which are linked to the antennas with a complex switch matrix subsystem. This architecture results in severe size, weight, and power (SWAP) constraints that limit expansion to support objective capacity and connectivity requirements within available facility space and infrastructure.

By moving the digital conversion as close to the antenna as possible, a number of efficiencies in SWAP and performance can be achieved. The individual converters can be replaced with wideband, multi-carrier digital up and down converters co-located with the antenna. The complex switch matrix can be eliminated and replaced with a lightweight digital distribution system. The modem functions can be consolidated into a multi-card enclosure, where several carriers can be implemented on a single programmable processor card.

In addition to reducing terminal complexity and SWAP, this approach also enables concepts such as hybrid mesh networks, decentralized power monitoring and control, and remote terminal control. This has the potential to dramatically increase satellite network efficiency and improve utilization of expensive satellite assets. This paper expands upon preliminary work performed to date at CERDEC.

INTRODUCTION

The Enterprise Wideband SATCOM Terminals Systems (EWSTS) is a family of terminals that provide world wide coverage, connectivity, and mission essential services to joint forces. EWSTS is a major component to the Global Information Grid (GIG) and an integral piece to achieving network centricity. The first generation EWSTS terminals, supporting early Defense Satellite Communications System (DSCS) satellites and commercial satellites (C and Ku band), have been procured, maintained, and upgraded over the last thirty years. During that time frame requirements have changed as a consequence of force mobilization and an increase in information exchange, demanding more capacity and connectivity. With the emergence of the Wideband Global SATCOM (WGS) constellation, the second generation of EWSTS terminals provides supportability, interoperability, and a high capacity/connectivity capability. Generation two, much like the previous generation has a life cycle expectancy of about 20-25 years, in which time modernization shall occur.

Future Advanced SATCOM Terminals (FAST) is a CERDEC program investigating and developing advanced satellite communications technology for potential insertion into the modernization of current and future generations of EWSTS. This program takes a close look at the past, current, and projected enterprise terminals to develop this technology. Furthermore, this program understands the complexity of the existing enterprise terminal architecture and its planned evolutionary upgrade path. FAST leverages advanced digital processing concepts, modular card level components, and mature analog-to-digital (A/D) and digital-to-analog (D/A) technology to develop a digital modular based terminal architecture. A digital based terminal architecture enables innovative network architectures, monitoring and control features, with potential for improved terminal and bandwidth utilization. CERDEC has experimented and demonstrated a digital based receive system, with technology developed by Hypres, Welkin Sciences, EADS Astrium, and L-3 Communications Systems–West through Small Business Innovative Research (SBIR) and Cooperative Research and Development (CRADA) programs. This experimental system serves as motivation for the concept of a digital based terminal.

MOTIVATION

In FY 07 CERDEC Space & Terrestrial Communications Directorate demonstrated an All Digital Receiver (ADR) developed by Hypres. This ADR uses superconducting Rapid Single Flux Quantum (RSFQ) devices to perform direct digital conversion of X-Band (7.5 GHz). The ADR system is a superconductor integrated circuit chip, consisting of a bandpass delta-sigma analog-to-digital converter (ADC) modulator and a digital channelizing circuit both clocked above 10 GHz, used to convert RF signals in the 7.25-7.75 GHz range to digital and perform down-conversion and filtering completely in digital domain [2]. The output of the ADR is a 16 bit in-phase (I) and quadrature (Q) signal. Demodulation of this I & Q signal required L-3 Communications Systems- West (CS-W) to modify their Generation-3 modem. The Generation-3 modem was modified to accept 16 bit parallel I & Q data directly from the ADR. Essentially the Generation-3 modem behaved as a direct baseband processor.

The demonstration was performed on an EWSTS test terminal over the air on the XTAR satellite, demonstrating complete demodulation of video and data over a MIL-STD-188 165 A waveform. The transmit source consisted of a packetized video feed modulated onto a 1.544 Mbps BPSK carrier, transmitted through the AN/GSC-39 terminal at X-band (8.326 GHz). The X-band (7.676 GHz) downlink was fed directly to the ADR for digitization and decimation, and hand off of 16 bit parallel I & Q to Generation-3 modem for demodulation. Note that the modem on the transmit side was not modified, and although the receive portion of the experiment was performed at the same location it was not in a loopback configuration (independent modems were used).

This demonstration served as an early proof of concept experiment for an "all digital terminal". As a result CERDEC initiated parallel efforts exploring advanced waveform processing techniques with EADS Astrium and Welkins Sciences. These efforts were to develop waveform processors capable of channelizing a wideband digital signal and processing the individual baseband signals, with programmable features.

CONCEPT OF A DIGITAL TERMINAL

The current terminal architecture RF subsystem on newer terminals takes a RF analog and block up/down converts to an analog IF. The analog IF then runs through the Interconnect Facility (ICF). The ICF comprises all fiber optic, copper or microwave connectivity between the terminal and its supporting technical control. The analog IF off the ICF interfaces to the Digital Communications Satellite System (DCSS). The DCSS performs all the modem, multiplexing, switching, routing, patching, and link adaptation functions. Current DCSS implementations are comprised of over 70 different rack configurations and 90 different equipment types that can be installed in a van or fixed configurations [1].

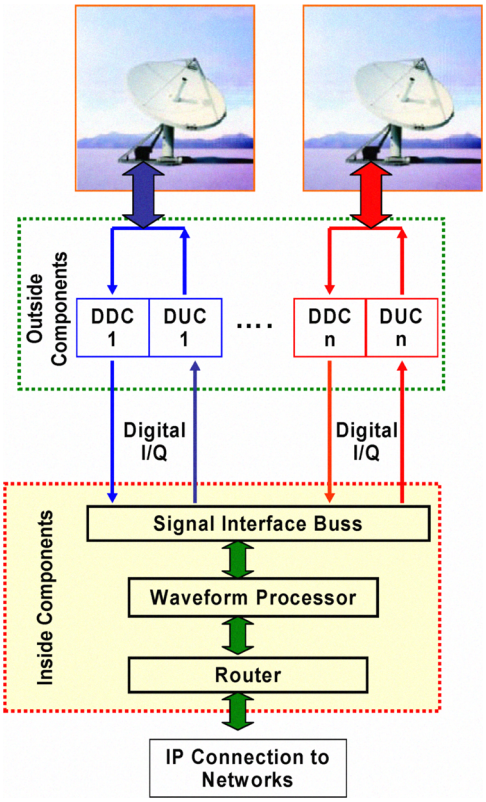

Figure 1 Digital Terminal Architecture

The concept of a digital terminal is derived from the ability to provide the DCSS with a wideband digital signal. This would be realized by introducing a wideband digitization and synthesizing function at the RF subsystem and ICF boundary, eliminating the adjoining analog front end, networks of combiners/dividers/filters and complex switch matrices. The wideband digitization/synthesis function would be done at IF, ranging between 950 – 2150 MHz. This frequency range was selected based on an assessment of what is currently feasible with reasonably mature technology that would be interoperable with EWSTS terminals without requiring major modifications. Once in the digital domain the wideband signal would be a preserved "digital copy", ready for further processing and manipulation. The digital domain offers tremendous advantages in regards to compensation of amplitude and phase imbalances; not as sensitive to the effects of temperature in regards to linear performance and frequency drift as analog components (corrective through

software); adaptive equalization and linearization techniques can be implemented. The "digital copy" would be a 500 – 1000 MHz wide aggregate/instantaneous bandwidth (depending on downlink bandwidth) digitized downlink, where the composite digital I & Q would traverse over the ICF to a waveform processor. The waveform processor would be a modular, multi-functional, signal processor with some programmable (swap out/add-on) features including waveform portability. It would channelize the composite digital I & Q, and handle individual stream modulation/demodulation. The waveform processor would provide the data streams in a packetized format for network distribution, see Figure 1. The waveform processor would have functional equivalency of approximately 120 modems, but at a 6:1 reduction in power consumption and greater than 60 % reduction in form factor.

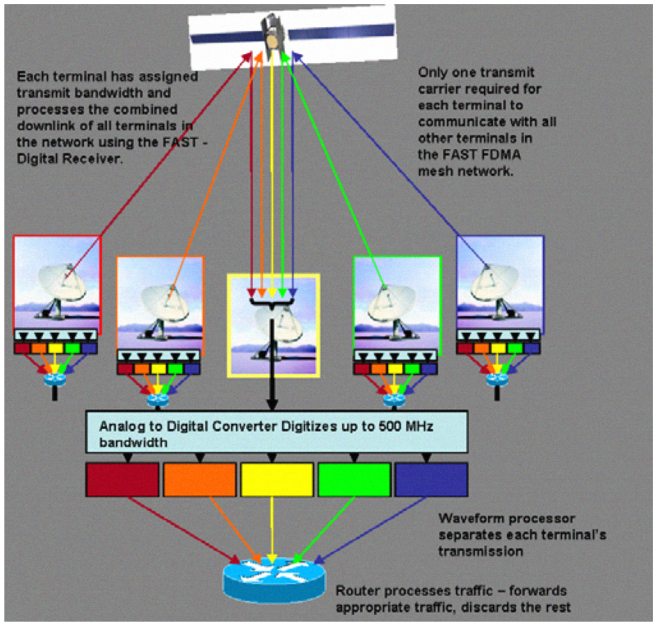

Figure 2. System Architecture

With a "digital copy" and a robust waveform processor, features such as redundancy, power control and spectrum monitoring, can be centralized and/or decentralized to the terminal. In a decentralized mode, with all processing done in the digital domain an operator can automate or have a high fidelity level of control, allowing for built in feed back between power control and spectrum monitoring functions to include failover within implemented policies. From the networking aspect, this technology enables innovative network architectures for medium-large/ large-large size terminals. An example of this concept is depicted in Figure 2. With a wideband digital receiver implemented at all terminals, they would all have the ability to process the entire (viewable) downlink band of a satellite. In essence, the number of transmit carriers required to extend a frequency division multiple access (FDMA) network across medium-large terminals would be reduced. To explore this further, let "n" be the number of terminals in a network, where each terminal is required to use FDMA for dedicated trunks between terminals. To form a mesh topology requires each terminal to put up a number of carriers, let "C_{total}" be the summation of carriers from the set of "n" terminals, $C_{total} = \sum_{N=1}^{n} 2(N-1)$. The sum "$C_{total}$" for a set of "$n$" terminals is $C_{total} = n(n-1)$. Letting $C_{total} \rightarrow n$, reduces "C_{total}" by a factor of $\frac{1}{n-1}$. The reduction factor of "C_{total}" directly correlates to a reduction in bandwidth. Figure 3 shows a normalized overall bandwidth reduction and comparison.

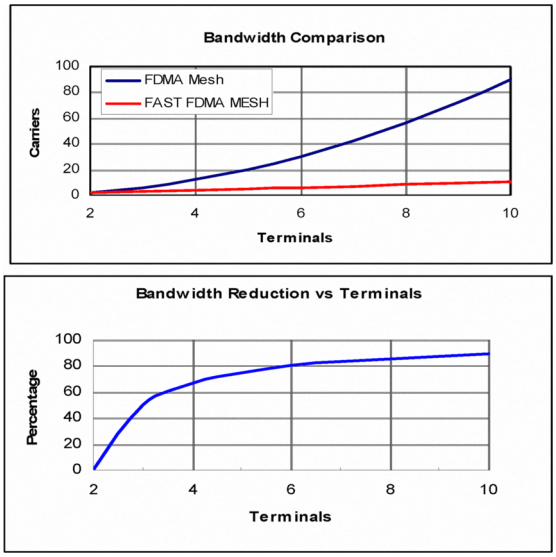

Figure 3. Bandwidth Comparison & Reduction

This works out to a 50 % reduction in bandwidth for at least a three terminal configuration requiring topology in Figure 2. Reducing the number of carriers at a given terminal reduces the amount of additional back off required, which open up trades, e.g., either resizing the transmitter or gaining additional margin. A FAST terminal in this configuration eliminates multiple satellite hops to communicate across any two or more given points in a multi-terminal network. Bandwidth and utilization efficiencies can be realized by the inherent properties of a FAST digital terminal. FAST network topology is not limited to just FDMA. The waveform processor can host other waveforms such that other topologies can be implemented. There are some fundamental challenges of porting that require attention to implementation, more so for complex waveforms. CERDEC plans to explore the implementation, networking, and utilization trades in future analysis.

TECHNICAL APPROACH & CHALLENGES

Design of the digitization and synthesis function in the terminal RF subsystem requires attention to some fundamental challenges that need to be considered in determining an approach that offers the best value, in terms of requirements and cost. Bandwidth, dynamic range, spurious free dynamic range (SFDR), and number of carriers supported are requirements that will drive design and method of implementation. There are two methods to consider; direct RF sampling-synthesis and IF sampling-synthesis. RF sampling-synthesis approach requires high speed ADC/DAC to operate with-in the 1st Nyquist zone, for recovery-construction of both frequency and signal bandwidth. RF sampling-synthesis can be done with ADC/DAC operating outside the 1st Nyquist zone, this technique would yield recovery-construction from a fold or image near DC, this form of band-pass sampling is applicable to IF sampling-synthesis as well. This method does not recover frequency (sampling independent of frequency), only signal bandwidth (sampling rate depends on bandwidth), reduces the overall instantaneous bandwidth of the device, and requires special attention to the design of reconstruction filters and band-pass filters. There is a trade present, such that the effective bandwidth within zone is reduced and integrated noise power is reduced, gaining slight increase in signal-to-noise ratio (SNR). IF sampling-synthesis approach requires up/down conversion stage to/from RF, such that ADC/DAC can digitize-synthesize an IF signal. Compared to the RF sampling-synthesis approach, this approach requires an ADC/DAC with 1/6th sampling capability operating in the 1st Nyquist zone, thus requiring less sampling capability if chosen to under sample. There is another fundamental challenge of high rate and under sampled sampling-synthesis that must be accounted for which greatly dictates device effective performance: sampling clock jitter. Clock jitter drives the effective SNR achieved by device, which in turn will affect Effective Number of Bits (ENOB). Clock jitter is dependent on the input frequency being sampled and not on the bandwidth of the input signal, so this serves as a double edge sword in high frequency under sampled applications (high frequency relative to 1st Nyquist zone of ADC). As the frequency increases beyond the 1st Nyquist zone, the ADC is sampling at full scale, performance decreases in terms of ENOB, SNR, and SFDR. Consider a realistic scenario incorporating driving requirements, a terminal operating in either X or Ka band, where the instantaneous bandwidths are 500 MHz and 1000 MHz respectively, with receive signal dynamic range of about 65 dB, requiring a ADC to have a SNR (plus margin) of 80-85 dB [4]. The relationship between SNR and clock jitter is $SNR = 20\log\frac{1}{2\pi f_c t_{rms}}$, where "$f_c$" is the input carrier frequency to ADC and "t_{rms}" is aperture jitter. This assumes an ideal ADC with no internal aperture jitter. ADC effective resolution is related to SNR by $ENOB = \frac{SNR - 1.76}{6.02}$.

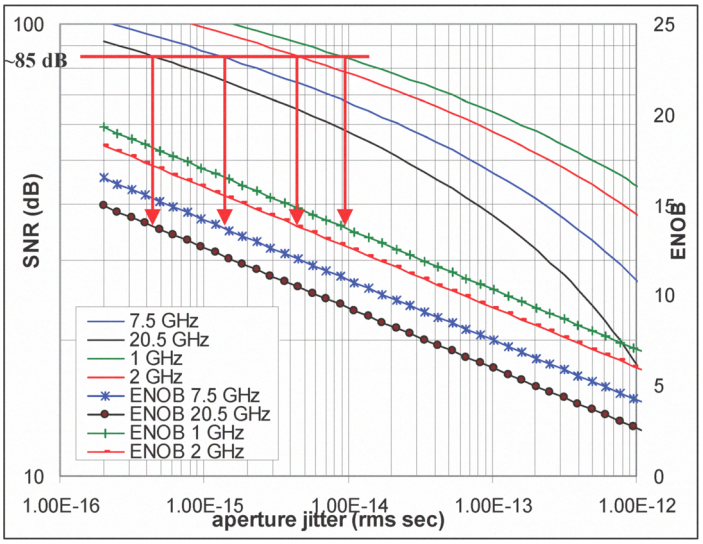

Figure 4 Effect of clock jitter on SNR & ENOB

Establishing the necessary relations between clock jitter, SNR, and ENOB yields Figure 4. This shows that for required SNR of 80-85 dB, depending on the input frequency sampled by the ADC requires an accurate clock source with very small jitter. After performing market surveys on available technology, the conclusion has been made that the top end on-board clock oscillators have jitter greater than 50 femtoseconds. What does this means for an application using direct RF sampling approach operating in the 1st Nyquist Zone, with the requirements for the terminal scenario? At best the ADC will only be able to achieve a SNR of 44 – 50 dB, and an ENOB of 7-8 bits. This will also impact SFDR. An IF sampling approach operating in the 1st Nyquist Zone, would achieve a SNR of 65-70 dB, and an ENOB of 12-13 bits. Market surveys show that ADC/DAC's for the IF sampling approach are commercially available, continually improving, and are less costly. Surveys also indicate an RF sampling approach requires additional development of the needed ADC/DAC's, and would likely be relatively expensive.

CONCLUSION

Increased capability requirements for future EWSTS terminals make it important to investigate methods to implement a more cohesive and easily operated system [1]. Bandwidth constraints and rapidly increasing demand make it important to investigate ways to achieve greater terminal and overall bandwidth efficiency. FAST is a start to addressing both of these concerns. FAST enables automation of previously manual functions like data patching, Intermediate Frequency (IF) patching and test functions. FAST enables a higher level of integration and automation of functions, including configuration, monitoring and control functions. FAST introduces a flexible digital modular architecture, which would require only software upgrades, and waveform ports, with minimal ("next to none") hardware changes over the terminal life cycle, making evolutionary upgrades over time seamless and less costly.

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