PIEZOELECTRIC MICRO-SCALE MECHANICAL COMPUTING SYSTEM

Robert M. Proie Jr., Jeffrey S. Pulskamp, Ronald G. Polcawich, Tony Ivanov
US Army Research Laboratory, Adelphi, Maryland, USA

ABSTRACT

Near-zero leakage current, nearly ideal on to off-state current ratios, sharp voltage to current relationship slopes and potential for intrinsic immunity to radiation have made MEMS-based mechanical logic an attractive area of research. This work builds upon an ongoing research effort, which aims to develop a lead zirconate titanate (PZT)-based, mechanical logic architecture, in order to demonstrate a fully capable digital MEMS system. The work presented here demonstrates an integration of combinational and sequential mechanical logic elements to provide a 1-bit counter without the aid of semiconductor technologies. The system demonstrates both proper functionality and data retention over multiple cycles.

INTRODUCTION

Near-zero leakage current and potential for intrinsic immunity to radiation have made MEMS-based mechanical logic an attractive area of research. Additionally, while fundamental sub-threshold slope limits of the metal-oxide-semiconductor field-effect-transistor (MOSFET) will ultimately hinder its minimum switching voltage [1], MEMS devices have the potential achieve at least an order of magnitude steeper slope [2]. Moreover, the physical gaps that typically separate the source and drain in MEMS relays and the metal-to-metal contact in the closed state produce a very high on to off-state current ratio.

Over the past few years, several groups have explored MEMS-based mechanical logic technologies up to the Boolean gate level either through electrostatic [2], [3] or piezoelectric devices [4]. These groups have focused on processes that maintain compatibility with existing CMOS fabrication flows. While that approach has its benefits, in each case the device's performance is degraded either in terms of voltage, speed or area.

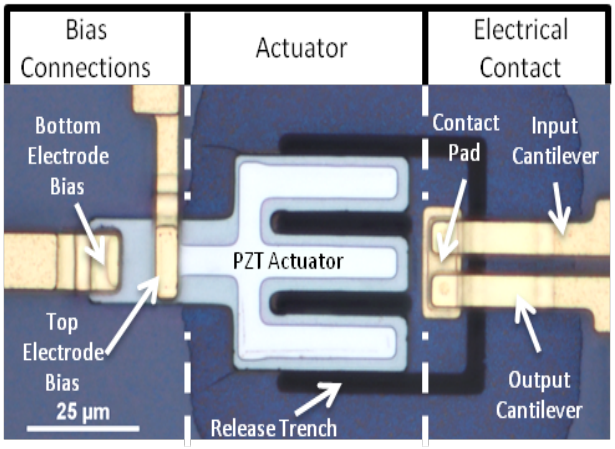

Figure 1: Fabricated image of the single-pole, single-throw digital MEMS relay.

This work builds on an alternative approach, which utilizes the lead zirconate titanate (PZT), mechanical logic architecture presented in [5]-[7]. The approach sacrifices integrated CMOS compatibility to obtain PZT's large d_{31} piezoelectric coefficient. This feature provides large deflections, relative to other common piezoelectric materials [8], at modest voltages. This enables a reduction in actuator length while still maintaining low actuation voltages, measured as low as 0.1 V, and contact gaps capable of supporting large output voltages, up to 40 V. The previous works have focused on developing the individual combinational and sequential elements. The work presented here demonstrates an integration of the combinational and sequential elements to provide a complete system and discusses the challenges associated with that integration.

DEVICE DESIGN AND PERFORMANCE CHARACTERISTICS

The switching element, shown optically in Figure 1, is configured as a normally open, single-pole, single-throw (SPST) relay. The relay utilizes a converse piezoelectric effect driven unimorph actuator, enabled via two platinum (Pt) electrodes that provide an electric field across a PZT (52/48) thin-film layer, to generate movement. Below the bottom Pt electrode is a three-layer, thin film stack. This stack, termed the elastic stack, is composed of two layers of silicon dioxide with a silicon nitride layer in between.

The design of the relay was intended to mimic that of the MOSFET, while improving upon the energy efficiency. To do this, the device needed an input that was electrically decoupled from the output, a high on to off-state current ratio and a sharp slope between the current-voltage relationship when turning on and off the device. For this design, the two Pt electrodes are separated from the contact system by a 0.5-µm gap, achieving both the decoupling and also minimizing any potential gate to channel leakage currents. The metal contacts used in the design are isolated by an air gap of approximately 300-nm, making the resistance essentially infinite and provide a closed-state resistance of under 100-Ω, which results in very high on to off-state current ratios. Additionally, metal-to-metal contacts are ambipolar, which allows a single device to carry both high and low voltages equally well. Finally, inherent in a metal contact switch is a sharp transition between the on and off states [2]. Real world conditions, however, such as hysteresis in the contacts and piezoelectric material, along with supply voltage noise, will limit this slope.

The operation of the device revolves around the movement of a contact pad, which is located on the distal end of the relay and situated below two substrate-anchored, Au cantilevers. When the electric field is small (~0-V), an air gap separates the contact pad from the cantilevers, leaving the two cantilevers electrically

isolated from each other. As the electric field increases, the actuator will deflect upward until the contact pad presses against the two cantilevers, electrically shorting them together. By using a high voltage reference on one electrode, rather than a ground reference, the device can also function as a normally closed relay, which enables it to mimic NMOS and PMOS functionality. While the bipolar nature of the device allows either electrode to serve as a fixed reference, a preferred polarity exists in the PZT with a positive bias applied relative to the bottom electric as shown in Figure 2.

The fabrication process performed is similar to the one reported in [6] with the addition of a nichrome thin film as a high resistivity material. The expected sub-kΩ contact resistance of these devices, coupled with potential contact hysteresis made the inclusion of current limiting resistors important to the reliability of circuits constructed with SPST relays. The nichrome film provided this capability. Tables 1 and 2 highlight the key performance attributes of the relay.

SYSTEM DESIGN AND RESULTS

It was shown in [7] that individual relays could be combined to form combinational and sequential Boolean gates. The system presented here, shown in Figure 3, expands on that concept by realizing a 1-bit counter. The counter is composed of an inverter and a dynamic latch. The goal of this system was two-fold: understand the challenges involved in building systems from digital MEMS gates and demonstration the processing and data retention capabilities of the devices.

The inverter utilizes two relays with their output cantilevers tied together. A common connection was also made between one of the electrodes on each relay. One relay has a ground reference connected to its non-shared Pt electrode and the input cantilever. The other relay has both its free Pt electrode and input cantilever tied to a high-voltage reference. When a low-voltage signal is passed to the shared electrode connection, the relay with the high-voltage reference closes, passing that high-voltage to the output. As the voltage on the shared electrode increases, that relay eventually opens and the relay with the ground reference closes, effectively grounding the output. This behavior is shown in Figure 4. While the design and operation of a MEMS inverter by itself is straightforward, in larger systems the contact and piezoelectric hysteresis can prove destructive to the device. The source of failure is a potential connection between the high and low voltage rails. In MOSFETs, this situation is referred to as short circuit power draw and occurs while the pull-up and pull-down networks are changing state. In that situation, the MOSFETs have large, 10s to 100s of kΩ, channel resistances, which minimizes the current's magnitude. In a MEMS device, where the resistances are under 100-Ω, this current can easily be in the 10s of mA range. To limit this effect, 10-kΩ current limiting resistors were placed on the output side of each relay. While these resistors will hinder the propagation delay of the device, they are placed in a manner that will not increase power consumption. An added benefit of the resistors is that they effectively mitigate resistance asymmetries between devices.

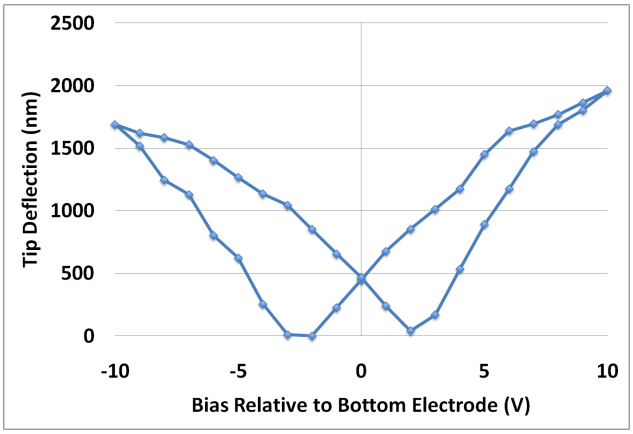

Figure 2: Bipolar Displacement Vs. Voltage for a 25 µm long device.

Table 1: Relevant device performance parameters.

Parameter	Value
Area Range (Varies Based on Device Length)	43 µm x 66 µm to 43 µm x 88 µm
Dynamic Energy Consumption Per Length	143 fJ/µm
Static Leakage Power Per Length	1.5E-2 pW/µm
Typical Contact Resistance	<100 Ω
Capacitance Per Length	6 pF + 0.25 pF/µm
Lifetime (Lab-Air/Unpackaged)	$>10^7$ Cycles

Table 2: Device propagation delay into a 206 pF load.

Relay Length (µm)	Average Delay (ns)	Standard Deviation (ns)
3	200.	27.4
5	191.	25.5
10	203.	48.5
15	257.	52.0
25	358.	135.

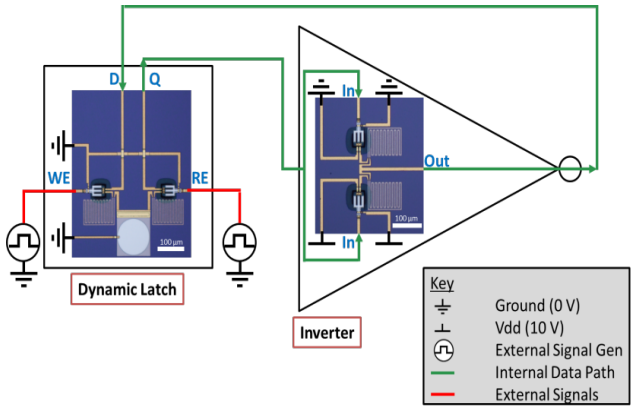

Figure 3: Schematic of the 1-bit MEMS counter composed of a dynamic latch and inverter.

The dynamic latch also utilizes two relays with their output cantilevers and one of their Pt electrodes tied together. Unlike the inverter, however, an additional 105-pF PZT storage capacitor is attached to the shared output cantilever connection. The capacitor's value was chosen to compensate for the parasitic capacitances induced by the testing equipment and thus simplified device characterization. In an actual system, the capacitor intrinsic to each relay would be sufficient for data storage.

For this design, the shared electrode connection was grounded and each relay was actuated independently via the other electrode. One relay was designated the input-enable relay and allowed new data to be written to the capacitor when closed. The other relay was designated the output-enable relay and allowed the stored data to propagate out to the system. Measured results of this operation are shown in Figure 5. Despite the sub-µs propagation delays of the relays, a much slower waveform was used to test the device to evaluate its data-retention capabilities. Alternate configurations of the device to further explore both synchronous and asynchronous operations were described in [7].

While dynamic memory is not appropriate for long-term storage in CMOS systems without being refreshed, it is ideal for a low power mechanical logic process with PZT capacitors. In a typical semiconductor process, a capacitor's parasitic resistance will be low and thus necessitate refreshes on a ms time scale. The thin-film PZT capacitors here, however, have a parasitic resistance >10-TΩ, leading to reliable, long-term storage without consuming any power. As shown in Figure 6, adjusting the high-voltage rail relative to the actuation voltage allows an operator to tailor data retention from a few minutes to several hours.

For the complete system, the two gates were connected in a feedback loop. Each cycle, data stored in the dynamic latch is fed to the inverter, inverted and restored in the latch. This particular design mimics the retrieval and processing of register data, a common task in microcontrollers.

Several parameters went into the development of this system. In addition to the short-circuit currents mentioned previously, a flexibility in terms of actuation voltage variation was also required. A challenge for many MEMS devices has been a variable residual stress in the actuator, resulting in open-state gap variations from wafer-to-wafer [9]. For this process, the open-state gap has been measured to vary from 100-nm to 500-nm. Additionally, small variations also exist between devices on the same wafer. To design a system that incorporates multiple relays, it was important that the system be capable of handling these variations. Therefore, while functional relays with actuators as short as 3-µm have been fabricated, longer 25-µm actuators provided greater deflections for a given voltage. These longer devices, however, come at the cost of increased capacitance and propagation delay. For the initial design of this system, however, minimizing the actuation voltage took precedence over performance. This would help minimize the voltage that would need to be hot-switched across the contacts during operation and allow a larger applied to

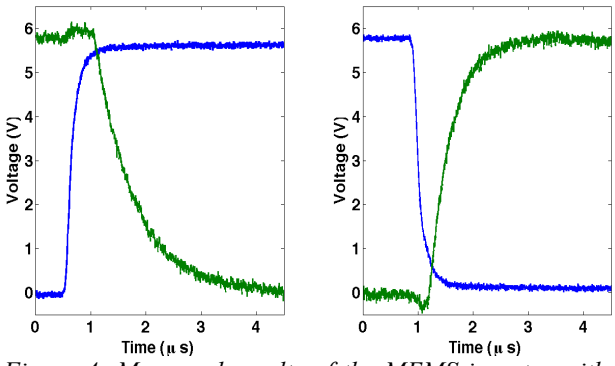

Figure 4: Measured results of the MEMS inverter with a 14-kΩ resistive load in series with 160 pF capacitive load, showing a 920-ns high to low propagation delay (left) and a 520-ns low to high propagation delay (right). The blue curve shows the actuation voltage and the green curve shows the output voltage.

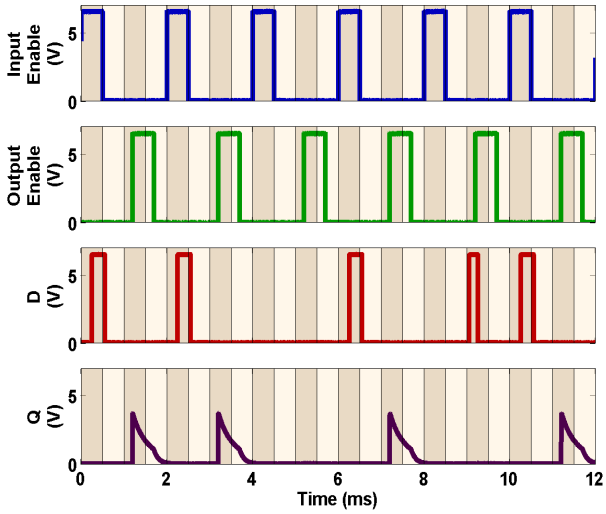

Figure 5: Measured results of the dynamic latch. Note that the glitch introduced between 9 and 9.5-ms does not propagate.

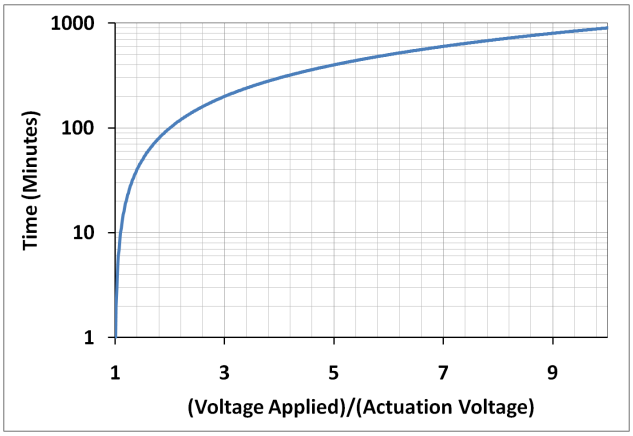

Figure 6: Results extracted from leakage current measurements, showing data persistence relative to the ratio of supply vs. actuation voltage for the PZT capacitors.

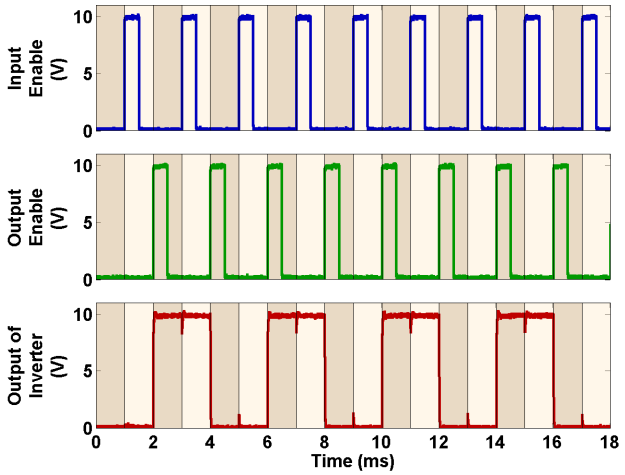

Figure 7:Measured results of the functional MEMS 1-Bit counter.

actuation voltage for increase data retention duration, as shown in Figure 6.

Through simulation with a custom, compact relay model, coupled with design experience garnered during the individual gate development, the system was designed, fabricated and successfully demonstrated in a lab-air environment with measured results shown in Figure 7. Similar to the dynamic latch, the device was operated below its maximum speed to illustrate the data-retention capabilities of the system. Only the high-voltage/ground rail and the latch's read/write enable signals are applied externally; internal data is never externally refreshed.

CONCLUSION

The system presented here provides an additional step towards showing the viability of mechanical logic as an alternative to MOSFETs in low power, embedded applications. An inverter and dynamic latch were combined to produce a system that demonstrated data integrity and repeatability over multiple cycles. Additional considerations were taken to account for variability and hysteresis in device performance. The MEMS relays shown here were previously demonstrated to have low leakage currents, a high on to off-state current ration and the ability to hot-switch a large range of voltages, up to 40-V, across their contacts. Additionally, these devices have integration advantages with existing MEMS components and intrinsic environmental resistances not found with CMOS.

Future efforts are planned to investigate the design variables necessary for consideration when developing more complex, microcontroller systems. Additionally, further optimizations are being examined in the fabrication flow to limit the wafer-to-wafer variation of devices.

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