

# Modeling Timing Variations in Digital Logic Circuits Due to Electrical Fast Transients

Xu Gao <sup>#1</sup>, Chunchun Sui <sup>#2</sup>, Daryl Beetner <sup>#3</sup>, Sameer Hemmady <sup>\*4</sup>, Joey Rivera <sup>\*5</sup>, Susumu Yakura <sup>6</sup>,

Julio Villafuerte <sup>7</sup>, David Pommerneke <sup>#8</sup>

<sup>#</sup> EMC Laboratory, Missouri University of Science and Technology  
Rolla, MO, USA

<sup>1</sup> xg2z7@mst.edu, <sup>2</sup> csdh8@mail.mst.edu, <sup>3</sup> daryl@mst.edu, <sup>8</sup> davidjpm@mst.edu

<sup>\*</sup> TechFlow Scientific-A Division of TechFlow Inc.  
Albuquerque, NM, USA

<sup>4</sup> shemmady@techflow.com, <sup>5</sup> jrivera@techflow.com

**Abstract**—Integrated circuits (ICs) sometimes fail when their power supply is disrupted by external noise, like an electrical fast transient (EFT). Soft failures in these cases are often caused by timing errors in the IC, for example when delays through logic become too large to meet internal timing constraints. Methods are needed to predict when these failures will occur. A closed-form expression is proposed in this paper to predict the change in propagation delay through logic as a result of an EFT on the IC power supply. The expression uses process parameters that can be found from SPICE models of FETs within the IC or through external measurements of the IC when SPICE models are unavailable. The model is used to predict the frequency of a CMOS ring oscillator manufactured in 0.5  $\mu\text{m}$  technology. Predicted results closely match those found through measurements with a maximum relative error of approximately 1%.

## I. INTRODUCTION

Immunity problems in electronic circuits are becoming increasingly important as the number of functions implemented by integrated circuits (ICs) grow and as the IC power supply voltages shrink. Shrinking power supply voltages cause shrinking noise margins, meaning that even small fluctuations in the power supply can cause failures in the IC.

While recent studies have focussed on predicting the level of voltage fluctuation in an IC caused by an external electromagnetic event [1][2], methods are needed to better predict when failures will occur as a result of these fluctuations. Failures may either be soft or hard. Hard failures cause permanent damage to the IC. Soft errors are typically due to incorrect data being read from I/O, internal logic, or memory. The causes of hard errors are generally better understood than soft errors. A common reason for soft errors is that a change in the power supply voltage causes a change in the propagation delay through internal logic or the clock tree, resulting in the clock edge to arrive at register before valid data, so that an incorrect logic value is stored at the register [3]. Methods are developed in the following paper to predict these changes in the propagation delay as a result of changes in the power supply voltage, with the goal of

predicting when errors will occur from events like electrical fast transients (EFTs).

EFTs are usually caused by switching of inductive loads connected to the power distribution network and are a common cause of variations in the power supply voltage of ICs [2]. An EFT has a rise time of several nanoseconds and a pulse width of tens of nanoseconds [4]. The EFT can be coupled to the power pins or I/O pins of the IC.

Delay models for logic gates are available in the literature to help predict maximum clock speed in the presence of simultaneous switching noise on the on-die power supply [5], [6]. These models are extended in the following paper to predict variations in the propagation delay through a logic circuit as a result of an EFT applied to the power supply. While the study focuses on the EFT, results might be readily applied to other immunity problems. The resulting model is used to predict the variation in the frequency of a ring oscillator implemented on a test chip in 0.5  $\mu\text{m}$  technology. Test results show the measurement and modeling results match closely. This delay model can help engineers to predict and prevent potential failures in digital ICs.

## II. DELAY MODEL

The propagation delay through a CMOS inverter, like the one in Fig. 1, is given by [7]:

$$t_{pHL}, t_{pLH} = \left( \frac{1}{2} - \frac{1 - v_T}{1 + \alpha} \right) t_T + \frac{C_L V_{dd}}{2 I_{D0}}, \quad (1)$$

where  $v_T = V_{th}/V_{dd}$ ,  $V_{dd}$  is the power supply voltage,  $V_{th}$  is the threshold voltage,  $\alpha$  is the velocity saturation index for a MOSFET which varies from 1 to 2,  $t_T$  is the rise or fall time of the input signal,  $I_{D0}$  is the drain current when  $V_{GS} = V_{DS} = V_{dd}$ , and  $C_L$  is the load capacitance driven by the gate. The propagation delay is defined as the time between the input signal reaching  $V_{dd}/2$  to the output signal reaching  $V_{dd}/2$ . High-to-low propagation delay times,  $t_{pHL}$ , are dependent on the parameters for nFETs (i.e. on  $V_{th,n}$  and  $\alpha_{th,n}$ ). Low-to-high propagation delay are dependent on pFETs (i.e. on  $V_{th,p}$  and  $\alpha_{th,p}$ ). Both the threshold voltage,  $V_{th}$ , and the velocity

saturation index,  $\alpha$ , are technology dependent. The rise or fall time,  $t_T$ , is a property of the input signal and is often unknown in the propagation delay calculation. If the input signal is generated inside the IC, however, this parameter can be approximated by assuming (1) that each gate has approximately the same drive strength and load capacitance, so the rise and fall time of the input and output are the same; and (2) that the output begins to transition when the input signal reaches a value of  $V_{dd}/2$ . Using these two assumptions, the rise or fall time of the input signal is approximately twice the propagation delay time,  $t_T = 2t_p$ , as illustrated in Fig. 2.

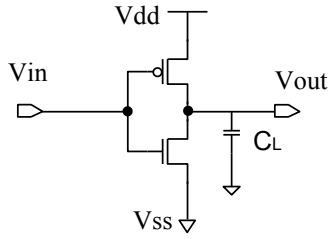


Fig. 1. A MOSFET inverter.

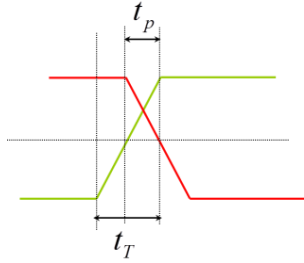


Fig. 2. Relationship between propagation delay time and the rise/ fall time of the input signal.

Using  $t_T = 2t_p$  in (1) gives:

$$t_{pHL}, t_{pLH} = \frac{C_L V_{dd}}{2I_{D0}} \cdot \frac{1+\alpha}{2(1-\nu_T)}. \quad (2)$$

The drain current,  $I_{D0}$ , is given by [7]:

$$I_{D0} = \left( \frac{V_{dd} - V_{th}}{V_{dd,ref} - V_{th}} \right)^\alpha I_{D0,ref}, \quad (3)$$

where  $I_{D0,ref}$  is the drain current when  $V_{GS} = V_{DS} = V_{dd,ref}$ .

Using this relationship gives the propagation delay as:

$$t_{pHL}, t_{pLH} = \frac{C_L}{4} (1+\alpha) \frac{(V_{dd,ref} - V_{th})^\alpha}{I_{D0,ref}} \frac{V_{dd}^2}{(V_{dd} - V_{th})^{\alpha+1}}. \quad (4)$$

Defining the first part of this equation as a constant which is independent of the power supply voltage,

$A = \frac{C_L}{4} (1+\alpha) \frac{(V_{dd,ref} - V_{th})^\alpha}{I_{D0,ref}}$ , (4) can be written as:

$$t_{pHL}, t_{pLH} = A \cdot \frac{V_{dd}^2}{(V_{dd} - V_{th})^{\alpha+1}}. \quad (5)$$

When the load capacitance is unknown, the constant  $A$  will also be unknown.

Because the constant  $A$  is independent on power supply voltage  $V_{dd}$ , the propagation delay of data through many logic gates, rather than just a single gate can be extended from (5). A simple structure representing a generic logic structure is a series of inverters as shown in Fig. 3. In this case, the inverters are configured as a ring oscillator. Equation (5) can be used to predict changes in the delay through the inverter chain, and thus changes in the oscillation frequency of the ring oscillator.

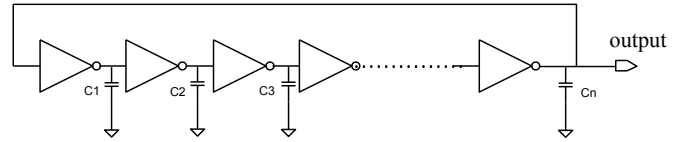


Fig. 3. A ring oscillator.

The propagation delay through the inverter chain is given by:

$$t_{pHL}^{tot} = t_{pHL}^1 + t_{pLH}^2 + t_{pHL}^3 + \dots + t_{pHL}^n \quad (6)$$

$$t_{pLH}^{tot} = t_{pLH}^1 + t_{pLH}^2 + t_{pLH}^3 + \dots + t_{pLH}^n \quad (7)$$

where  $t_{pHL}^i$  and  $t_{pLH}^i$  are the high-to-low and low-to-high propagation delay through the  $i$ th inverter, respectively,  $n$  is an odd integer (to allow oscillation), and  $t_{pHL}^{tot}$  and  $t_{pLH}^{tot}$  are the low-to-high and high-to-low propagation delay through the entire inverter chain. The period of the output oscillation is given by the sum of  $t_{pHL}^{tot}$  and  $t_{pLH}^{tot}$ :

$$T = t_{pHL}^{tot} + t_{pLH}^{tot} \quad (8)$$

Substituting (5) (6) and (7) into (8), the period of the ring oscillator is given by:

$$T = M_n \cdot \frac{V_{dd}^2}{(V_{dd} - V_{th,n})^{\alpha_n+1}} + M_p \cdot \frac{V_{dd}^2}{(V_{dd} + V_{th,p})^{\alpha_p+1}} \quad (9)$$

where  $M_n$  and  $M_p$  are unknown constants, associated with  $A$  in (5).

Because  $M_n$  and  $M_p$  are independent of the power supply voltage, they can be calculated by measuring the periods of the oscillator,  $T_1$  and  $T_2$ , at two different power supply voltages,  $V_{dd,1}$  and  $V_{dd,2}$ . The constants can be found by solving the equation:

$$\begin{bmatrix} N_1 & P_1 \\ N_2 & P_2 \end{bmatrix} \begin{bmatrix} M_n \\ M_p \end{bmatrix} = \begin{bmatrix} T_1 \\ T_2 \end{bmatrix} \quad (10)$$

where

$$N_i = \frac{V_{dd,i}^2}{(V_{dd,i} - V_{th,n})^{\alpha_n+1}}, \quad (11)$$

and

$$P_i = \frac{V_{dd,i}^2}{(V_{dd,i} + V_{th,p})^{\alpha_p+1}}. \quad (12)$$

### III. VALIDATION

The delay model in (9) was validated through experiments on a test IC implemented in 0.5 micron technology. While the 0.5 micron technology is relatively old, the basis for the delay models should not be substantially different for a newer technology [5]. A ring oscillator with 11 inverters was implemented in the test IC. The frequency of oscillation was measured while applying EFTs to the power supply input.

Fig. 4 shows the test setup. An EFT generator was connected to the IC Vdd pin through a 40 dB attenuator and a 33 nF capacitor. The 40 dB attenuator was used to avoid physical damage to the IC. A 4.7 nF off-chip decoupling capacitor was mounted near to the  $V_{dd}$  pin of the test IC to minimize switching noise from the IC itself. A DC power supply was connected to the  $V_{dd}$  pin through a ferrite and inductor to decouple the power supply from the EFT test. The  $V_{dd}$  pin and the output of the ring oscillator were monitored using a 1 kohm resistive probe.

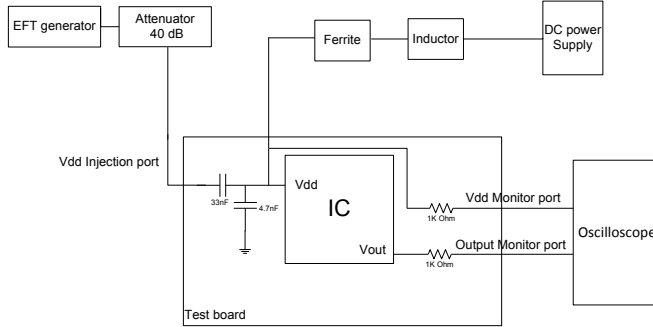


Fig. 4. Test setup.

Fig. 5 shows one test result when the EFT generator was set to negative 600 V. The top plot shows the waveform at the  $V_{dd}$  pin of the IC. The middle plot shows the waveform at the output pin of ring oscillator. The bottom plot shows the frequency of the output oscillation. The voltage on  $V_{dd}$  dropped during the EFT injection. As  $V_{dd}$  dropped, the frequency of the oscillation also decreased, which means that the propagation delay in the inverter chain increased. This increasing propagation delay through the logic gates in IC could cause timing errors in the digital IC.

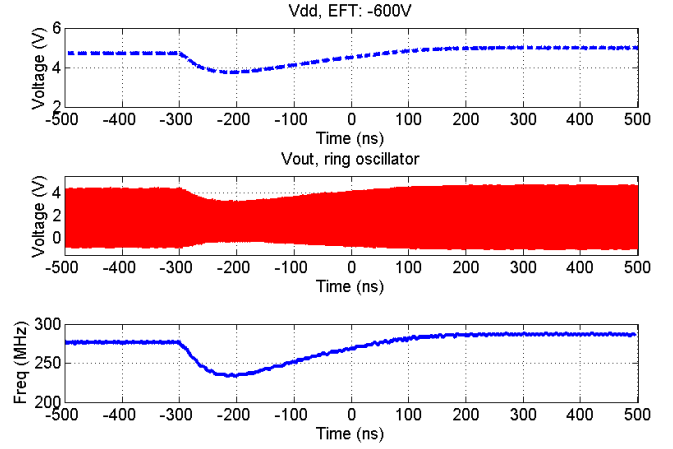


Fig. 5. Test results during a negative 600 V EFT.

### IV. MODELING RESULTS

The measured power supply voltage was used in (9) to predict the period and/or frequency of the ring oscillator during an EFT event. Fig. 6 shows a comparison of the predicted and measured results during a negative 600 V EFT. The predicted and measured frequency matched well, with a maximum relative error of 1.15%.

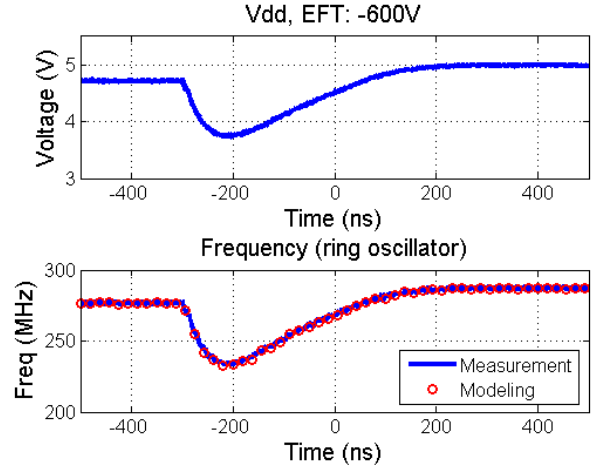


Fig. 6. Waveform on Vdd during a negative 600 V EFT and the corresponding frequency of the ring oscillator.

In this modeling process, the two unknown constant  $M_n$  and  $M_p$  in (9) can be calculate from an immunity test. For example, in Fig. 6, two different  $V_{dd}$  values were selected to calculate  $N_i$  and  $P_i$  in (11). The values of  $T_1$  and  $T_2$  in (11) are the periods of the ring oscillator corresponding the two different values of  $V_{dd}$ . Once  $M_n$  and  $M_p$  were determined, they were used to predict delays in EFT immunity tests.

The model was further tested with EFTs of different amplitude levels and with both polarities. Fig. 7 shows a comparison of predicted and measured oscillation frequencies for EFT injections at negative 400 V, 600 V and 800 V.

Similar results are shown in Fig. 8 for positive 400 V, 600 V and 800 V EFTs. The results in Fig. 7 and Fig. 8 demonstrate that the proposed model can accurately predict the frequency variations within the ring oscillator during an EFT immunity test, given the correct voltage on  $V_{dd}$ .

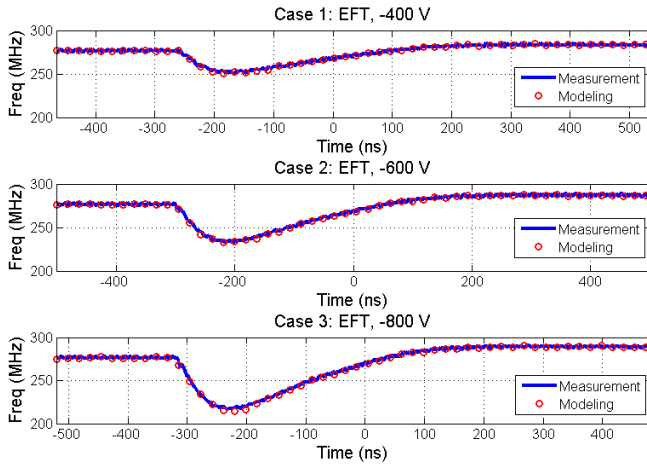


Fig. 7. Measured and predicted frequency of the ring oscillator during negative EFTs.

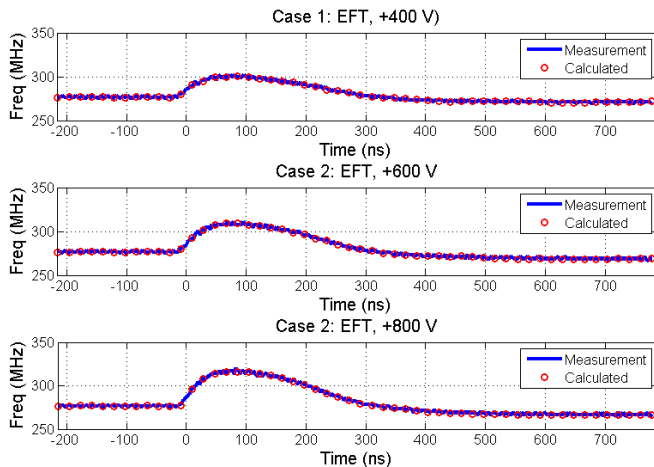


Fig. 8. Measured and predicted frequency of the ring oscillator during positive EFTs.

## V. POWER SUPPLY WAVEFORM MODELING

In the previous section, the measured waveform on  $V_{dd}$  was used to predict the delays through the logic gates. In a more generic case, however, one would like to predict the  $V_{dd}$  waveform from the test setup. The circuit model in Fig. 9 was developed to predict the waveform on the  $V_{dd}$  bus during an EFT test when noise is injected to the  $V_{dd}$  of the test IC. The circuit includes a model of the EFT generator, lumped components on PCB board, and a model for the IC. The EFT generator is modelled using voltage source which creates a waveform measured from an actual EFT generator. The lumped components on PCB board include a 47  $\mu$ H

decoupling inductor and ferrite used to decouple the DC power supply from the EFT test, and a 4.7 nF on-board decoupling capacitor. The model of the IC includes a simple model of the package and the on-die power delivery network. A non-linear resistor is used to represent the non linear relationship between  $V_{dd}$  the switching current consumed by the test IC.

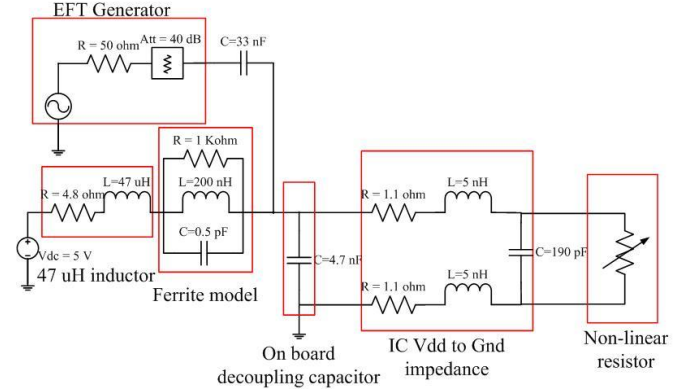


Fig. 9. Circuit model to predict the waveform on the  $V_{dd}$  bus during an EFT test.

Measured and predicted voltage waveforms on  $V_{dd}$  are shown in Fig. 10 when the EFT generator was set to positive or negative 600 or 800 V. The results demonstrate that the  $V_{dd}$  waveform can be accurately predicted using this model.

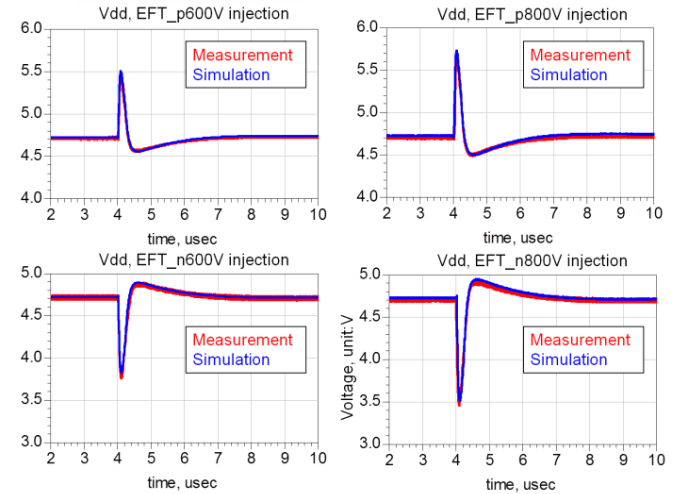


Fig. 10. Modeling results for  $V_{dd}$  waveform

## VI. CONCLUSION

An analytical model was developed to predict timing variations in digital logic as a result of variations in the power supply voltage. The model was validated by applying EFTs to a ring oscillator built in a test IC. The predicted and measured ring oscillator frequencies agreed closely, illustrating the accuracy of the approach. While tests were performed on only a simple inverter chain using EFTs, the model should be

applicable to a much wider class of problems. It should straightforward to use this model to predict propagation delays through generic logic that occurs within a digital IC and to apply this model to other sources of power supply noise. The key is to first predict the variation in the power supply voltage from these events. Future work will focus on applying these equations to more complex problems in realistic IC structures, and to evaluate the combined effect of these delay variations on the clock-tree and the internal logic in the development of logic errors.

#### REFERENCES

- [1] J. Zhang, D. Beetner, R. Moseley, S. Herrin, D. Pommerenke, "Modeling electromagnetic field coupling from an ESD gun to an IC," *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on*, pp. 553-8, Aug 2011.
- [2] Ji Zhang, J. Koo, D. G. Beetner, R. Moseley, S. Herrin, D. Pommerenke, "Modeling of the immunity of ICs to EFTs," *Electromagnetic Compatibility (EMC), 2010 IEEE International Symposium on*, pp.484-489, 2010.
- [3] J. G. Tront, "Predicting URF upset of MOSFET digital IC's," *IEEE Trans. Electromagn. Compat.*, vol. EMC-27, pp. 64-69, May 1985.
- [4] EMC—Part 4-4: Testing and measurement techniques—Electrical fast transient /burst immunity test, *IEC International Standard 61000-4-4*, 2004
- [5] M. Alioto and G. Palumbo, "Impact of supply voltage variations on full adder delay: Analysis and comparison," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1322–1335, Dec. 2006.
- [6] M. Saint-Laurent and M. Swaminathan, "Impact of power-supply noise on timing in high-frequency microprocessors," *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 135–144, Feb. 2004.
- [7] T. Sakurai and R. Newton, "Alpha-power law MOSFET model and it's applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, pp. 584–594, Apr. 1990.